PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Book IC04 1988

HE4000B logic family

CMOS

HE4000B LOGIC FAMILY
CMOS

SELECTION GUIDE

CMOS HE4000B FAMILY SURVEY

Type numbers have a suffix which signifies the type of package and burn-in option:
P = plastic DIL; D = ceramic (cerdip) DIL; T = plastic SO mini-pack; 2nd B = burn-in option

extended type no.	package code	no. of pins	pin position	category	page
HEC4001BDB	SOT73	14	DIL	gates	151
HEC4002BDB	SOT73	14	DIL	gates	161
HEC4007UBDB	SOT73	14	DIL	gates	167
HEC40097BDB	SOT74	16	DIL	buffers	751
HEC40098BDB	SOT74	16	DIL	buffers	755
HEC4011BDB	SOT73	14	DIL	gates	179
HEC4012BDB	SOT73	14	DIL	gates	189
HEC4013BDB	SOT73	14	DIL	flip-flops	191
HEC4014BDB	SOT74	16	DIL	MSI	197
HEC4015BDB	SOT74	16	DIL	MSI	203
HEC4016BDB	SOT73	14	DIL	gates	207
HEC4017BDB	SOT74	16	DIL	MSI	215
HEC40174BDB	SOT74	16	DIL	MSI	805
HEC40175BDB	SOT74	16	DIL	MSI	809
HEC4019BDB	SOT74	16	DIL	MSI	229
HEC40194BDB	SOT74	16	DIL	MSI	829
HEC40195BDB	SOT74	16	DIL	MSI	835
HEC4020BDB	SOT74	16	DIL	MSI	233
HEC4023BDB	SOT73	14	DIL	gates	253
HEC4024BDB	SOT73	14	DIL	MSI	255
HEC4025BDB	SOT73	14	DIL	gates	259
HEC4027BDB	SOT74	16	DIL	flip-flops	261
HEC4030BDB	SOT73	14	DIL	gates	283
HEC4035BDB	SOT74	16	DIL	MSI	291
HEC4040BDB	SOT74	16	DIL	MSI	299
HEC4042BDB	SOT74	16	DIL	MSI	305
HEC4047BDB	SOT73	14	DIL	MSI	333
HEC4049BDB	SOT74	16	DIL	buffers	347
HEC4050BDB	SOT74	16	DIL	buffers	349
HEC4051BDB	SOT74	16	DIL	MSI	351
HEC4066BDB	SOT73	14	DIL	gates	389
HEC4068BDB	SOT73	14	DIL	gates	405
HEC4069UBDB	SOT73	14	DIL	gates	407
HEC4070BDB	SOT73	14	DIL	gates	413
HEC4071BDB	SOT73	14	DIL	gates	415
HEC4073BDB	SOT73	14	DIL	gates	419
HEC4081BDB	SOT73	14	DIL	gates	433
HEC4093BDB	SOT73	14	DIL	gates	443
HEC4094BDB	SOT74	16	DIL	MSI	449
HEC4505BDB	SOT73	14	DIL	LSI	465

extended type no.	package code	no. of pins	pin position	category	page
HEF40098BP	SOT38Z	16	DIL	buffers	755
HEF40098BT	SOT109A	16	SO16	buffers	755
HEF40106BD	SOT73	14	DIL	gates	759
HEF40106BP	SOT27	14	DIL	gates	759
HEF40106BT	SOT108A	14	SO14	gates	759
HEF4011BD	SOT73	14	DIL	gates	179
HEF4011BP	SOT27	14	DIL	gates	179
HEF4011BT	SOT108A	14	SO14	gates	179
HEF4011UBD	SOT73	14	DIL	gates	181
HEF4011UBP	SOT27	14	DIL	gates	181
HEF4011UBT	SOT108A	14	SO14	gates	181
HEF4012BD	SOT73	14	DIL	gates	189
HEF4012BP	SOT27	14	DIL	gates	189
HEF4012BT	SOT108A	14	SO14	gates	189
HEF4013BD	SOT73	14	DIL	flip-flops	191
HEF4013BP	SOT27	14	DIL	flip-flops	191
HEF4013BT	SOT108A	14	SO14	flip-flops	191
HEF4014BD	SOT74	16	DIL	MSI	197
HEF4014BP	SOT38Z	16	DIL	MSI	197
HEF4014BT	SOT109A	16	SO16	MSI	197
HEF4015BD	SOT74	16	DIL	MSI	203
HEF4015BP	SOT38Z	16	DIL	MSI	203
HEF4015BT	SOT109A	16	SO16	MSI	203
HEF4016BD	SOT73	14	DIL	gates	207
HEF4016BP	SOT27	14	DIL	gates	207
HEF4016BT	SOT108A	14	SO14	gates	207
HEF40160BD	SOT74	16	DIL	MSI	765
HEF40160BP	SOT38Z	16	DIL	MSI	765
HEF40160BT	SOT109A	16	SO16	MSI	765
HEF40161BD	SOT74	16	DIL	MSI	775
HEF40161BP	SOT38Z	16	DIL	MSI	775
HEF40161BT	SOT109A	16	SO16	MSI	775
HEF40162BD	SOT74	16	DIL	MSI	785
HEF40162BP	SOT38Z	16	DIL	MSI	785
HEF40162BT	SOT109A	16	SO16	MSI	785
HEF40163BD	SOT74	16	DIL	MSI	795
HEF40163BP	SOT38Z	16	DIL	MSI	795
HEF40163BT	SOT109A	16	SO16	MSI	795
HEF4017BD	SOT74	16	DIL	MSI	215
HEF4017BP	SOT38Z	16	DIL	MSI	215

extended type no.	package code	no. of pins	pin position	category	page
HEF4017BT	SOT109A	16	SO16	MSI	215
HEF40174BD	SOT74	16	DIL	MSI	805
HEF40174BP	SOT38Z	16	DIL	MSI	805
HEF40174BT	SOT109A	16	SO16	MSI	805
HEF40175BD	SOT74	16	DIL	MSI	809
HEF40175BP	SOT38Z	16	DIL	MSI	809
HEF40175BT	SOT109A	16	SO16	MSI	809
HEF4018BD	SOT74	16	DIL	MSI	223
HEF4018BP	SOT38Z	16	DIL	MSI	223
HEF4018BT	SOT109A	16	SO16	MSI	223
HEF4019BD	SOT74	16	DIL	MSI	229
HEF4019BP	SOT38Z	16	DIL	MSI	229
HEF4019BT	SOT109A	16	SO16	MSI	229
HEF40192BD	SOT74	16	DIL	MSI	813
HEF40192BP	SOT38Z	16	DIL	MSI	813
HEF40192BT	SOT109A	16	SO16	MSI	813
HEF40193BD	SOT74	16	DIL	MSI	821
HEF40193BP	SOT38Z	16	DIL	MSI	821
HEF40193BT	SOT109A	16	SO16	MSI	821
HEF40194BD	SOT74	16	DIL	MSI	829
HEF40194BP	SOT38Z	16	DIL	MSI	829
HEF40194BT	SOT109A	16	SO16	MSI	829
HEF40195BD	SOT74	16	DIL	MSI	835
HEF40195BP	SOT38Z	16	DIL	MSI	835
HEF40195BT	SOT109A	16	SO16	MSI	835
HEF4020BD	SOT74	16	DIL	MSI	233
HEF4020BP	SOT38Z	16	DIL	MSI	233
HEF4020BT	SOT109A	16	SO16	MSI	233
HEF4021BD	SOT74	16	DIL	MSI	239
HEF4021BP	SOT38Z	16	DIL	MSI	239
HEF4021BT	SOT109A	16	SO16	MSI	239
HEF4022BD	SOT74	16	DIL	MSI	245
HEF4022BP	SOT38Z	16	DIL	MSI	245
HEF4022BT	SOT109A	16	SO16	MSI	245
HEF4023BD	SOT73	14	DIL	gates	253
HEF4023BP	SOT27	14	DIL	gates	253
HEF4023BT	SOT108A	14	SO14	gates	253
HEF4024BD	SOT73	14	DIL	MSI	255
HEF4024BP	SOT27	14	DIL	MSI	255
HEF4024BT	SOT108A	14	SO14	MSI	255

extended type no.	package code	no. of pins	pin position	category	page
HEF40240BP	SOT146	20	DIL	buffers	843
HEF40240BT	SOT163A	20	SO20	buffers	843
HEF40244BP	SOT146	20	DIL	buffers	849
HEF40244BT	SOT163A	20	SO20	buffers	849
HEF40245BP	SOT146	20	DIL	buffers	855
HEF40245BT	SOT163A	20	SO20	buffers	855
HEF4025BD	SOT73	14	DIL	gates	259
HEF4025BP	SOT27	14	DIL	gates	259
HEF4025BT	SOT108A	14	SO14	gates	259
HEF4027BD	SOT74	16	DIL	flip-flops	261
HEF4027BP	SOT38Z	16	DIL	flip-flops	261
HEF4027BT	SOT109A	16	SO16	flip-flops	261
HEF4028BD	SOT74	16	DIL	MSI	267
HEF4028BP	SOT38Z	16	DIL	MSI	267
HEF4028BT	SOT109A	16	SO16	MSI	267
HEF4029BD	SOT74	16	DIL	MSI	271
HEF4029BP	SOT38Z	16	DIL	MSI	271
HEF4029BT	SOT109A	16	SO16	MSI	271
HEF4030BD	SOT73	14	DIL	gates	283
HEF4030BP	SOT27	14	DIL	gates	283
HEF4030BT	SOT108A	14	SO14	gates	283
HEF4031BD	SOT74	16	DIL	MSI	285
HEF4031BP	SOT38Z	16	DIL	MSI	285
HEF4031BT	SOT109A	16	SO16	MSI	285
HEF4035BD	SOT74	16	DIL	MSI	291
HEF4035BP	SOT38Z	16	DIL	MSI	291
HEF4035BT	SOT109A	16	SO16	MSI	291
HEF40373BP	SOT146	20	DIL	MSI	861
HEF40373BT	SOT163A	20	SO20	MSI	861
HEF40374BP	SOT146	20	DIL	MSI	867
HEF40374BT	SOT163A	20	SO20	MSI	867
HEF4040BD	SOT74	16	DIL	MSI	299
HEF4040BP	SOT38Z	16	DIL	MSI	299
HEF4040BT	SOT109A	16	SO16	MSI	299
HEF4041BD	SOT73	14	DIL	buffers	303
HEF4041BP	SOT27	14	DIL	buffers	303
HEF4041BT	SOT108A	14	SO14	buffers	303
HEF4042BD	SOT74	16	DIL	MSI	305
HEF4042BP	SOT38Z	16	DIL	MSI	305
HEF4042BT	SOT109A	16	SO16	MSI	305

extended type no.	package code	no. of pins	pin position	category	page
HEF4518BP	SOT38Z	16	DIL	MSI	527
HEF4518BT	SOT109A	16	SO16	MSI	527
HEF4519BD	SOT74	16	DIL	MSI	533
HEF4519BP	SOT38Z	16	DIL	MSI	533
HEF4519BT	SOT109A	16	SO16	MSI	533
HEF4520BD	SOT74	16	DIL	MSI	537
HEF4520BP	SOT38Z	16	DIL	MSI	537
HEF4520BT	SOT109A	16	SO16	MSI	537
HEF4521BD	SOT74	16	DIL	MSI	543
HEF4521BP	SOT38Z	16	DIL	MSI	543
HEF4521BT	SOT109A	16	SO16	MSI	543
HEF4522BD	SOT74	16	DIL	MSI	553
HEF4522BP	SOT38Z	16	DIL	MSI	553
HEF4522BT	SOT109A	16	SO16	MSI	553
HEF4526BD	SOT74	16	DIL	MSI	563
HEF4526BP	SOT38Z	16	DIL	MSI	563
HEF4526BT	SOT109A	16	SO16	MSI	563
HEF4527BD	SOT74	16	DIL	MSI	573
HEF4527BP	SOT38Z	16	DIL	MSI	573
HEF4527BT	SOT109A	16	SO16	MSI	573
HEF4528BD	SOT74	16	DIL	MSI	581
HEF4528BP	SOT38Z	16	DIL	MSI	581
HEF4528BT	SOT109A	16	SO16	MSI	581
HEF4531BD	SOT74	16	DIL	MSI	587
HEF4531BP	SOT38Z	16	DIL	MSI	587
HEF4531BT	SOT109A	16	SO16	MSI	587
HEF4532BD	SOT74	16	DIL	MSI	591
HEF4532BP	SOT38Z	16	DIL	MSI	591
HEF4532BT	SOT109A	16	SO16	MSI	591
HEF4534BD	SOT94	24	DIL	LSI	599
HEF4534BP	SOT101A	24	DIL	LSI	599
HEF4534BT	SOT137A	24	SO24	LSI	599
HEF4538BD	SOT74	16	DIL	MSI	607
HEF4538BP	SOT38Z	16	DIL	MSI	607
HEF4538BT	SOT109A	16	SO16	MSI	607
HEF4539BD	SOT74	16	DIL	MSI	615
HEF4539BP	SOT38Z	16	DIL	MSI	615
HEF4539BT	SOT109A	16	SO16	MSI	615
HEF4541BD	SOT73	14	DIL	MSI	619
HEF4541BP	SOT27	14	DIL	MSI	619

extended type no.	package code	no. of pins	pin position	category	page
HEF4753BD	SOT133B	18	DIL	LSI	725
HEF4753BP	SOT102	18	DIL	LSI	725
HEF4754VD	SOT135A	28	DIL	LSI	733
HEF4754VP	SOT117	28	DIL	LSI	733
HEF4754VT	SOT136A	28	SO28	LSI	733
HEF4755VD	SOT135A	28	DIL	LSI	739
HEF4755VP	SOT117	28	DIL	LSI	739
HEF4755VT	SOT136A	28	SO28	LSI	739

GENERAL

Rating systems

Handling MOS devices

CECC qualified products

Burn-in options

Ordering information

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

CECC QUALIFIED PRODUCTS

INTRODUCTION

The CECC Quality System, which dates from 1973, facilitates international trade by the publication of harmonized specifications and quality assessment procedures for electronic components. CECC approval is issued by independent, nationally recognized, National Supervisory Inspectorates (NSI). Our CMOS quality control programme is based on the rules and procedures laid down by the CECC and our manufacturing activities have received official CECC approval.

Our CMOS ICs are qualified to the generic specification CECC 90 000 (latest issue) and the family specifications CECC 90 109.

CECC - WHAT ARE CUSTOMERS OFFERED?

- ICs wholly manufactured in CECC approved premises.
- ICs released by an Inspection Organization which is approved by the National Supervising Inspectorate (NSI).
- ICs released in accordance with CECC adopted specifications.
- Mandatory sample life tests and environmental tests.
- Delivery in packages which are sealed with the mark of conformity under supervision of the NSI.
- Certified test records compiled every six months and available on request.
- Audits of the production facilities by the NSI.

THE CECC SCHEME

CECC is a scheme for providing electronic components of assessed quality controlled by the National Supervising Inspectorate (NSI, e.g. KEMA). It is set up by the CENELEC (European Committee for Electrotechnical Standardization) Electronic Components Committee (CECC) and the International Electrotechnical Commission (IEC).

The CECC scheme includes two essential features of any Quality Assurance Scheme:
— a specification system,
— a certification procedure supported by an independent inspectorate.

CECC IN OPERATION

The CECC scheme operates essentially in three parts.

Part 1: the plant qualification
Part 2: the device qualification
Part 3: quality conformance inspection of deliveries

Part 1

Established to the satisfaction of the NSI that the organization has adequate quality systems, procedures and standards to control the manufacturing of electronic components to the minimum standard as defined in the CECC system.

Part 2

Established by demonstration to the NSI that the electronic components are capable of meeting the requirements of detail specifications which are prepared in accordance with the CECC system. This is accomplished by performing the qualification activity.

Part 3

Established on a lot-by-lot and periodic sampling basis such that the ICs conform to the specifications to which they were initially qualified. Data on the results of these tests are provided as Certified Test Records (CTRs), certified by a representative of the NSI and published at six-monthly intervals.

CECC - QUALIFICATION FEATURES

Lot-by-lot tests

Group A inspection

Group A prescribes the visual examination and electrical measurements to be made on a lot-by-lot basis to assess the principal electrical properties of a circuit (see CECC 00 107).
Group A inspection is divided into appropriate Sub-Groups.

Group B inspection

Group B prescribes the procedures to be used on a lot-by-lot basis to assess certain additional properties of the circuit, including environmental and endurance tests which can be completed in less than one week (see CECC 00 107).
Group B inspection is divided into appropriate Sub-Groups.

Periodic tests

Group C inspection

Group C prescribes the procedures to be used on a periodic basis to assess certain properties of the circuit including environmental and endurance tests which are appropriate for checking at intervals of 3 months.
Group C inspection is divided into appropriate Sub-Groups.

Group D inspection

Group D prescribes the procedures to be used on a periodic basis at intervals of 12 months.

CECC - QUALIFICATION PROCEDURE

- Raise detail specification in accordance with appropriate rules.
- Detail specification approved by NSI and NAI (National Authorized Institution).
- Submit 3 separate lots for qualification.
- Pass all group A and B tests on each of the 3 lots.
- Pass all group C tests on a combined sample from the 3 lots.
- Pass all group C tests, except test C8 (endurance).
- Pass C8 endurance test at 2000 hours, submit test records countersigned by supervising inspector and apply for provisional approval.

CECC - PRODUCTS

Our CMOS products are available up to the highest assessment level P. Products qualified by CECC are recognized by the symbol on the individual data sheets in this handbook and in the Qualified Parts List (Q.P.L.) CECC 00 200 (latest issue), which is available at the National Authorized Institutions. The appropriate CECC detail specification number is also given.

BURN-IN OPTIONS

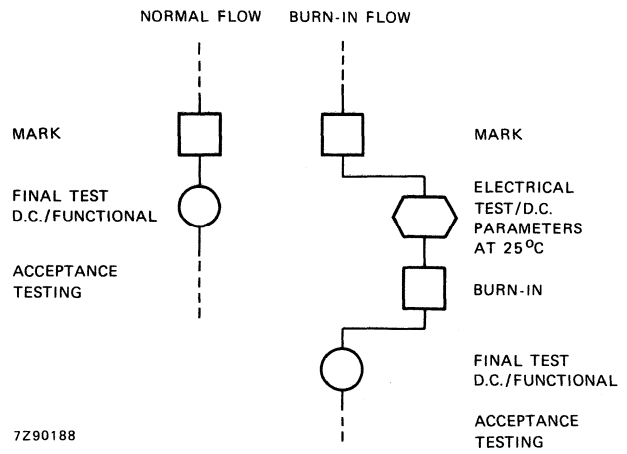
Production quality control ensures that the quality inherent in a design is realized during manufacture of our CMOS integrated circuits. This is achieved by monitoring the quality, both conformity and reliability, of finished ICs; by inspection of the materials and components to be used in the process; by calibration of the equipment; and by monitoring the temperature, humidity and dust content of the manufacturing area.

Careful integration of the production and quality-control functions is essential for good and improving quality.

The BURN-IN option is an additional feature and is available on all our plastic and ceramic (cerdip) DIL packaged CMOS ICs. The features are:

- reduced infant mortality
- reduced printed-circuit board and system re-design
- reduced equipment down-time
- reduced field failures

Flow-charts

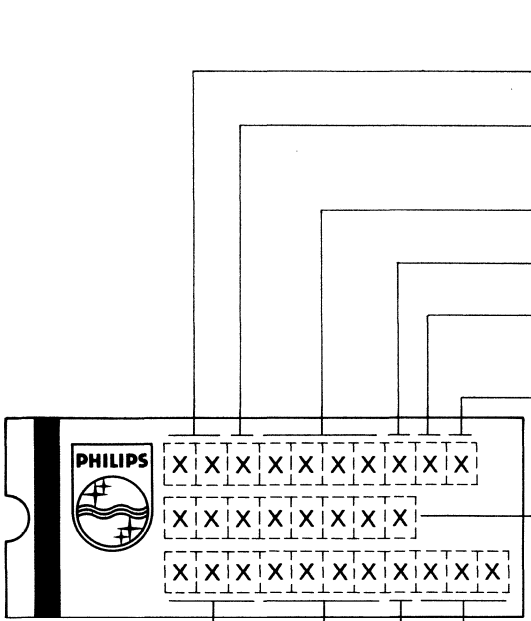


Burn-in is performed under the following conditions:

V_{DD}	15 V	
T_{amb}	125 °C	or equivalent
time	168 hours	
bias	static	

ORDERING INFORMATION

MARKING



EXTENDED TYPE NUMBER

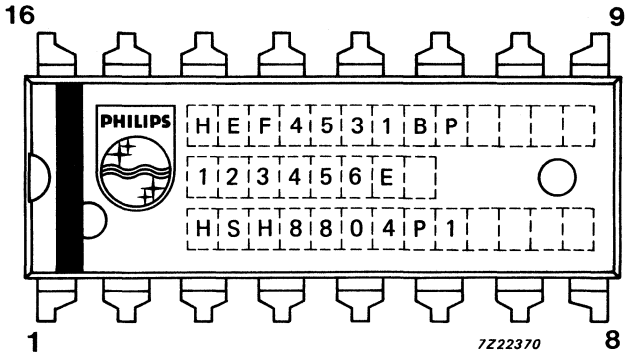
HE	family identification
C or F	operating temperature range: C = full; F = limited
4XXX	device number (up to 5 digits)
B	JEDEC 'B' series CMOS specification
D, P or T	package code: D = ceramic; P = plastic; T = SO (small-outline plastic mini-pack)
X	screening class: B = burn-in

DIFFUSION NUMBER and
ENVELOPE TECHNOLOGY CODE

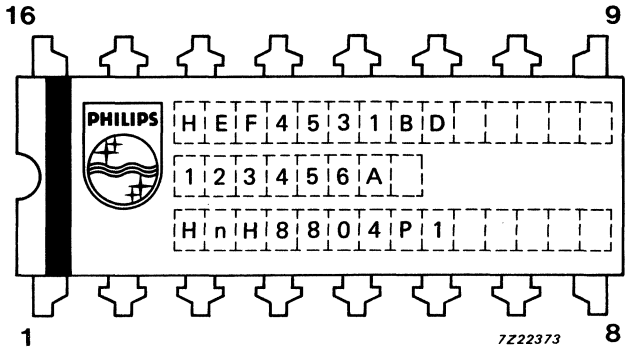
PRODUCTION INFORMATION

- layout number and product status
- CECC quality assessment level
- date code
- factory identification

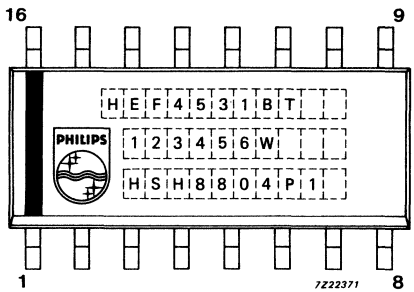
MARKING EXAMPLES



Example of 16-lead dual in-line plastic package.



Example of 16-lead dual in-line ceramic package.



Example of 16-lead small-outline plastic SO mini-pack.

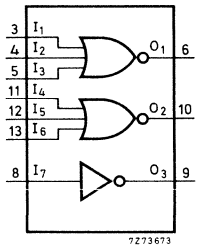
ORDERING

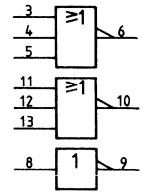
When ordering, please state:

- the quantity required;
- the operating temperature range (HEC or HEF followed by the device number);
- the package code (D = ceramic, P = plastic DIL, T = plastic SO mini-pack);
- the screening class (B) if burn-in option is required.

FUNCTIONAL DIAGRAMS/ IEC SYMBOLS

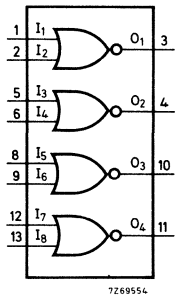
HEF4000B





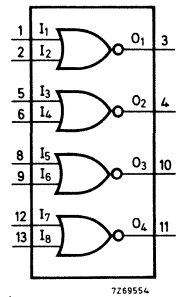
Dual 3-input NOR gate and inverter.

HEF4001B

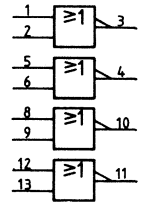


Quadruple 2-input NOR gate.

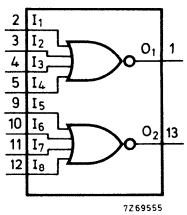
HEF4001UB

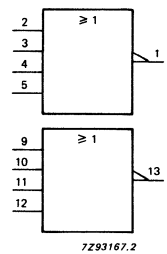


Quadruple 2-input NOR gate; unbuffered.



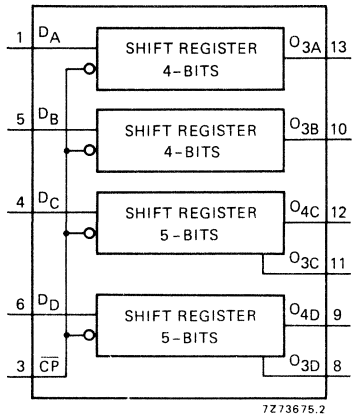
HEF4002B

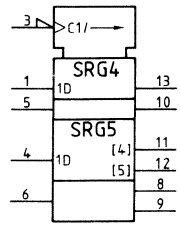




Dual 4-input NOR gate.

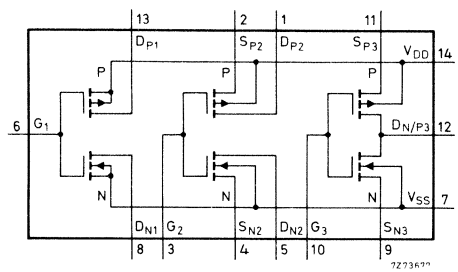
HEF4006B





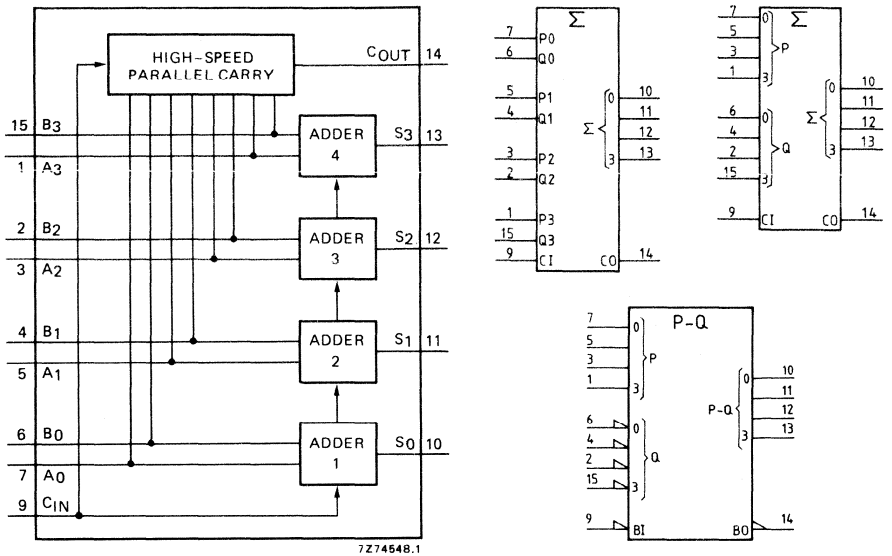
18-stage static shift register.

HEF4007UB



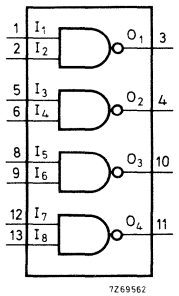
Dual complementary pair and inverter; unbuffered.

HEF4008B



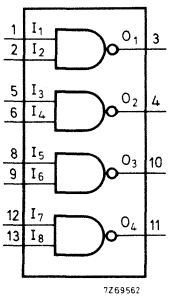
4-bit binary full adder.

HEF4011B

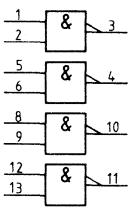


Quadruple 2-input NAND gate.

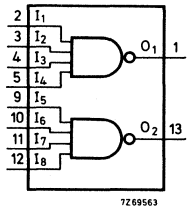
HEF4011UB

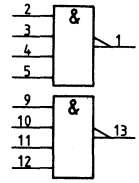


Quadruple 2-input NAND gate; unbuffered.



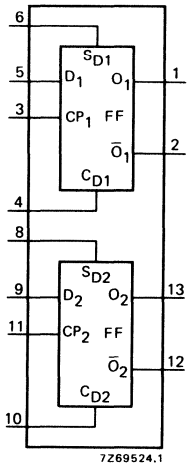
HEF4012B

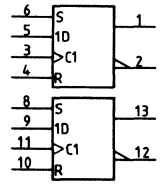




Dual 4-input NAND gate.

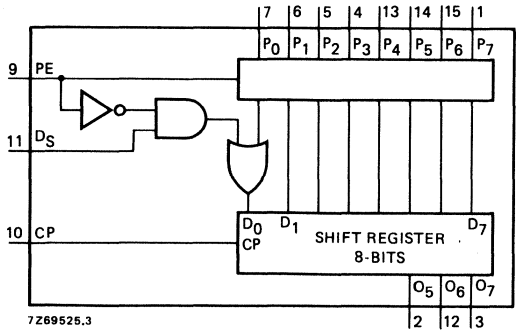
HEF4013B

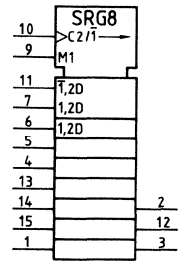




Dual D-type flip-flop.

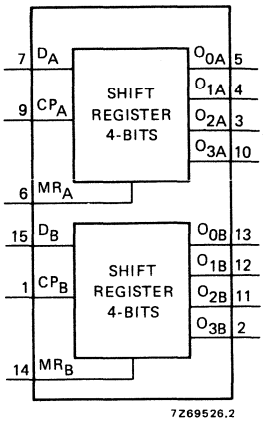
HEF4014B

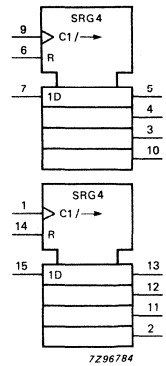




8-bit static shift register.

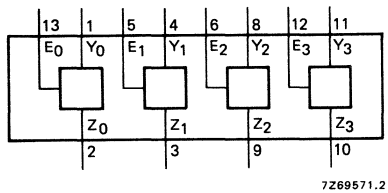
HEF4015B

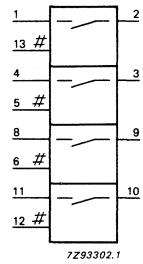


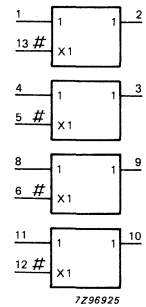


Dual 4-bit static shift register.

HEF4016B

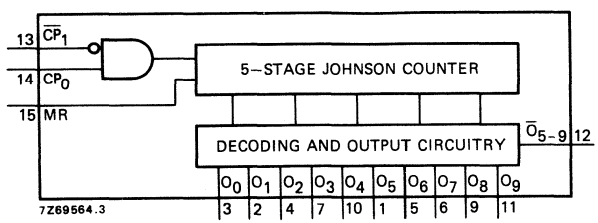


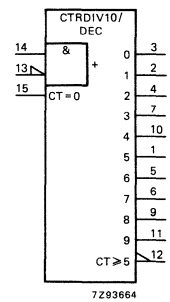




Quadruple bilateral switches.

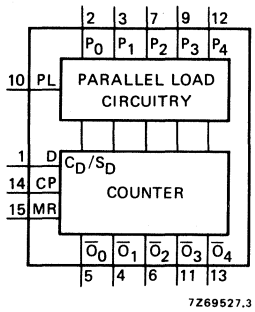
HEF4017B

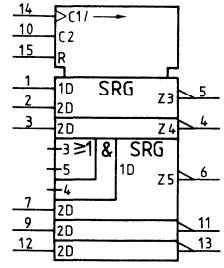




5-stage Johnson counter.

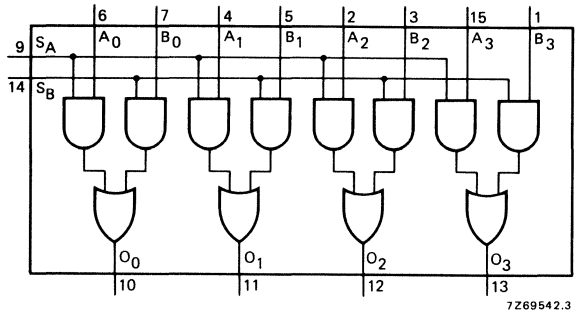
HEF4018B

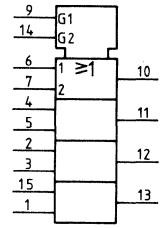




Presettable divide-by-n counter.

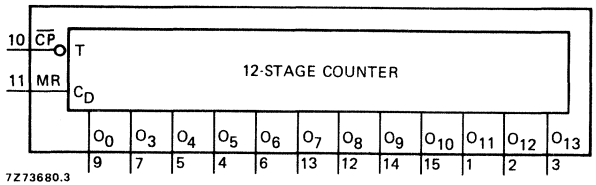
HEF4019B

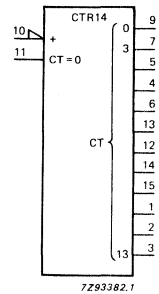




Quadruple 2-input multiplexer.

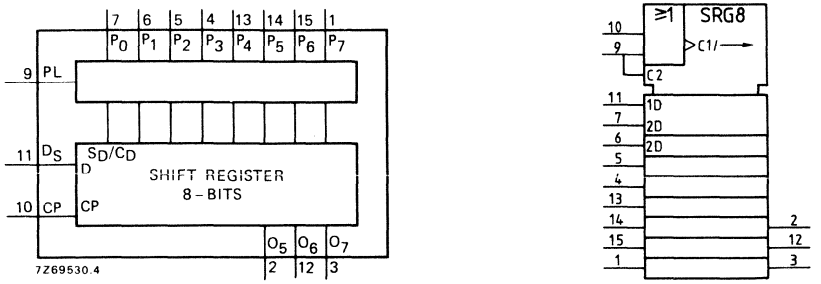
HEF4020B





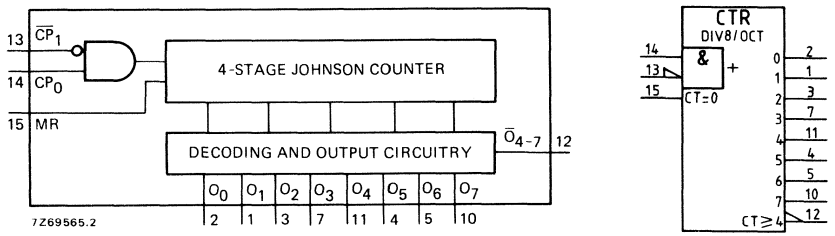
14-stage binary counter.

HEF4021B



8-bit static shift register.

HEF4022B

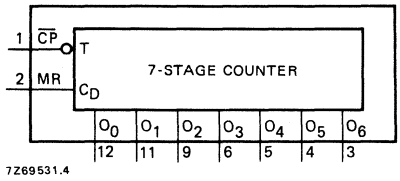


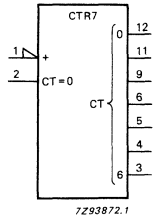
4-stage divide-by-8 Johnson counter.

HEF4023B

Triple 3-input NAND gate.

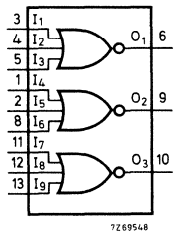
HEF4024B

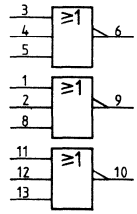




7-stage binary counter.

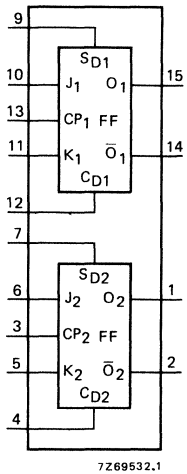
HEF4025B

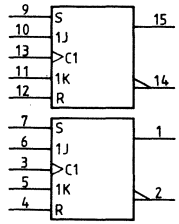




Triple 3-input NOR gate.

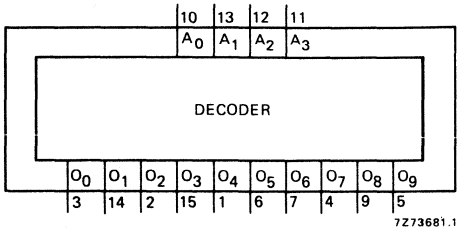
HEF4027B

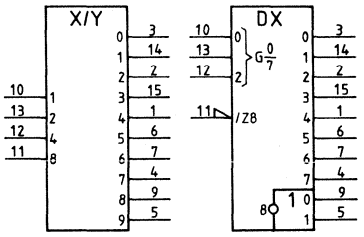




Dual JK flip-flop.

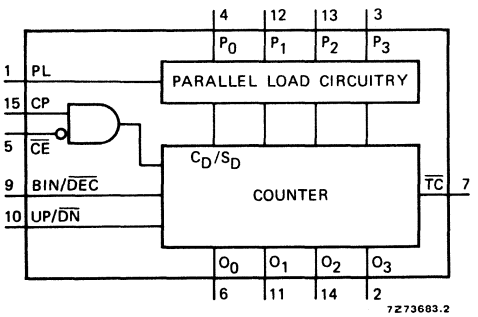
HEF4028B

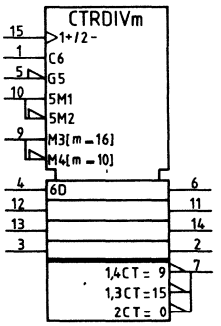




1-of-10 decoder.

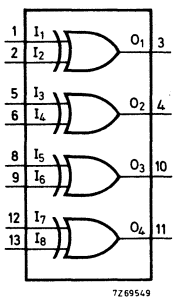
HEF4029B

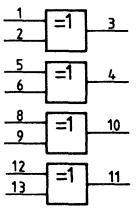




Synchronous up/down counter,
binary/decade counter.

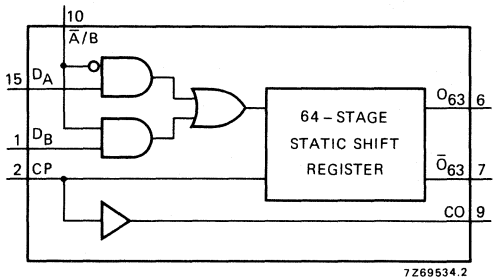
HEF4030B

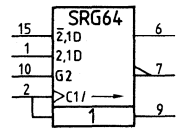




Quadruple EXCLUSIVE-OR gate.

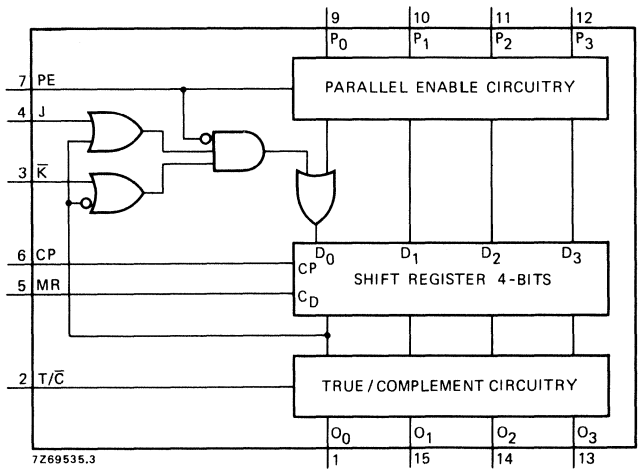
HEF4031B

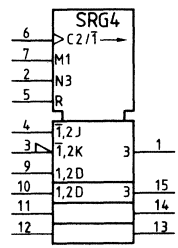




64-stage static shift register.

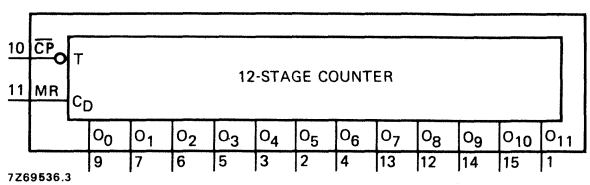
HEF4035B

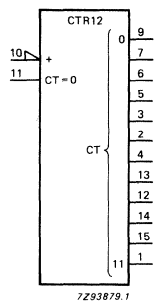




4-bit universal shift register.

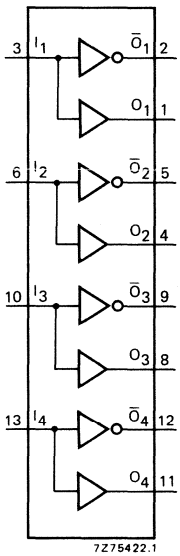
HEF4040B

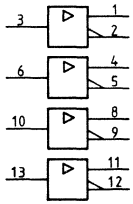




12-stage binary counter.

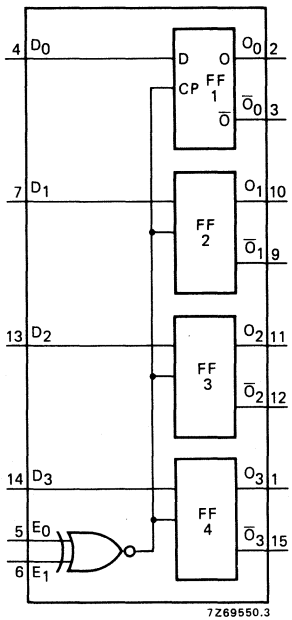
HEF4041B

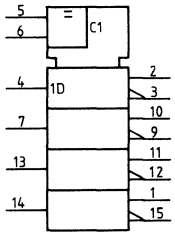




Quadruple true/complement buffer.

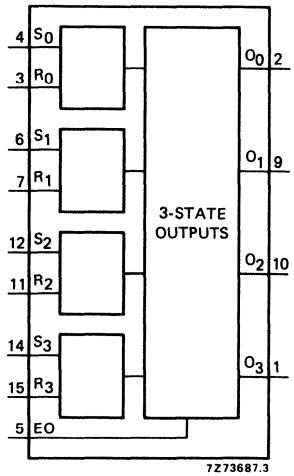
HEF4042B

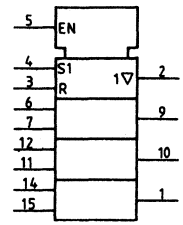




Quadruple D-latch.

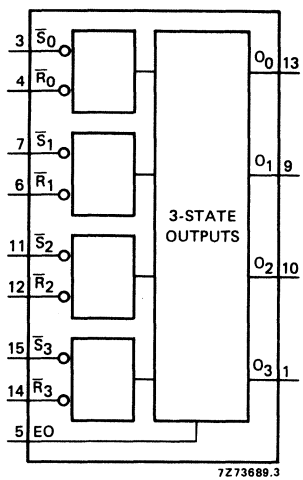
HEF4043B

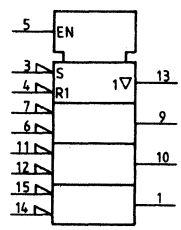




Quadruple R/S latch with 3-state outputs.

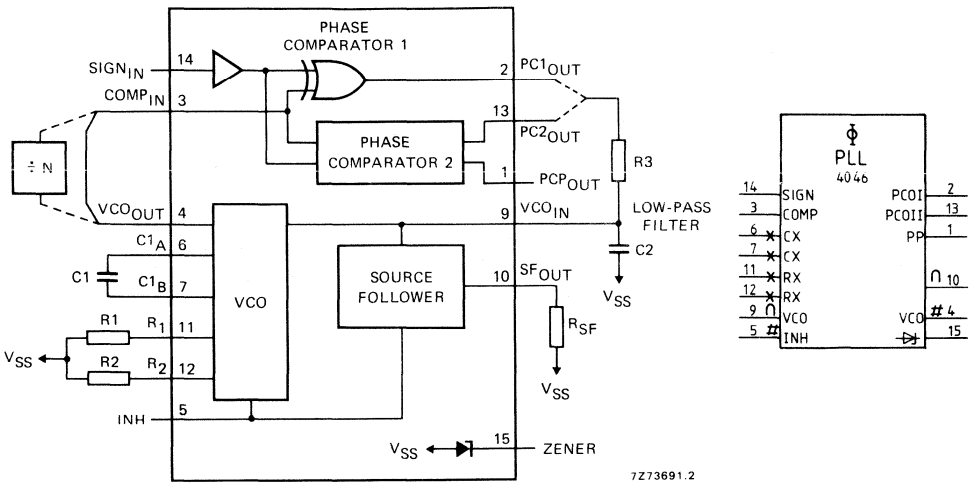
HEF4044B





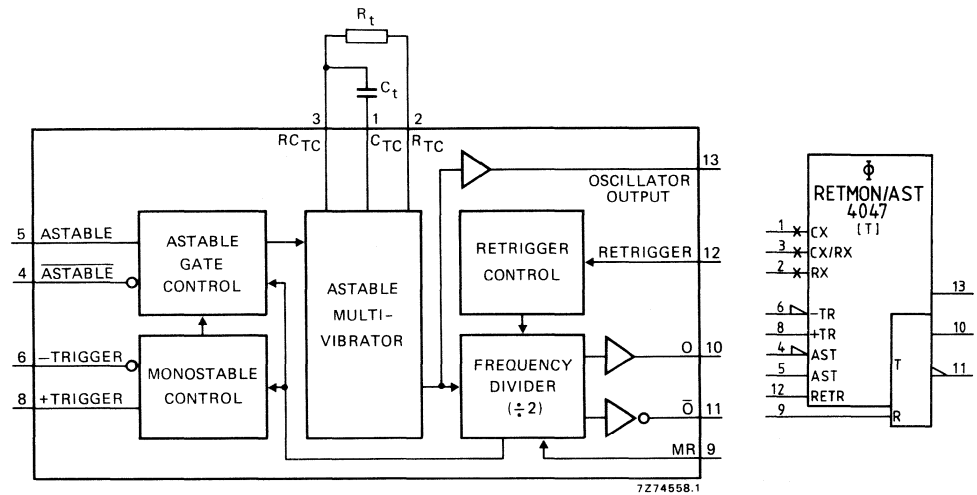
Quadruple R/S latch with 3-state outputs.

HEF4046B



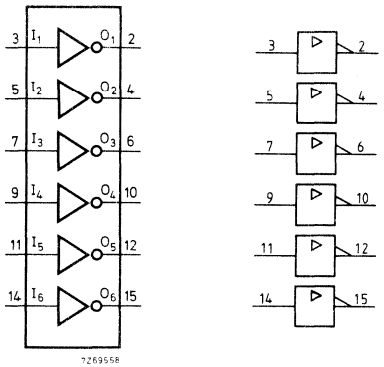
Phase-locked loop.

HEF4047B



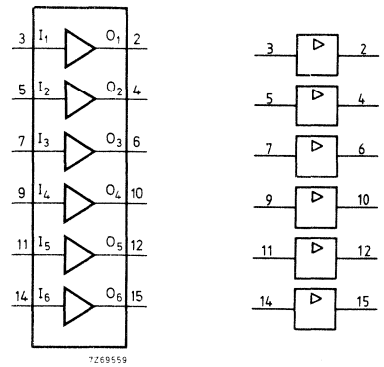
Monostable/astable multivibrator.

HEF4049B



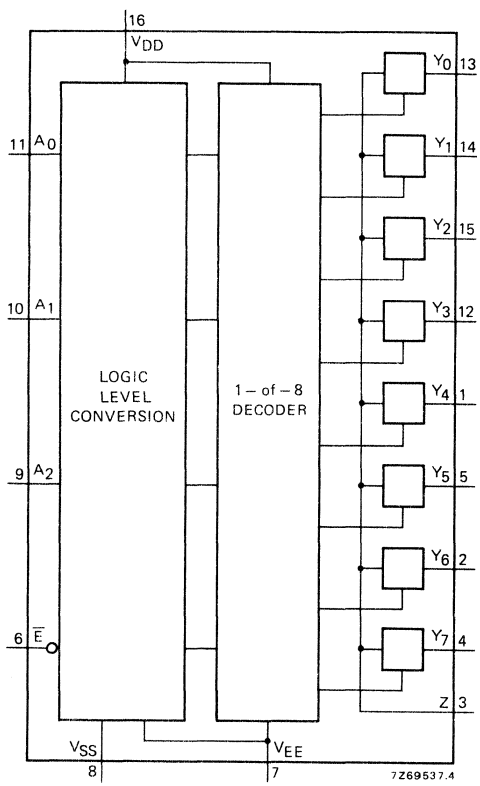
Hex inverting buffers.

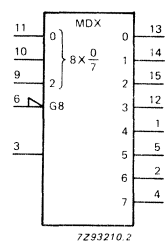
HEF4050B



Hex non-inverting buffers.

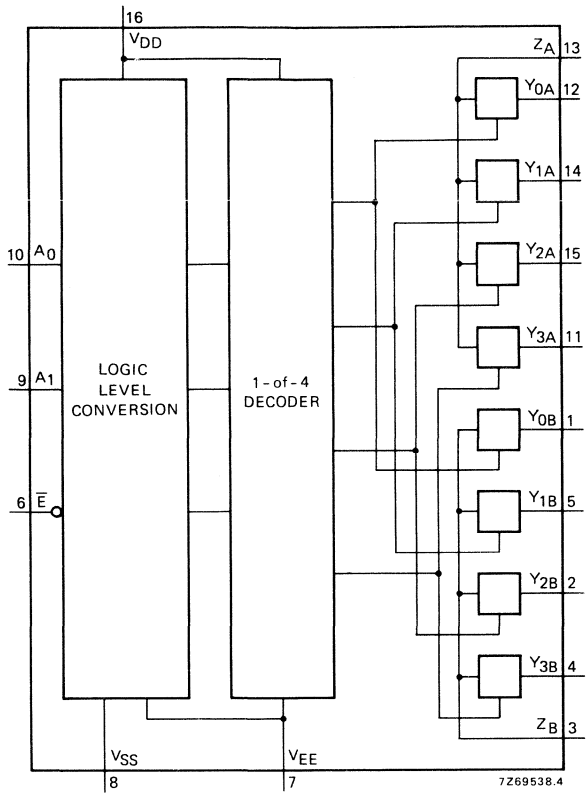
HEF4051B

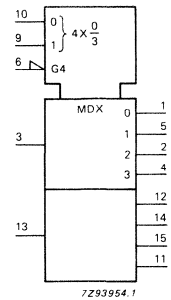




8-channel analogue multiplexer/demultiplexer.

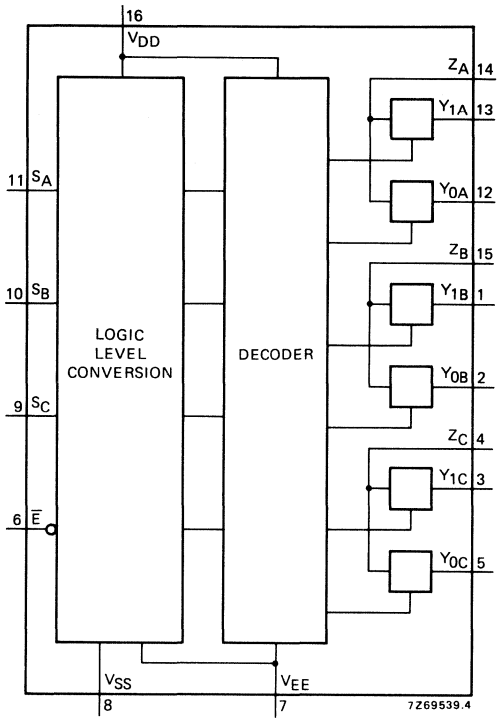
HEF4052B

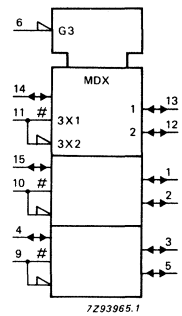




Dual 4-channel analogue multiplexer/demultiplexer.

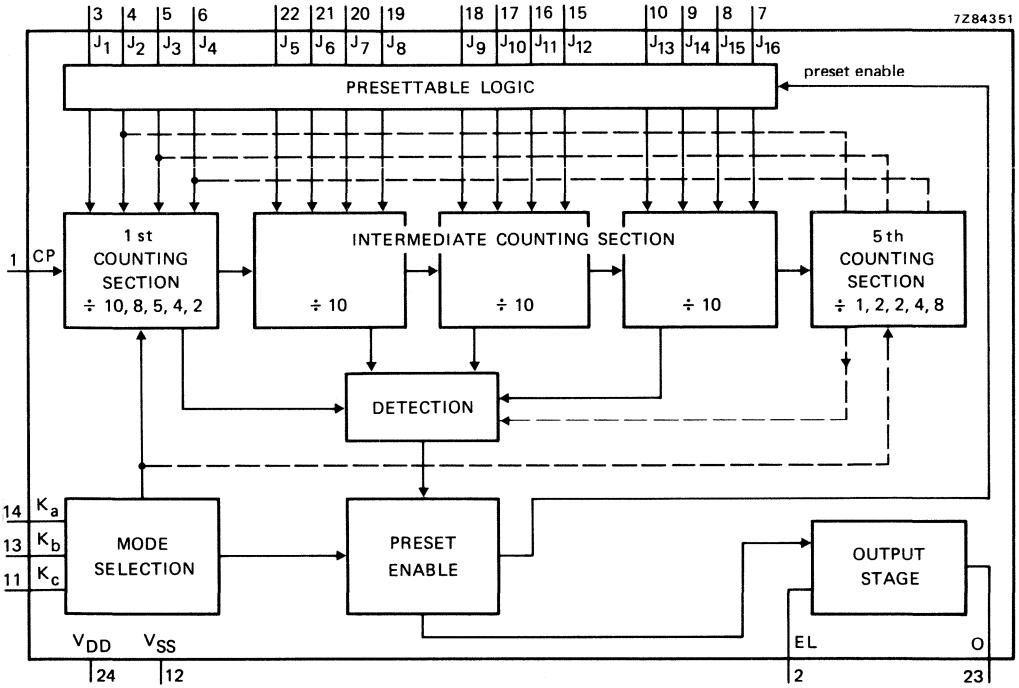
HEF4053B

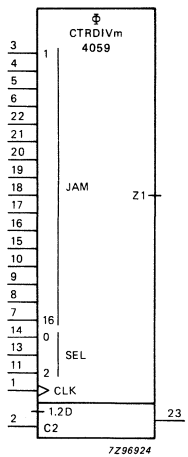




Triple 2-channel analogue multiplexer/demultiplexer.

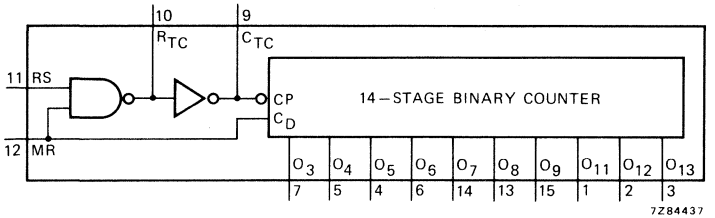
HEF4059B

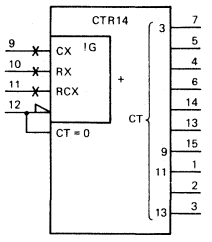


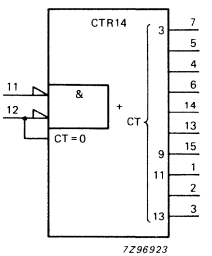


Programmable divide-by-n counter.

HEF4060B

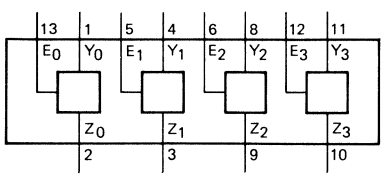


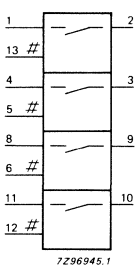


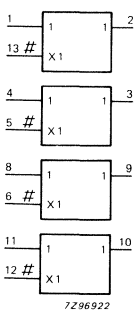


14-stage ripple-carry binary counter/divider and oscillator.

HEF4066B

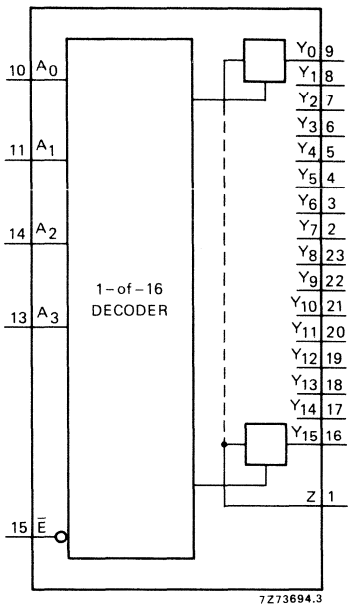


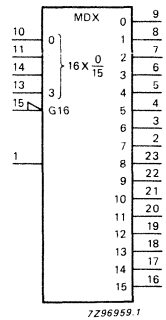




Quadruple bilateral switches.

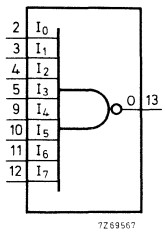
HEF4067B

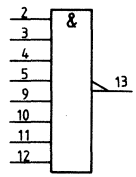




16-channel analogue multiplexer/demultiplexer.

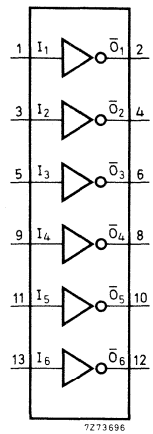
HEF4068B

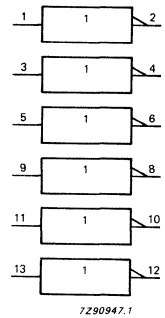




8-input NAND gate.

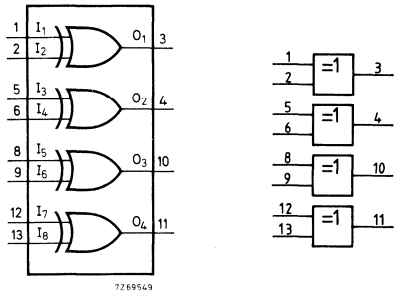
HEF4069UB





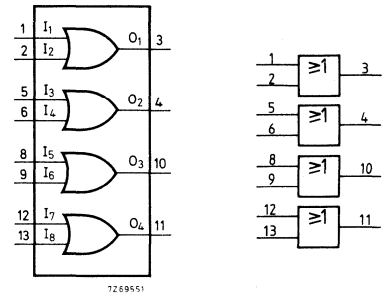
Hex inverter; unbuffered.

HEF4070B



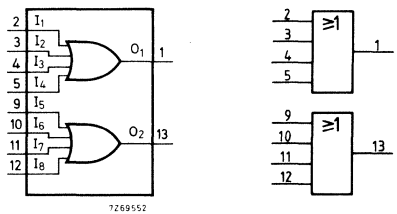
Quadruple EXCLUSIVE-OR gate.

HEF4071B



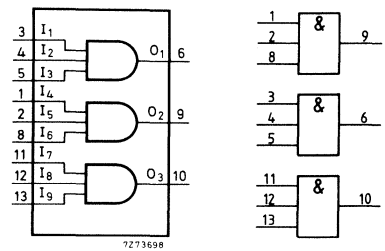
Quadruple 2-input OR gate.

HEF4072B



Dual 4-input OR gate.

HEF4073B

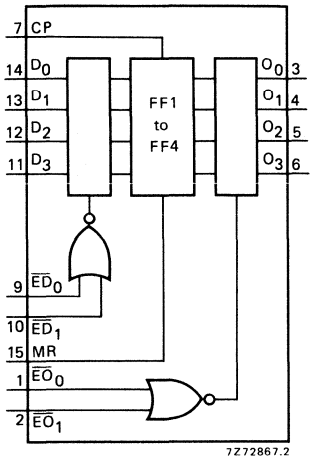


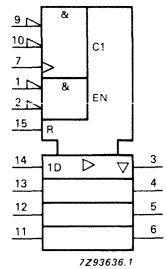
Triple 3-input AND gate.

HEF4075B

Triple 3-input OR gate.

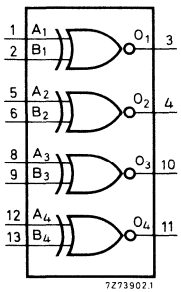
HEF4076B

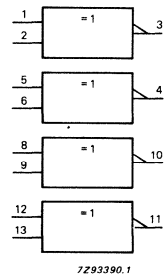




Quadruple D-type register with 3-state outputs.

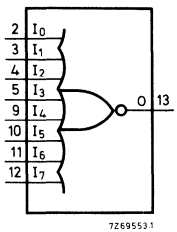
HEF4077B

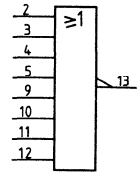




Quadruple EXCLUSIVE-NOR gate.

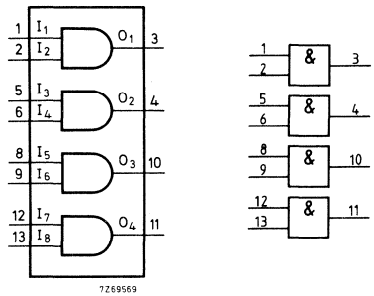
HEF4078B





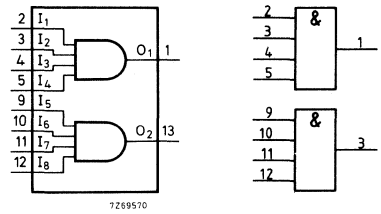
8-input NOR gate.

HEF4081B



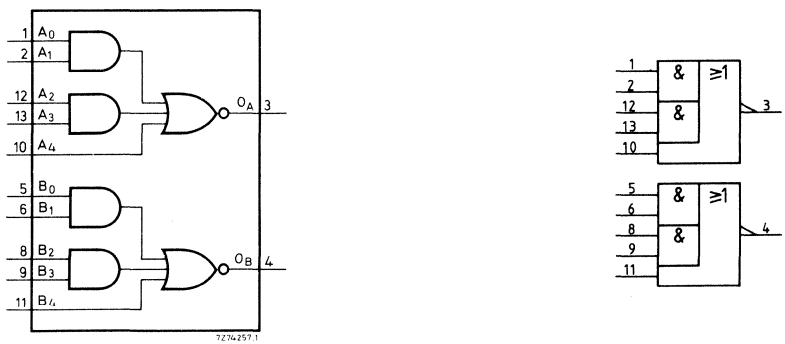
Quadruple 2-input AND gate.

HEF4082B



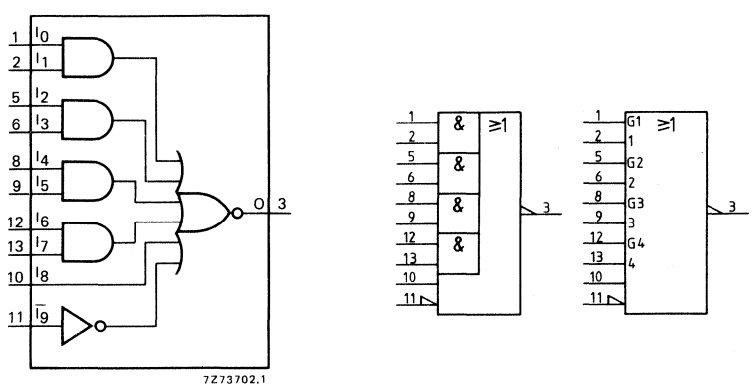
Dual 4-input AND gate.

HEF4085B



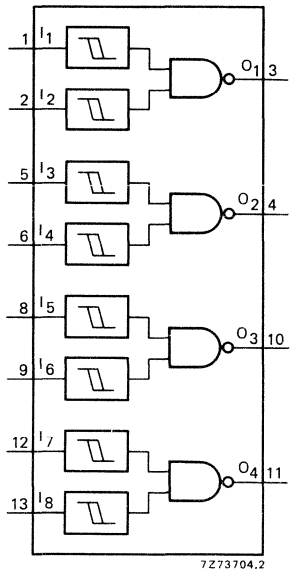
Dual 2-wide 2-input AND-OR-INVERT gate.

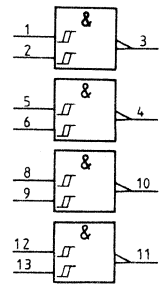
HEF4086B



4-wide 2-input AND-OR-INVERT gate.

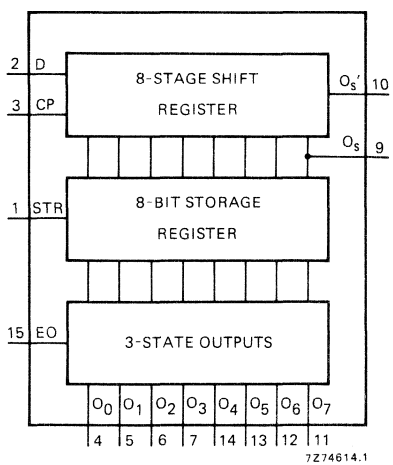
HEF4093B

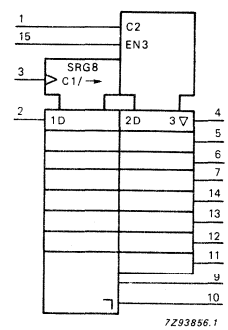




Quadruple 2-input NAND Schmitt trigger.

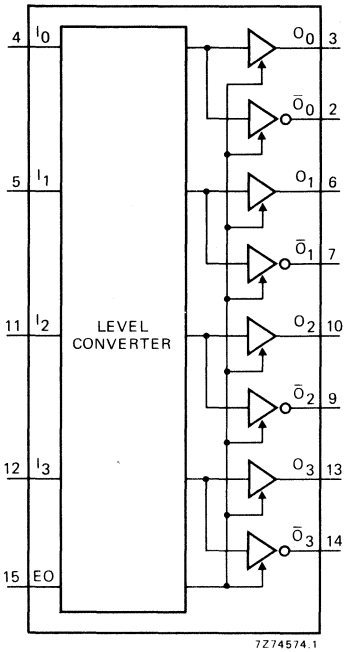
HEF4094B

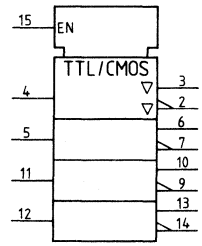




8-stage shift-and-store bus register.

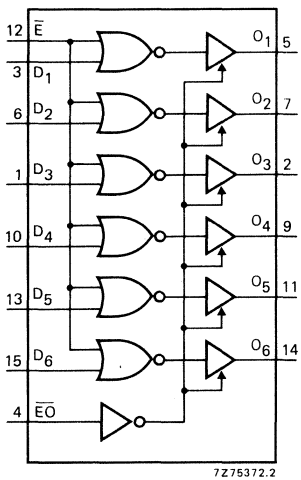
HEF4104B

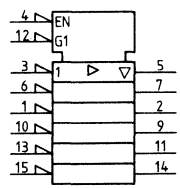


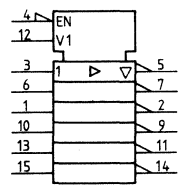


Quadruple low-to-high voltage translator with 3-state outputs.

HEF4502B

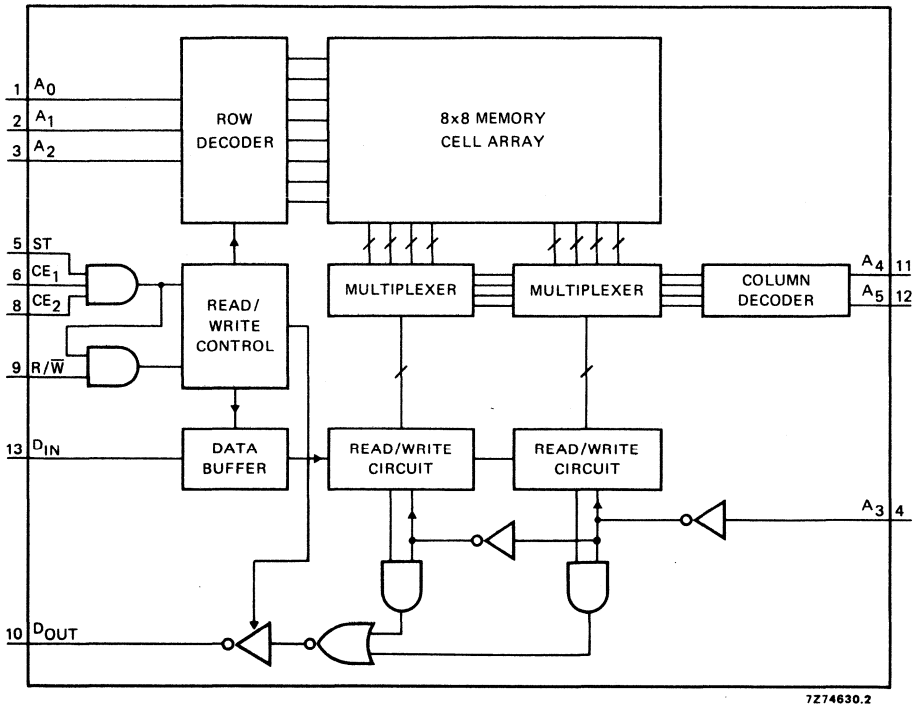


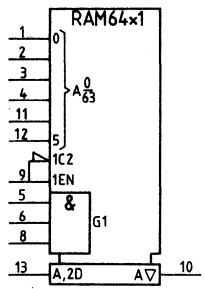




Strobed hex inverter/buffer.

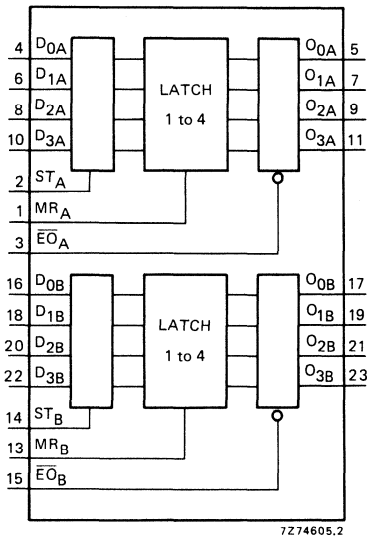
HEF4505B

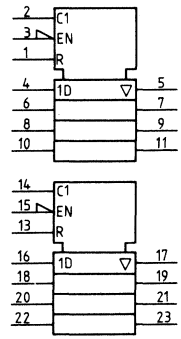




64-bit, 1-bit per word random access read/write memory.

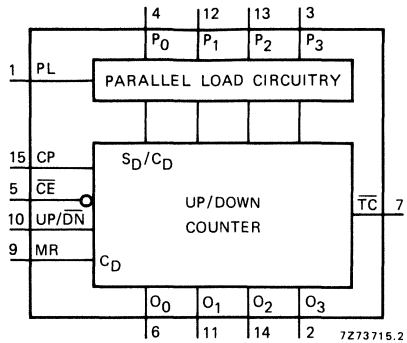
HEF4508B

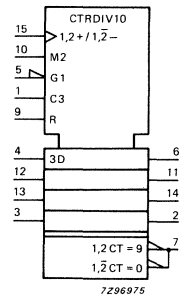




Dual 4-bit latch.

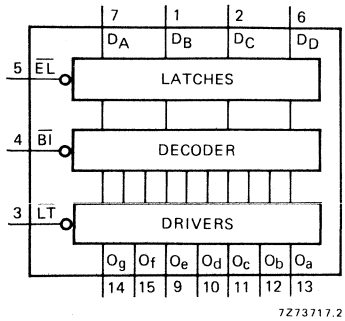
HEF4510B

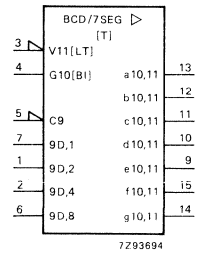




BCD up/down counter.

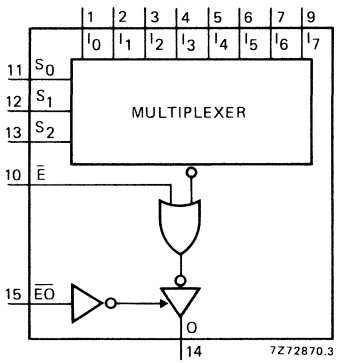
HEF4511B

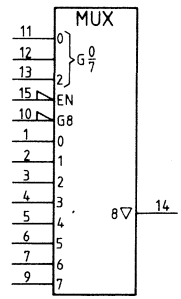




BCD to 7-segment latch/decoder/driver.

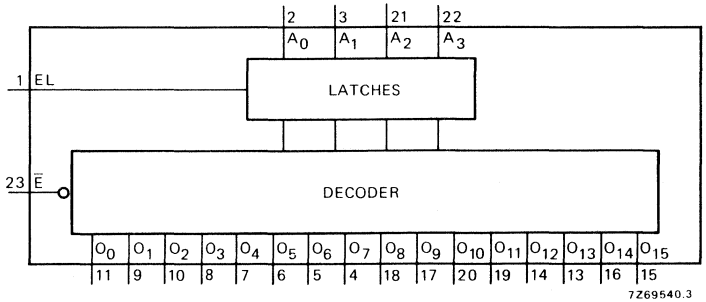
HEF4512B

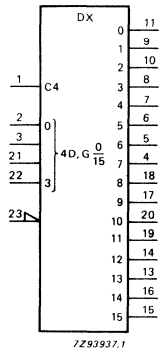


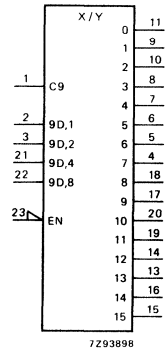


8-input multiplexer with 3-state output.

HEF4514B

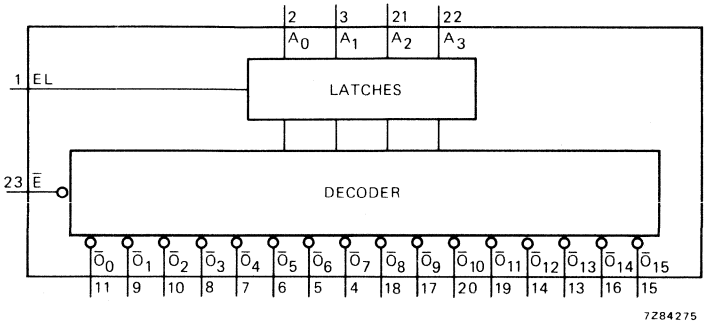


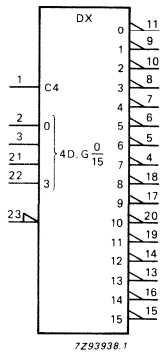


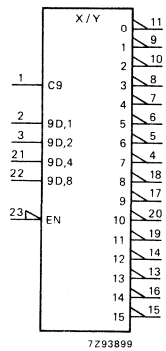


1-of-16 decoder/demultiplexer with input latches.

HEF4515B

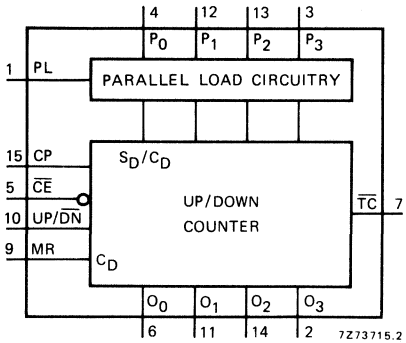


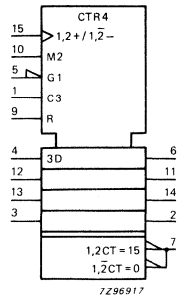




1-of-16 decoder/demultiplexer with input latches.

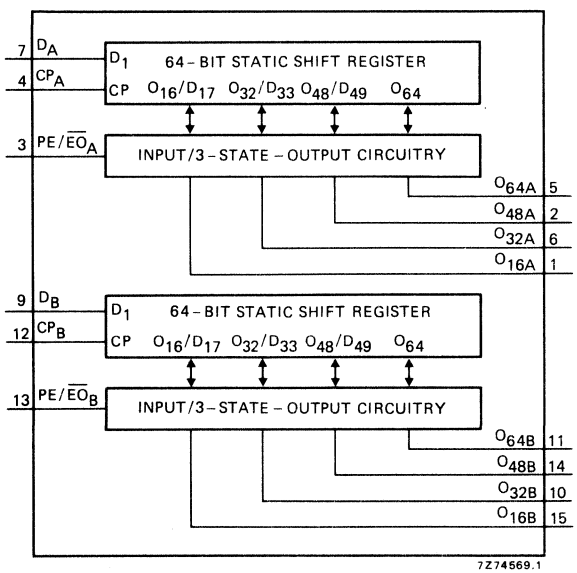
HEF4516B

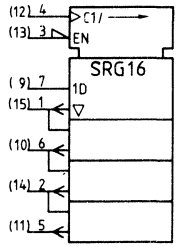


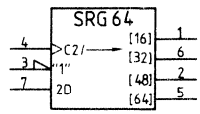


Binary up/down counter.

HEF4517B

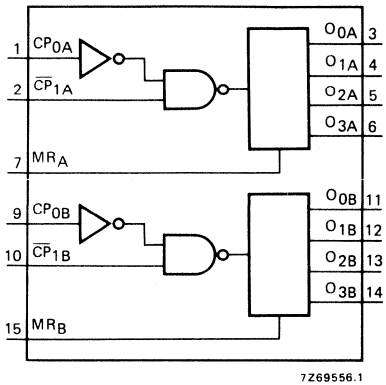


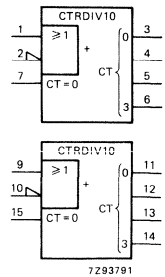




Dual 64-bit static shift register.

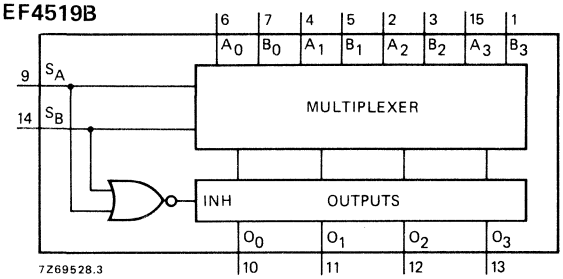
HEF4518B

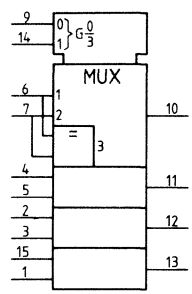




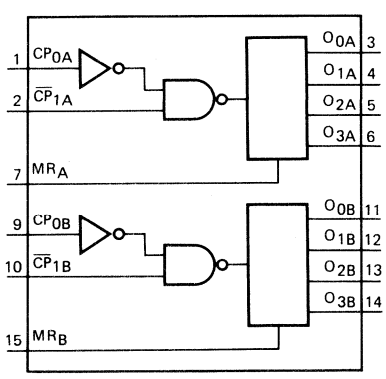
Dual BCD counter.

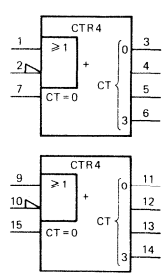
HEF4519B





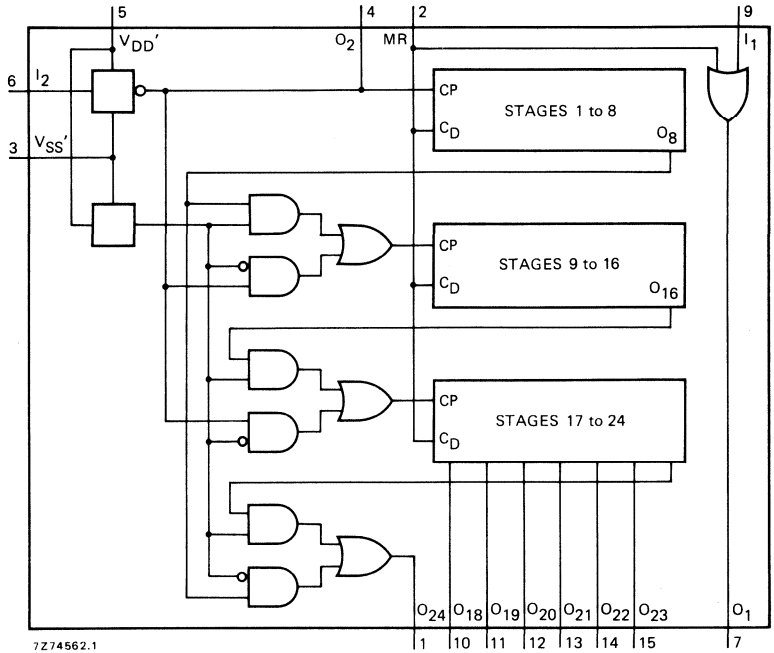
Quadruple 2-input multiplexer.

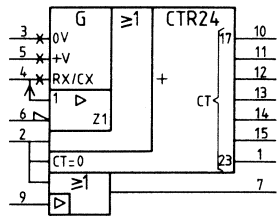




Dual binary counter.

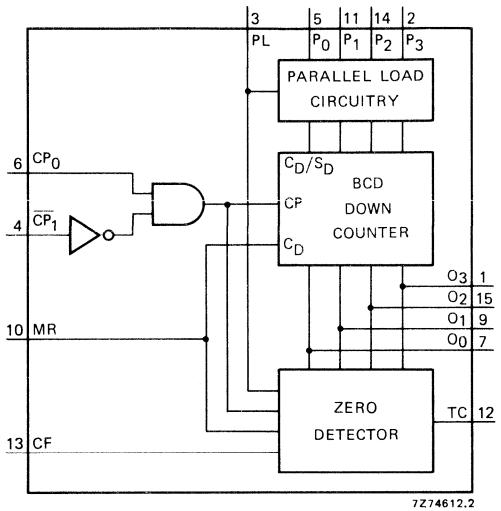
HEF4521B

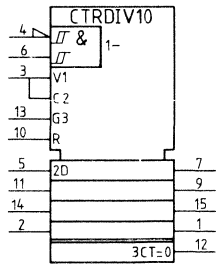




24-stage frequency divider.

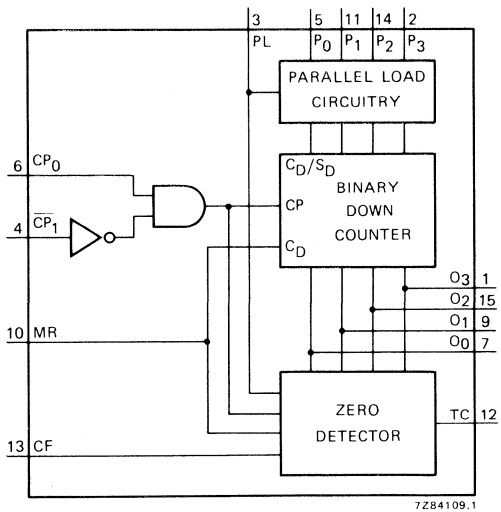
HEF4522B

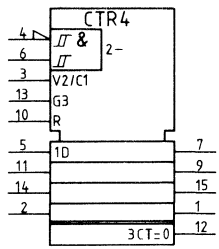




Programmable 4-bit BCD down counter.

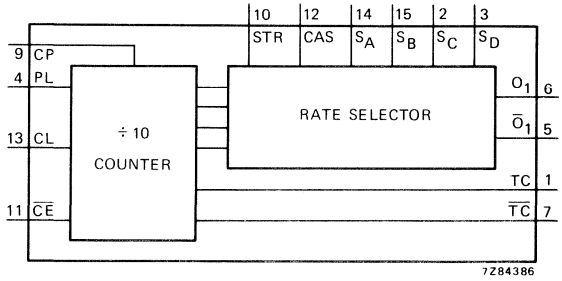
HEF4526B

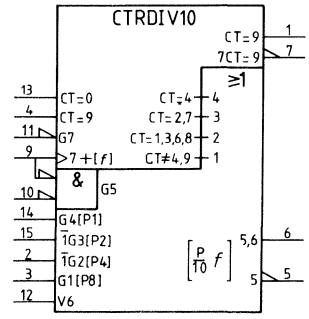




Programmable 4-bit binary down counter.

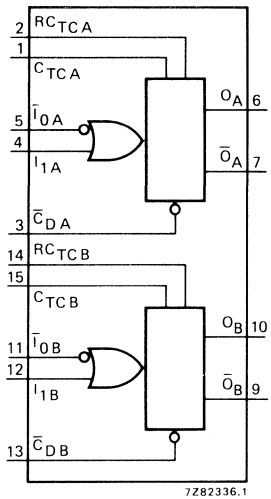
HEF4527B

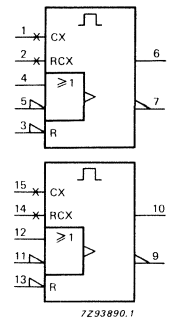




BCD rate multiplier.

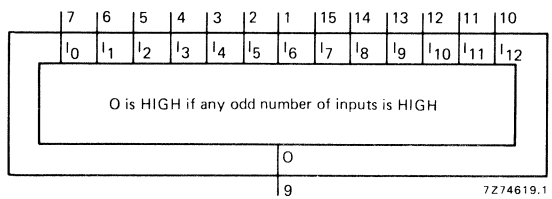
HEF4528B

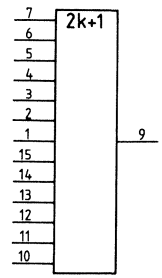




Dual monostable multivibrator.

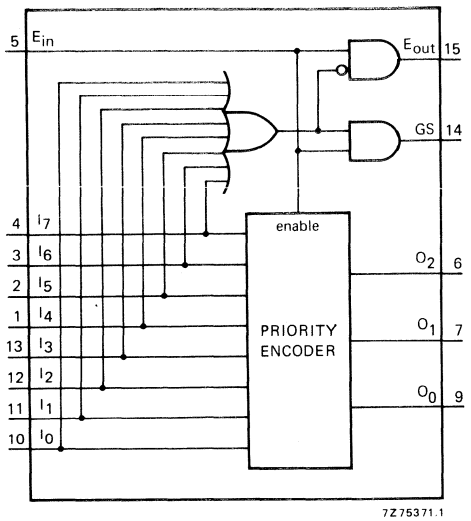
HEF4531B

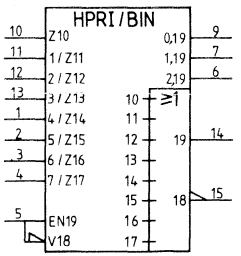




13-input parity checker/generator.

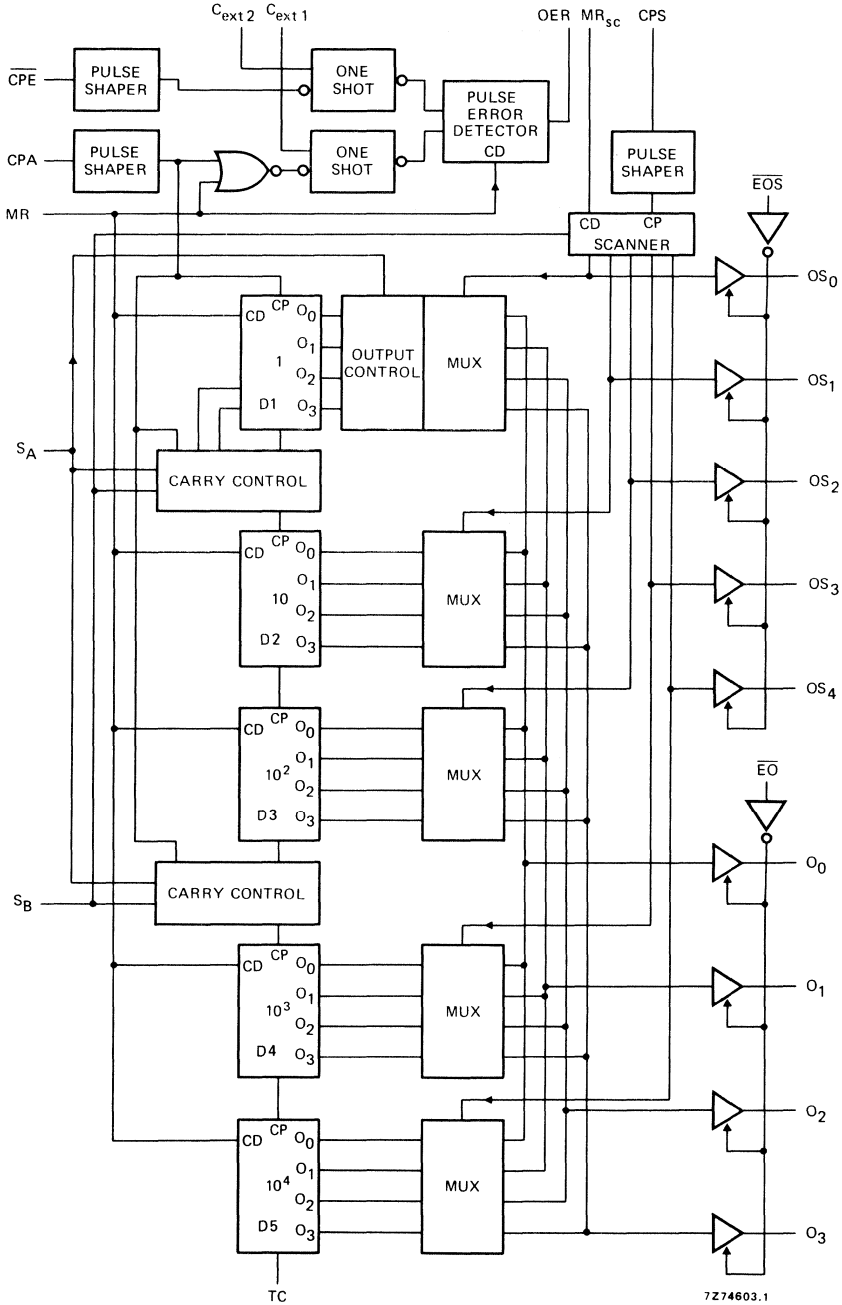
HEF4532B





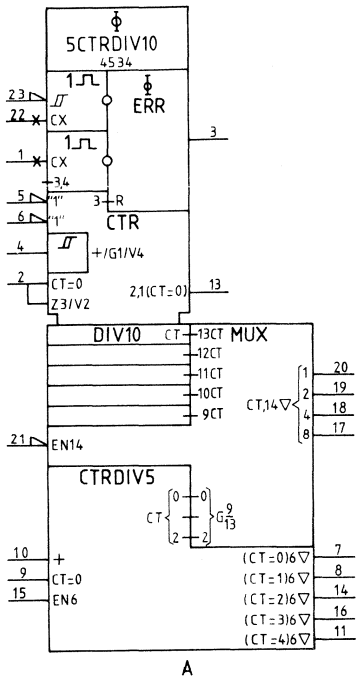
8-input priority encoder.

HEF4534B



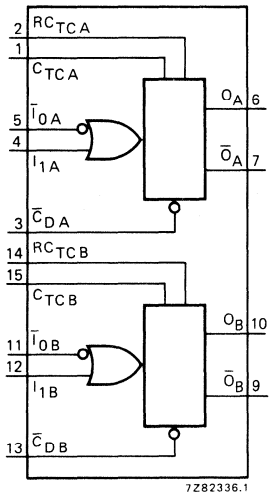
Real time 5-decade counter.

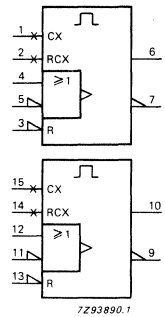
HEF4534B



Real time 5-decade counter.

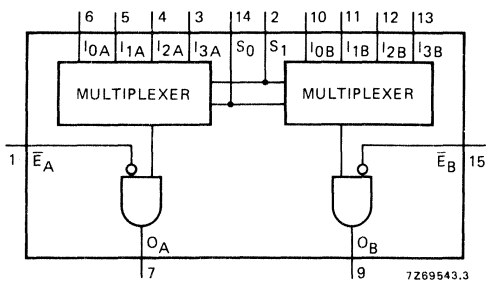
HEF4538B

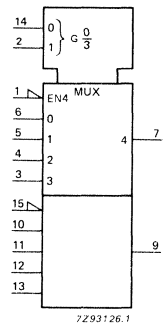




Dual precision monostable multivibrator.

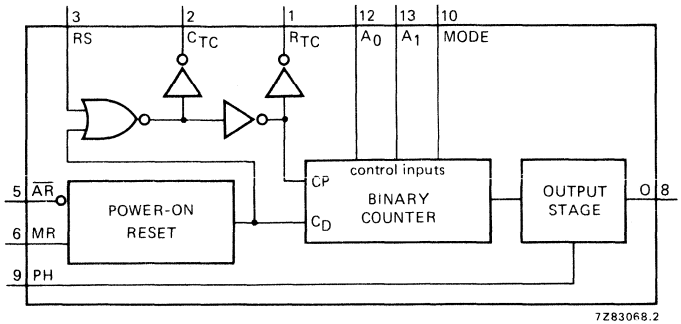
HEF4539B

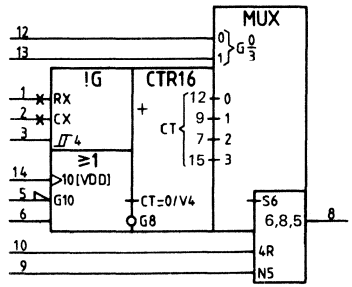




Dual 4-input multiplexer.

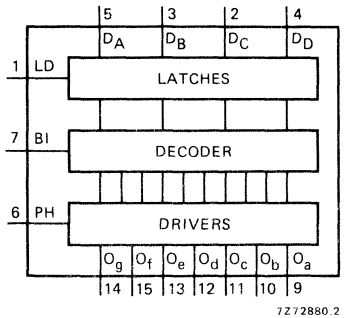
HEF4541B

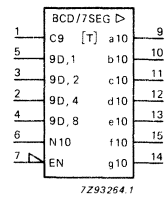




Programmable timer.

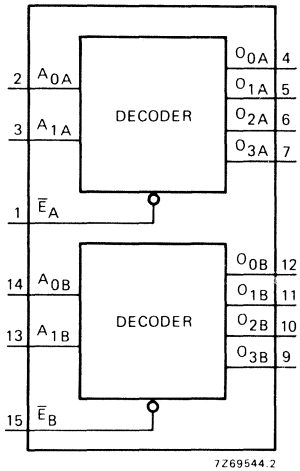
HEF4543B

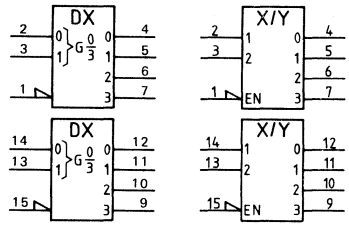




BCD to 7-segment latch/decoder/driver.

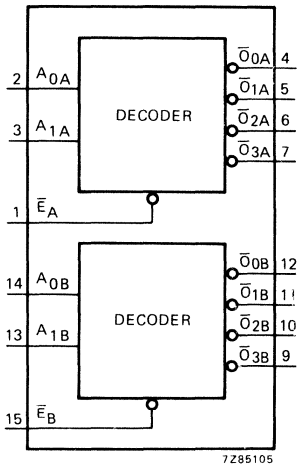
HEF4555B

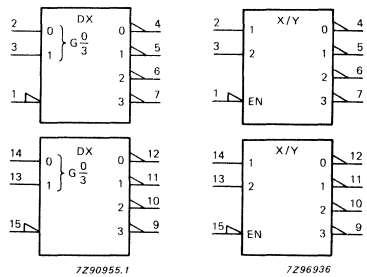




Dual 1-of-4 decoder/demultiplexer.

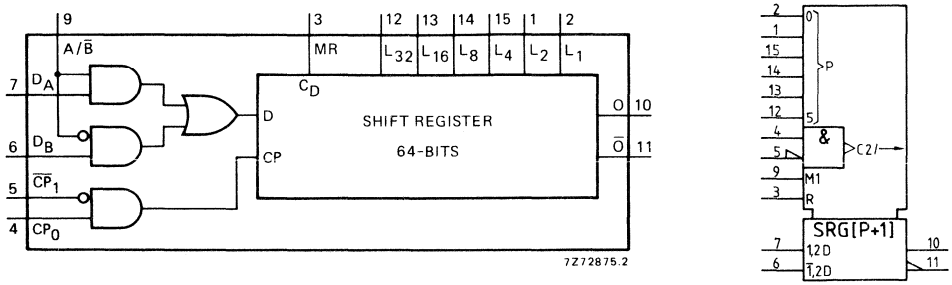
HEF4556B





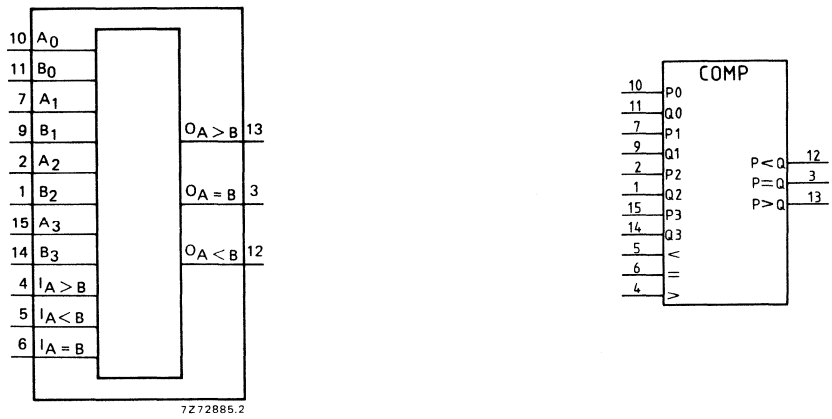
Dual 1-of-4 decoder/demultiplexer.

HEF4557B



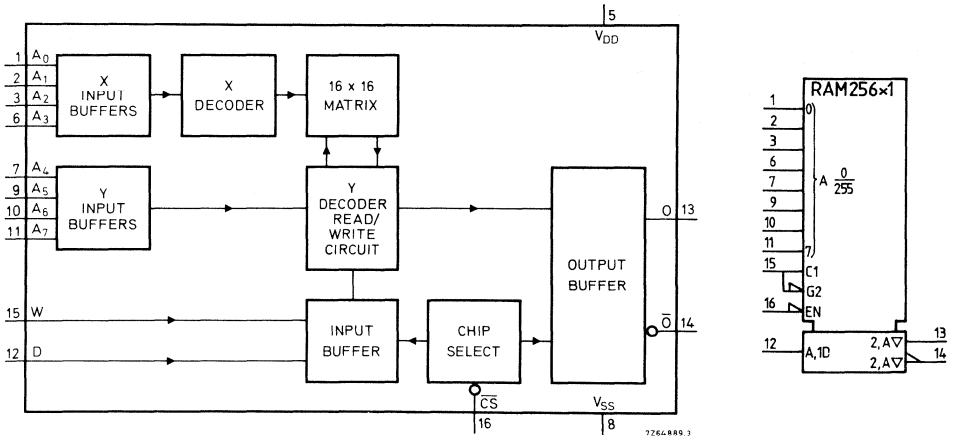
1-to-16 bit variable length shift register.

HEF4585B



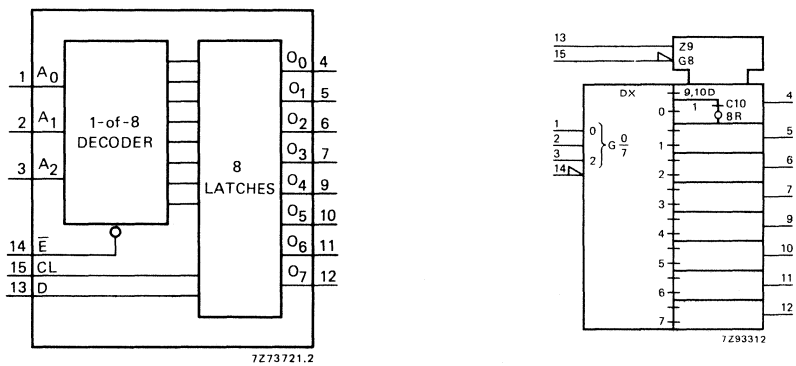
4-bit magnitude comparator.

HEF4720B; V



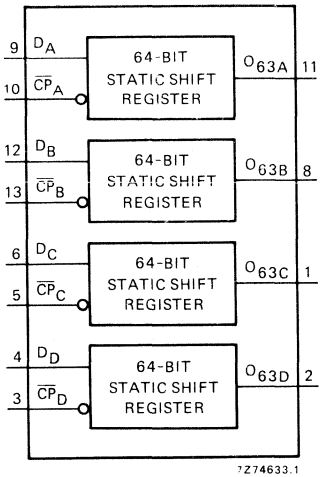
256-bit, 1-bit per word RAM.

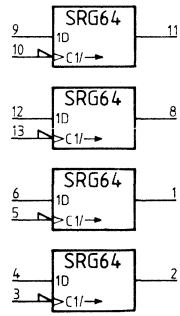
HEF4724B



8-bit addressable latch.

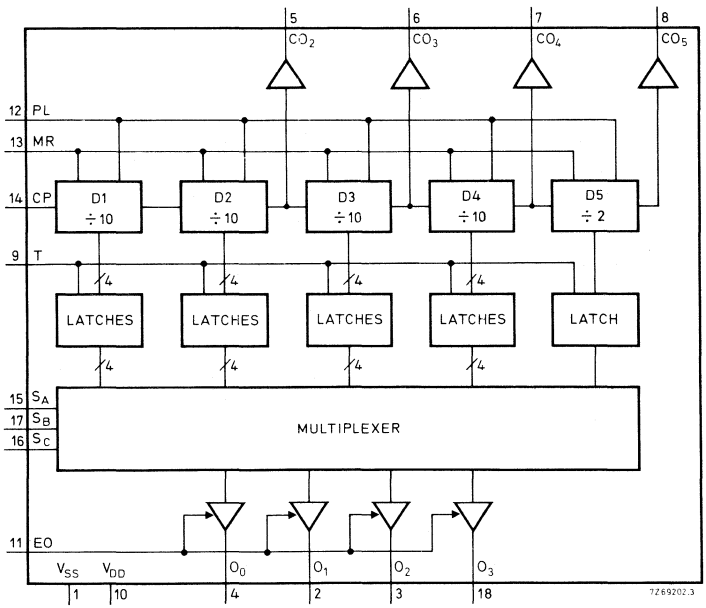
HEF4731B; V

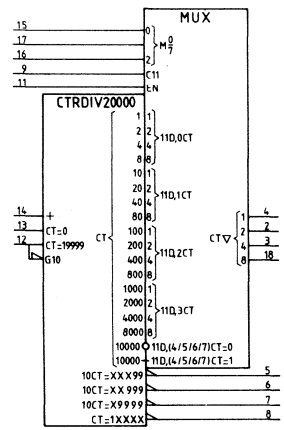




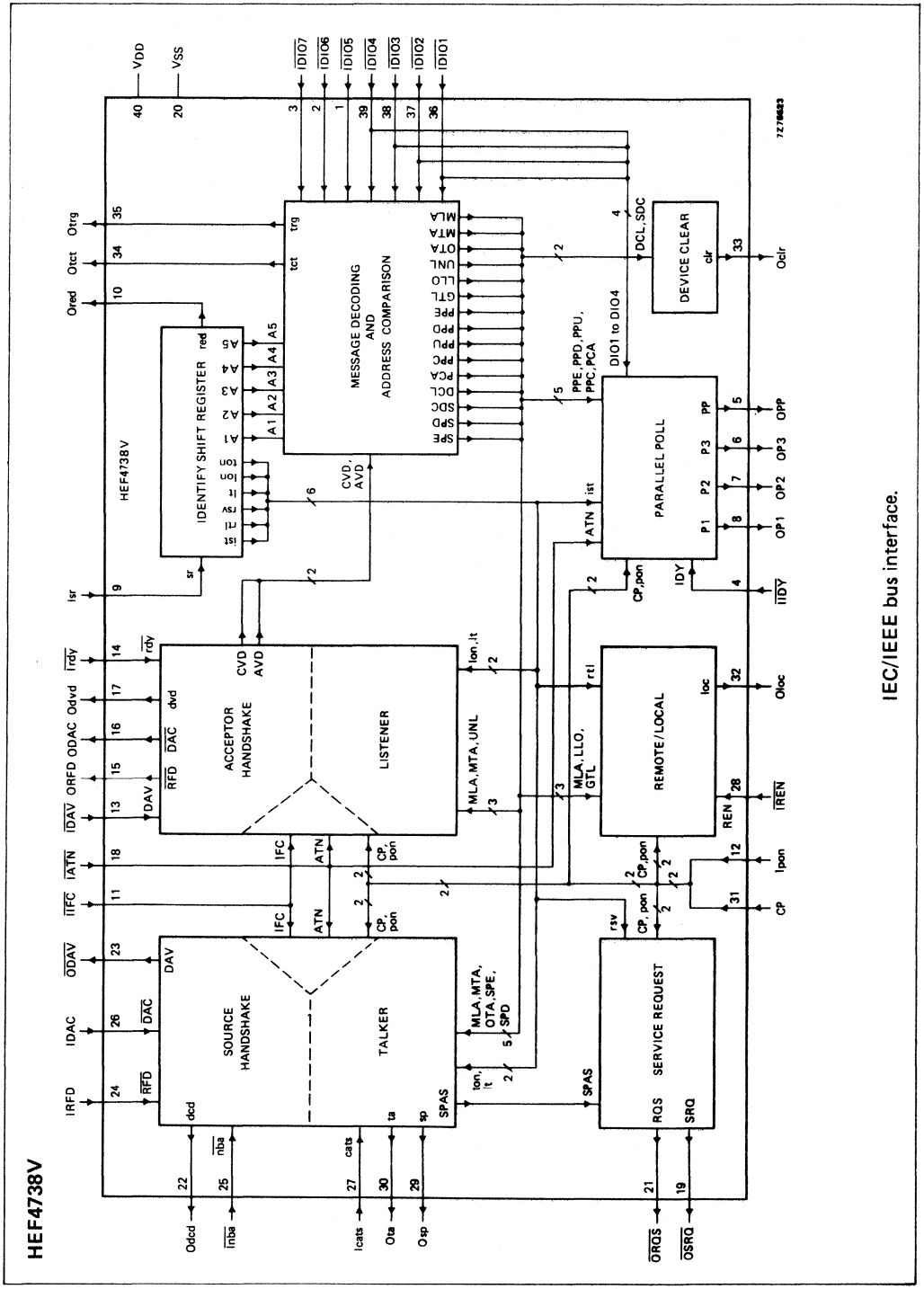
Quadruple 64-bit static shift register.

HEF4737B; V

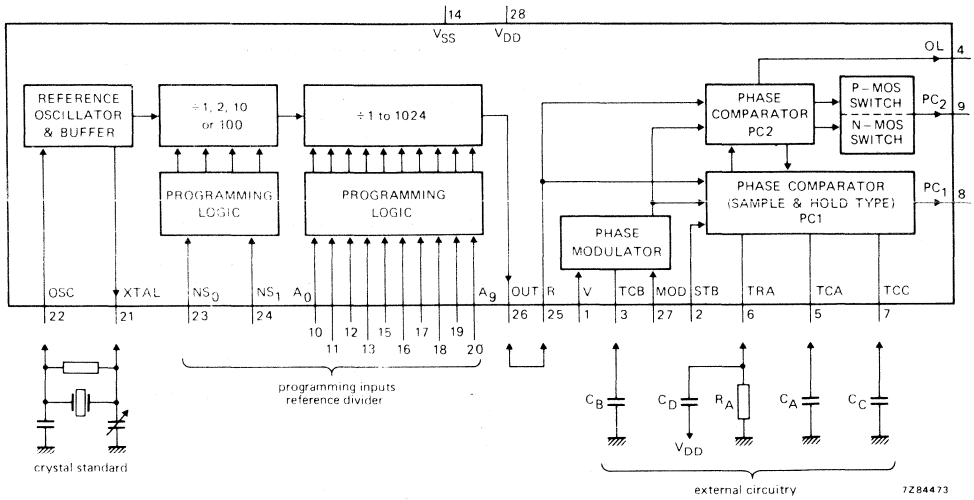


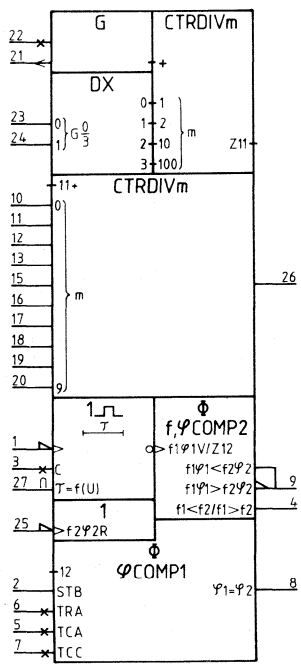


Quadruple static decade counter.


HEF4738V
IEC/IEEE bus interface.
HEF4738V
IDENTIFY SHIFT REGISTER
MESSAGE DECODING AND ADDRESS COMPARISON
DEVICE CLEAR
PARALLEL POLL
ACCEPTOR HANDSHAKE
LISTENER
REMOTE/LOCAL
SOURCE HANDSHAKE
TALKER
SERVICE REQUEST
VDD
VSS
IDIO7
IDIO6
IDIO5
IDIO4
IDIO3
IDIO2
IDIO1
DIO1 to DIO4
DCL, SDC
PPE, PPD, PPU, PPC, PCA
CVD, AVD
MLA, MTA, UNL
MLA, LLO, GTL
MLA, MTA, OTA, SPE, SPD
SPAS
RQS
SRQ
REN
IFC
ATN
DAV
RFD
DAC
EOI
CP, pon
rsv
ton, lt

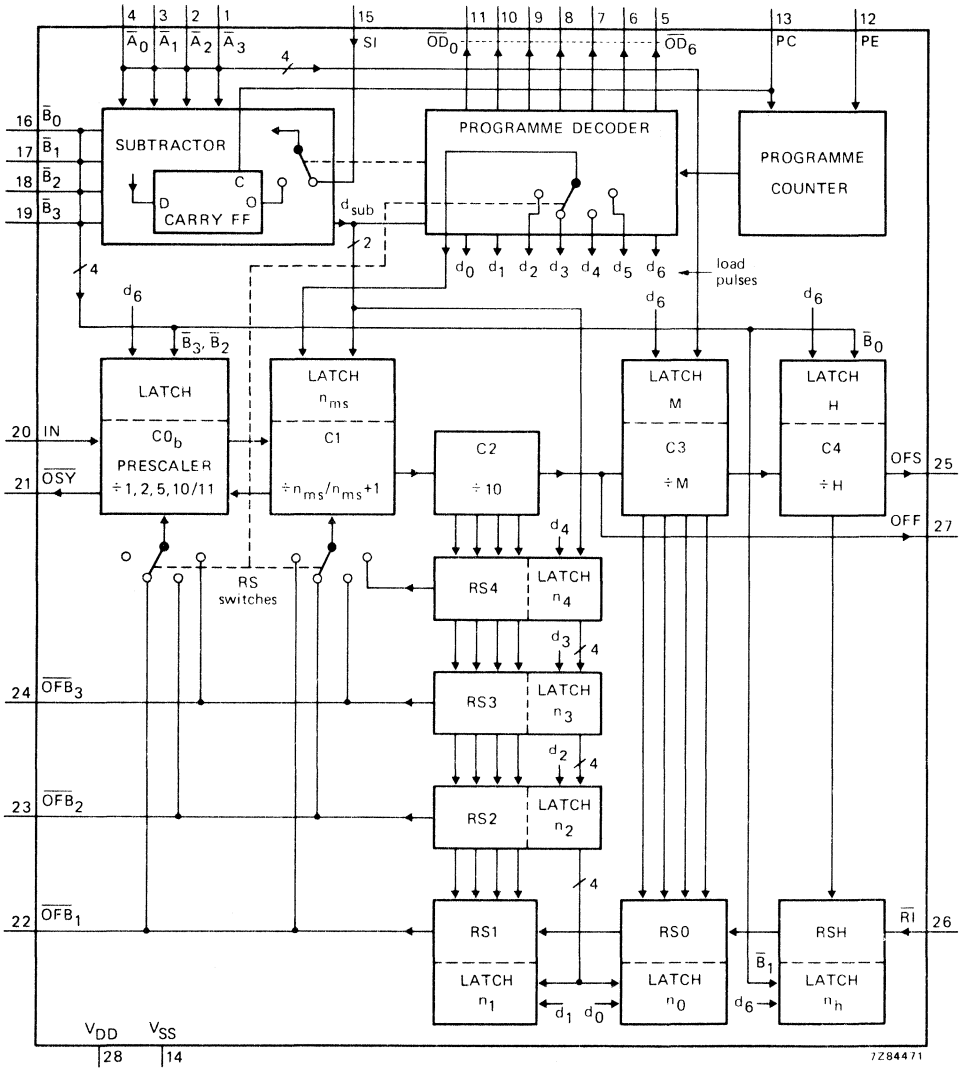
HEF4750V





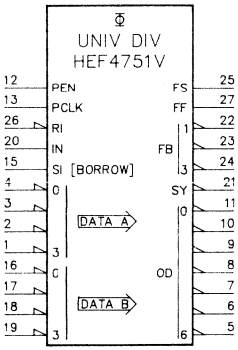
Frequency synthesizer.

HEF4751V



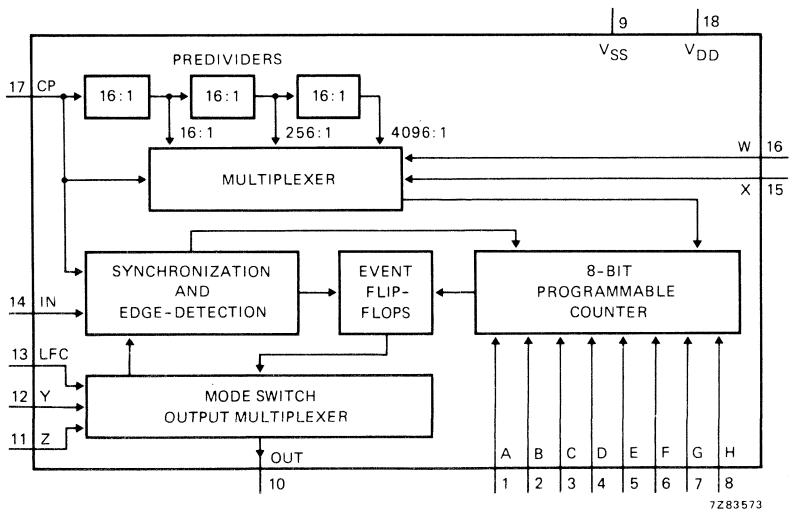
Universal divider.

HEF4751V



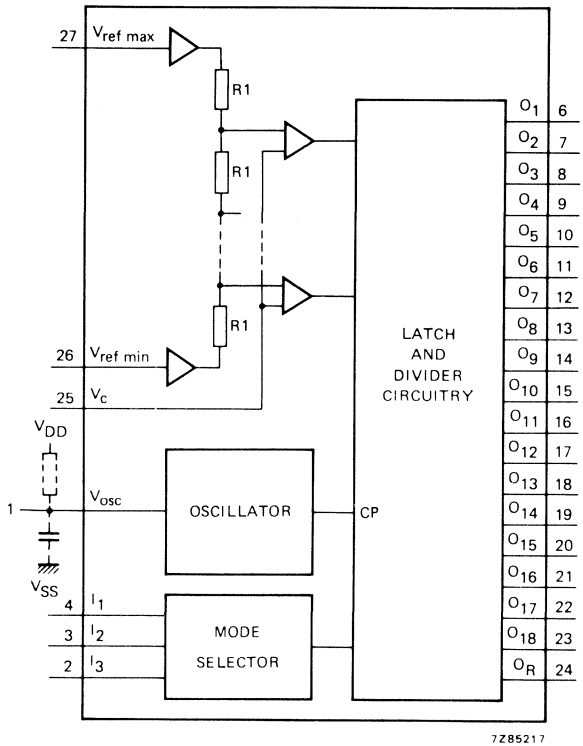
Universal divider.

HEF4753B



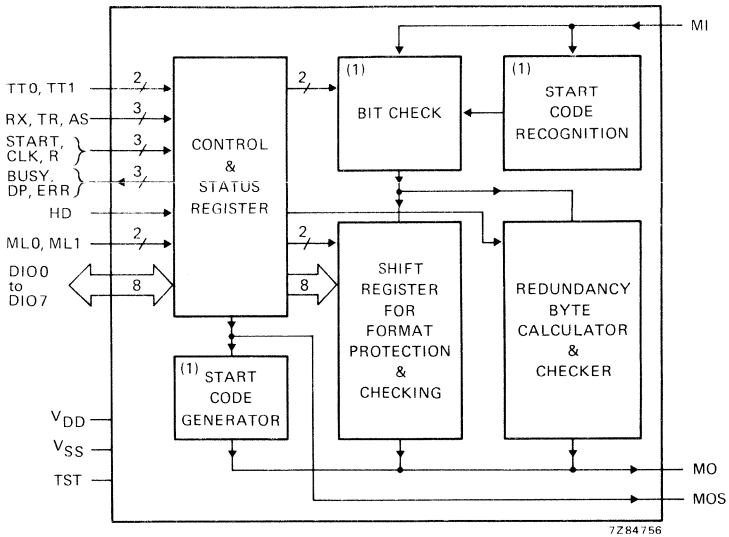
Universal timer module.

HEF4754V



18-element bargraph LCD driver.

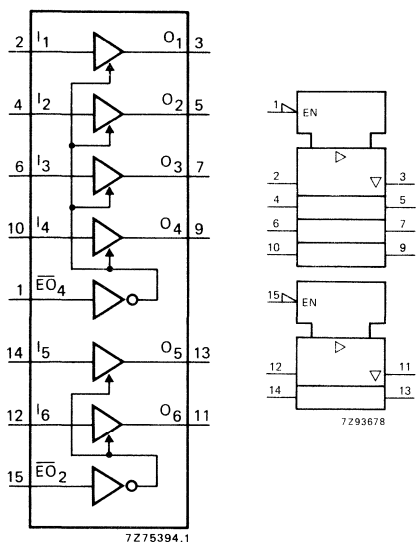
HEF4755V



(1) Only used in the asynchronous mode.

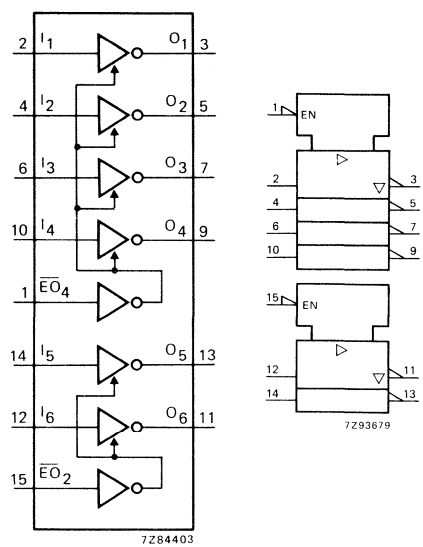
Transceiver for serial data communication.

HEF40097B



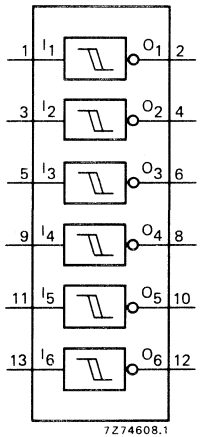
3-state hex non-inverting buffer.

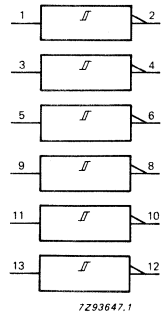
HEF40098B



3-state hex inverting buffer.

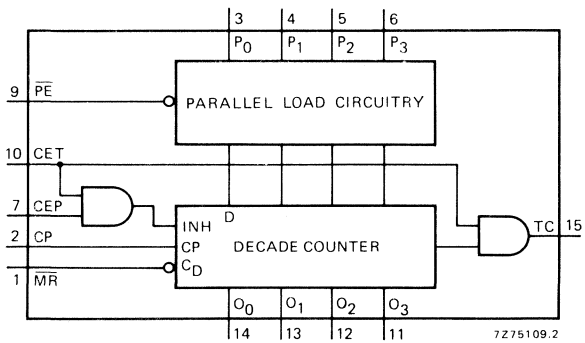
HEF40106B

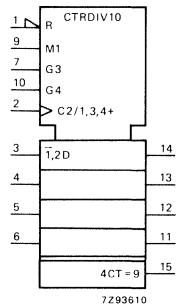




Hex Schmitt trigger.

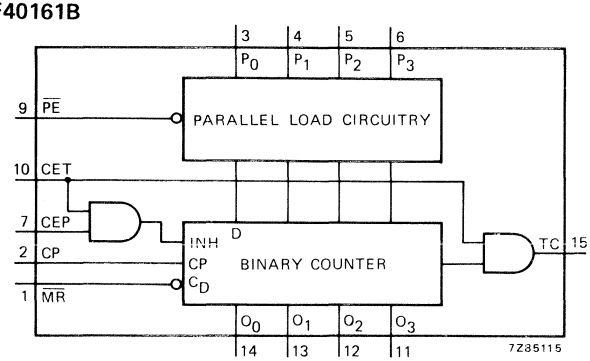
HEF40160B

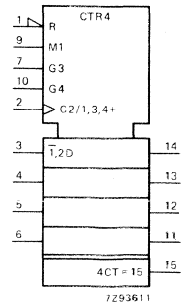




4-bit synchronous decade counter
with asynchronous reset.

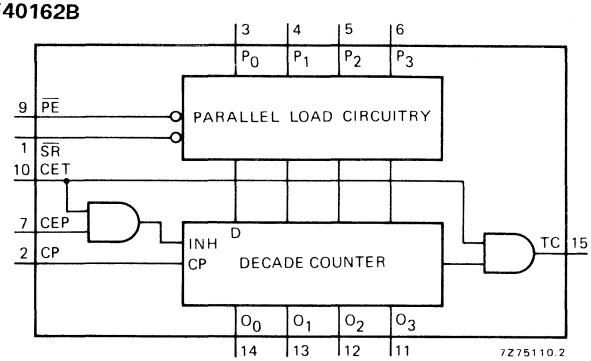
HEF40161B

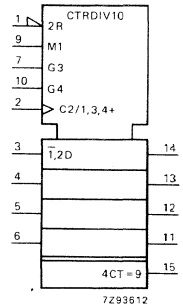




4-bit synchronous binary counter with asynchronous reset.

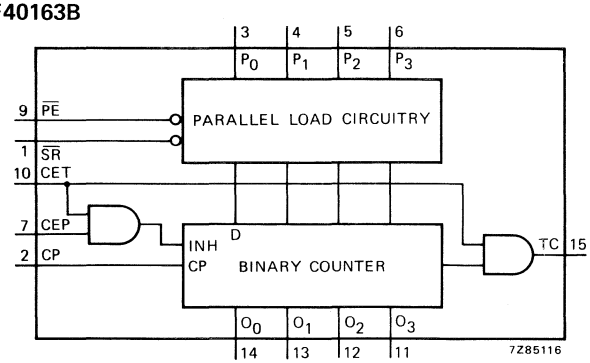
HEF40162B

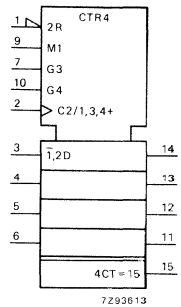




4-bit synchronous decade counter with synchronous reset.

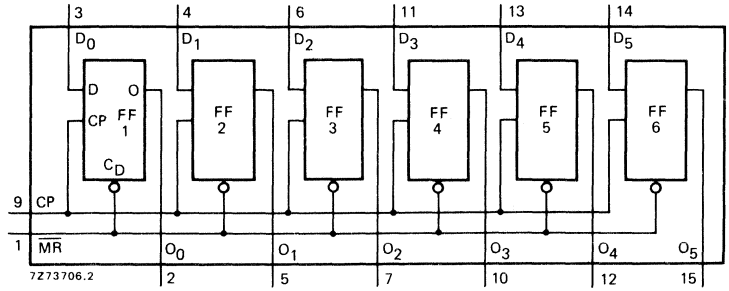
HEF40163B

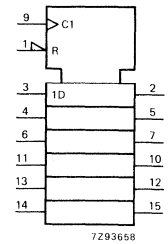




4-bit synchronous binary counter with synchronous reset.

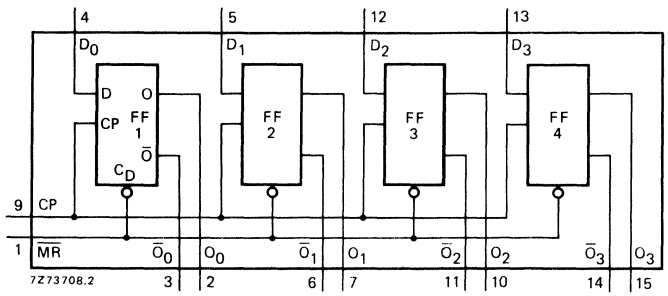
HEF40174B

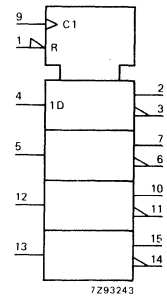




Hex D-type flip-flop.

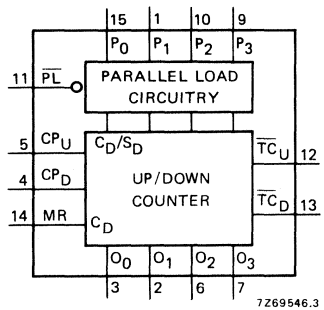
HEF40175B

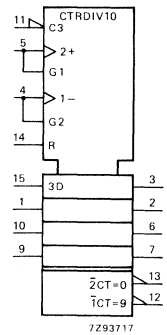




Quadruple D-type flip-flop.

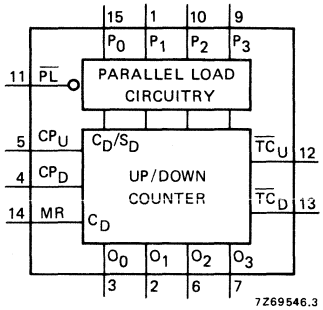
HEF40192B

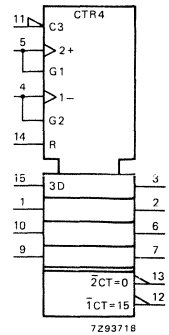




4-bit up/down decade counter.

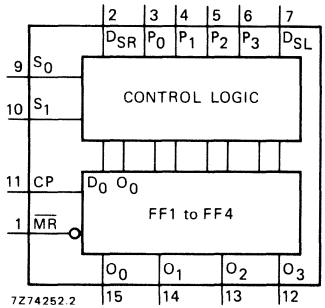
HEF40193B

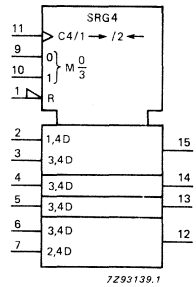




4-bit up/down binary counter.

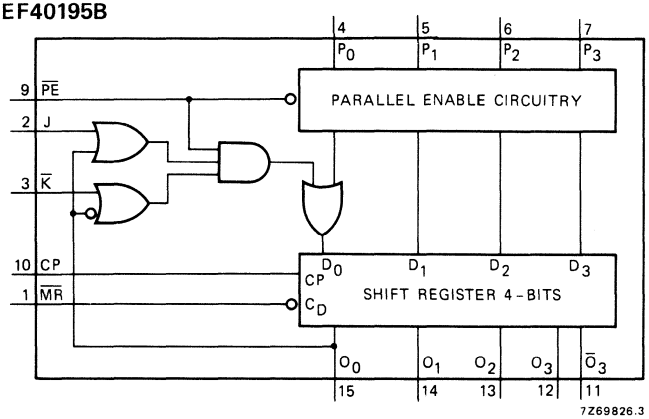
HEF40194B

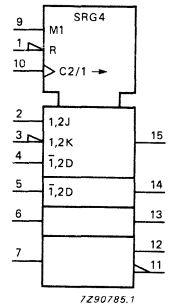




4-bit bidirectional universal shift register.

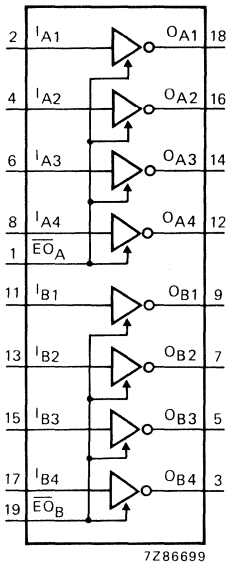
HEF40195B

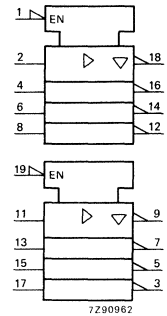




4-bit universal shift register.

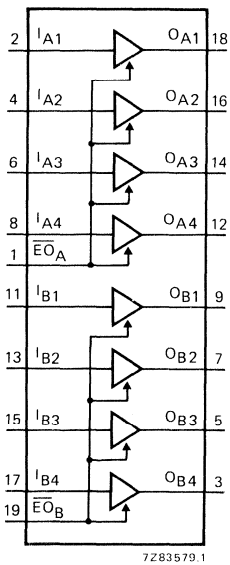
HEF40240B

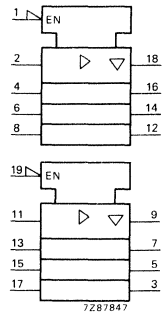




Octal buffers with 3-state outputs.

HEF40244B





Octal buffers with 3-state outputs.

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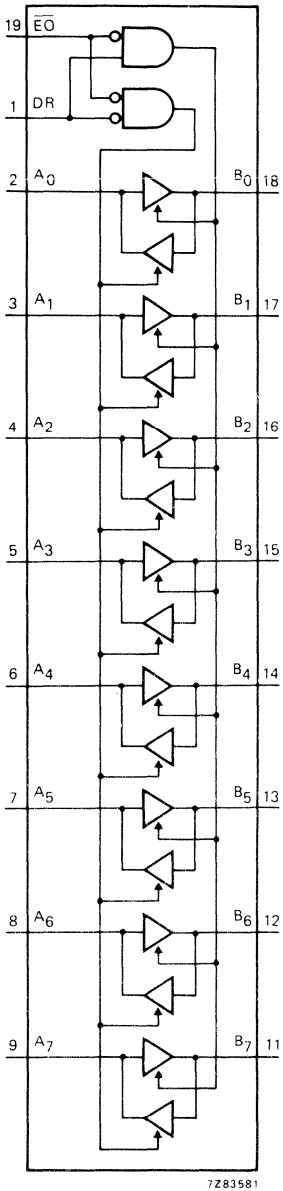
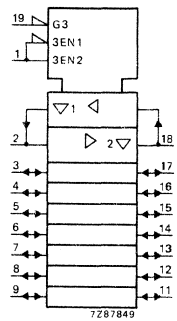
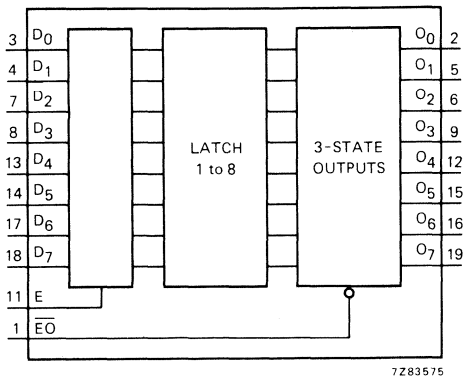
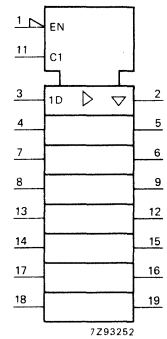




Octal bus transceiver with
3-state outputs.

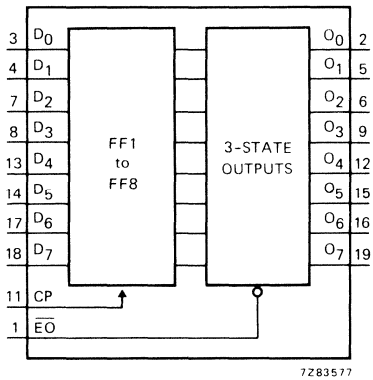
HEF40373B

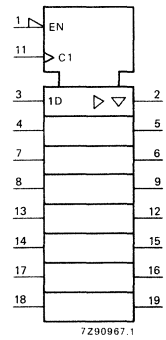




Octal transparent latch with 3-state outputs.

HEF40374B





Octal D-type flip-flop with 3-state outputs.

IEC SYMBOLOGY

Summary of IEC symbology

Rules for simplification of symbols

Example of application-dependency of symbols

SUMMARY OF IEC SYMBOLOGY

INTRODUCTION

The logic symbology used in the HCMOS published data follows the system developed by the International Electrotechnical Commission (IEC). The representation is very effective in that it shows the exact relationship between every input and output of digital circuits without having to detail internal logic. Basic logic functions are represented by symbols; in the symbols for more complex functions, use is made of 'dependency notation' that specified interrelationships of the digital inputs/outputs.

This summary describes the various elements used in symbol construction and the rules and definitions that apply.

SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying-symbols (Fig. 1). The purpose of a general qualifying-symbol is to accurately portray the logic function of the element and those used in this handbook are listed in Table 1. The preferred direction of signal flow through symbols and associated circuit is from left to right; inputs are on the left and outputs on the right. Exceptions to this convention are indicated by arrowheads in the signal lines showing the direction of signal flow, as shown in Fig. 12.

All outputs of a single element of a symbol have internal logic states that are determined by the element's function, unless otherwise indicated by an associated qualifying-symbol.

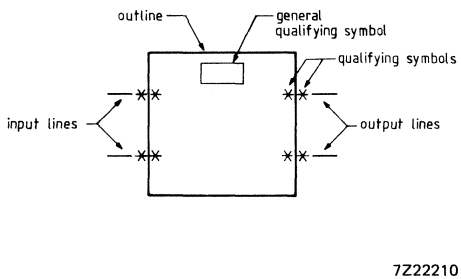


Fig. 1 Symbol composition.

Adjacent elements in a composite symbol may be joined by a common boundary line. When this boundary line is parallel to the direction of signal flow there is no logic connection between the elements, but when the line is perpendicular to the direction of signal flow then there is at least one logic connection between them. The number of logic connections between elements is shown by qualifying-symbols, but if there are no qualifying-symbols on either side of the common line then the elements have just one logic connection.

When a composite symbol contains at least one input common to one or more of the elements, a common-control block can be used. In the example of Fig. 2 the common-control block provides an input to each of the elements below it, this can be otherwise qualified by dependency notation.

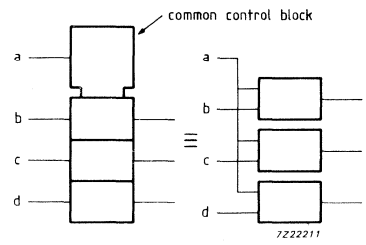


Fig. 2 Common-control block.

An output that depends on all elements of a composite symbol can be shown as an output from a common-output element. This part of the symbol is distinguishable by a double boundary line as shown in Fig. 3. The common-output element may have other inputs. Its function must be indicated by a qualifying-symbol within the outline.

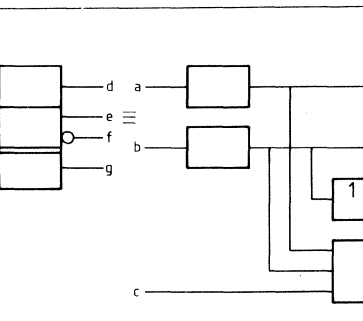


Fig. 3 Common-output element.

QUALIFYING-SYMBOLS

General qualifying-symbols

Table 1 shows the general qualifying-symbols used in this publication. These characters are usually placed near the top centre of a symbol element and define the logic function that is represented by the symbol or element.

Table 1 Oualifying-symbols - General

qualifying-symbol	definition
&	AND element. If all inputs are at internal logic "1" then the output is at internal logic "1"
≥ m	Logic threshold element. If at least m inputs are at internal logic "1" then the output is at internal logic "1"
≥ 1	OR element. If at least one input is at internal logic "1" then the output is at internal logic "1"
= m	m and only m element; if m inputs are at internal logic "1" then the output is at internal logic "1"
= 1	EXCLUSIVE-OR element. If only one input is at internal logic "1" then the output is at internal logic "1"
=	Logic identity element. If all inputs have the same logic state then the output is at internal logic "1"
> n/2	Majority element. If the majority of inputs are at internal logic "1" then the output is at internal logic "1"
2k	Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1"
2k+1	Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1"
1	Buffer element without specially amplified output. If the input is at internal logic "1" then the output is at internal logic "1"
or	Buffer elemtn with amplified output. The triangle points in the direction of signal flow
	Bi-threshold detector. Schmitt-trigger
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used
MUX	Multiplexer/data selector
DX	Demultiplexer
MUXDX	Bidirectional selector. MDX may be used as an alternative symbol
Σ	Adder

qualifying-symbol	definition
P-Q	Subtractor
CPG	Look-ahead carry generator
Π	Multiplier
COMP	Comparator
ALU	Arithmetic logic unit
	Retriggerable monostable element
1	Non-retriggerable monostable element
G	Astable element
!G	Synchronous-starting astable element
G!	Synchronous-stopping astable element
SGRm	Shift register. "m" = number of bits
CTRm	Binary counter. "m" = number of bits or is an indication of the cycle length 2^m
CTRDIVm	Counter with cycle length m
ROMm1xm2	Read only memory
PROMm1xm2	Programmable read only memory
RAMm1xm2	Random access memory
CAMm1xm2	Associative memory
FIFOm1xm2	First-in/first-out memory
	m1 is the number of words; m2 is the number of bits per word
I=0	Initial logic "0" state. When power is switched ON, the element goes to internal logic "0"
I=1	Initial logic "1" state. When power is switched ON, the element goes to internal logic "1"
NV	Non-volatile. The internal logic state is maintained regardless of power ON or OFF

qualifying-symbol	definition
Φ	Very complicated element. Depicted by a 'grey box' symbol. Within the 'grey box' outline, the Φ qualifying-symbol is accompanied by a further qualifying expression, e.g. ERR - for error detector or reference to supporting documentation, e.g. type number

Qualifying-symbols for inputs and outputs

Referring to Table 2, qualifying-symbols for inputs and outputs, the logic negation indicator is used in **pure logic diagrams** to indicate that an external logic "0" ("1") produces an internal logic "1" ("0") at the input, or that an internal logic "1" ("0") produces an external logic "0" ("1") at the output.

The polarity indicator is used in **detailed logic diagrams** to indicate which logic level corresponds with the internal logic "1". The following may occur:

- an input or output **with** polarity indicator indicates that the logic level "L" (LOW) corresponds to an internal logic "1".
- an input or output **without** polarity indicator indicates that the logic level "H" (HIGH) corresponds to an internal logic "1".

In an array of elements, if the same general qualifying-symbol and the same qualifying-symbols associated with inputs and outputs should appear inside each element of the array, then they are usually shown only in the first element. Similarly, for large identical elements with subdivisions, the subdivisions may be shown only in the first element. This is done to simplify the array and ease recognition. As an example, omissions of both repeating qualifying-symbols and subdividing lines can be seen in the HC/HCT242 symbol.

Table 2 Qualifying-symbols - Inputs and Outputs

qualifying-symbol	definition of input or output
	Logic negation at an input. An external logic "0" ("1") produces an internal logic "1" ("0")
	Logic negation at an output. An internal logic "1" ("0") produces an external logic "0" ("1")
	Polarity indicator at an input. A logic "L" (LOW) level ("H" (HIGH) level) at an input produces an internal logic "1" at that input
	Polarity indicator at an output. An internal logic "1" ("0") at an output produces a logic "L" (LOW) level ("H" (HIGH) level) at that output
	Polarity indicator at an input where the signal flow is from right to left
	Polarity indicator at an output where the signal flow is from right to left
(a)  (b) 	Indicator for direction of signal flow: (a) from right to left; (b) from bottom to top. With no indication of direction, flow is left to right or top to bottom
	Bidirectional information flow (alternate)
	Non-logic connection
	Input for analog signals
	Input for digital signals (used only to avoid confusion)

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Symbols inside the outline

Table 3 shows some of the symbols used within the symbol-outlines. Other symbols used in this handbook but not shown here are self-explanatory. Generally these are associated with arithmetic operations but all are in accordance with the IEC system. When non-standard information is shown inside a symbol-outline, it is enclosed in square brackets.

It can be seen in Table 3 that open-collector, open-emitter and three-state outputs have distinctive symbols. Note that an enable input (EN) affects all of the circuit outputs and has no effect on the inputs. When an enable input affects only certain outputs and/or one or more inputs, a form of dependency notation will indicate this (see 'Dependency Notation, EN-dependency').

Another important point is that a D-input is always the data input of a storage element. An internal logic "1" at the D-input sets the storage element to its "1" state, and an internal logic "0" at the D-input resets the storage element to its "0" state.

Grouping of inputs or outputs is indicated by the bit-grouping symbol. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. The weights of input and output lines are represented by powers-of-two only when the bit-grouping symbol is used, otherwise decimal equivalents are used. Inputs grouped together by this symbol produce an internal number that is the sum of the individual input weights at logic "1". This number can be a number on which a mathematical function is performed, an identifying number used in dependency notation or a value that becomes the content (CT) of the element (see Fig. 29). A frequent use of the bit-grouping symbol is in memory addressing, see also 'Use of Bit-grouping to Produce Affecting Inputs'. For outputs, usage of the bit-grouping symbol is similar to that of inputs; the number produced by the sum of the output weights is the internal number, or the content (CT) produced by the circuit.

The symbols shown in Table 3 may be used to indicate the internal connections between logic elements abutted together. Each logic connection may be shown by qualifying-symbols at one or both sides of the common line, however, if confusion could arise about the number of connections, one of the internal connection symbols may be used.

The internal (virtual) input is an input originating somewhere within the circuit and not connected directly to a terminal, and similarly the internal (virtual) output is not connected directly to a terminal.

Table 3 Symbols inside the outline

symbol inside outline	explanation
/	Solidus. Separator used in input and output labels. May be interpreted as an OR function
,	Comma. Separator with no logic significance
	Delayed output symbol for pulse and data-lock-out elements. The output change is delayed until the input that initiated the change (e.g. a "C" input) returns to its initial external state or level
	Bi-threshold input. Input with hysteresis
	Open output with low-impedance "L" (LOW) level
	Passive pull-up output. Similar to open output with low-impedance "L" level but with a built-in passive pull-up
	Open output with low-impedance "H" (HIGH) level

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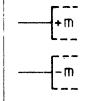
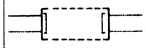
QUALIFYING-SYMBOLS (continued)

Table 3 Symbols inside the outline (continued)

symbol inside outline	explanation
	Passive pull-down output. Similar to open output with low-impedance "H" level but with a built-in passive pull-down
	Three-state output
	Enable input. When at internal logic "1", all outputs are enabled. When at internal logic "0": open outputs are OFF; three-state outputs retain their normal, defined internal logic state but give an external high-impedance state; all other outputs are at internal logic "0"
R, S, C, T	Control inputs of bistable elements
J, K, R, S, D	Information inputs of bistable elements
	Shift input. An internal logic "1" causes information contained in the element to be shifted m positions. The direction of shift is to the right or down when the arrow points to the right, or to the left or up when the arrow points to the left. The number may be omitted when "m" = 1
	Counting input. Count-up and count-down are indicated by + and − respectively. The number "m" is the count per command and may be omitted when "m" = 1
	Bit-grouping symbol. "m" is the highest power of 2 in the group. The asterisk shall be replaced by an appropriate indication of the operand, either the dependency notation or CT
	Content input. The internal logic "1" sets the element to the value "m"
	Content output. "*" is the value of the element that sets the output to an internal logic "1" (e.g. CT = 0, CT ⩾ 5, CT ≠ 4...9)
	Line-grouping symbol. The inputs or outputs enclosed by this symbol form a single logic input or output
	Fixed-mode input. This input is permanently at internal logic "1"

7Z22226

symbol inside outline	explanation
	Fixed-state output. This output is permanently at internal logic "1"
a...g	Seven segments of a display element
	Extension input. Input intended for connection to an extender output
	Extender output. Output to an extension input
	Operand input. This input represents one bit of an operand on which one or more mathematical functions are performed; "m" is the decimal equivalent of the **weight** of the bit. If the **weights** of all Pm inputs of the element are powers of 2 then "m" is the exponent of the power of 2
	Operand input. See Pm
	'Less-than' input of a magnitude comparator
	'Greater-than' input of a magnitude comparator
	'Equal' input of a magnitude comparator
	'Borrow-in' input of an arithmetic element
	'Borrow-generate' input of an arithmetic element
	'Borrow-generate' output of an arithmetic element
	'Borrow-out' output of an arithmetic element
	'Borrow-propagate' input of an arithmetic element

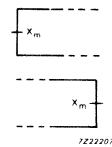
7Z22226

symbol inside outline	explanation
	'Borrow-propagate' output of an arithmetic element
	'Carry-in' input of an arithmetic element
	'Carry-generate' input of an arithmetic element
	'Carry-generate' output of an arithmetic element
	'Carry-generate' output of an arithmetic element
	'Carry-propagate' input of an arithmetic element
	'Carry-propagate' output of an arithmetic element
Π	Result of a multiplication
Σ	Result of an addition
P-Q	Result of a subtraction
	Added information
φm	Clock phase. "m" is the clock phase number
	Connection for external capacitor(s).
	Connection for external resistor(s).

7Z22227

symbol inside outline	explanation
	Dynamic input. A transition from logic "L" level to "H" level produces a transitory internal logic "1"
	Dynamic input. A transition from logic "H" level to "L" level produces a transitory internal logic "1"
	Internal connection. A logic "1" at the left-hand side produces a logic "1" at the right-hand side
	Negated internal connection. A logic "1" at the left-hand side produces a logic "0" at the right-hand side
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left-hand side produces a transitory logic "1" at the right-hand side
	Negated dynamic internal connection. A transition from internal logic "1" to internal logic "0" at the left-hand side produces a transitory internal logic "1" at the right-hand side
	Internal (virtual) input. This input is always at internal logic "1" state unless it is affected by a dependency notation
	Internal (virtual) output. The effect on the internal input connected to this output must be indicated by dependency notation

7Z22227

 7Z22207	Internal transmission path. Internal logic "1" enables internal transmission path. Internal logic "0" disabled internal transmission path

DEPENDENCY NOTATION

General conventions of dependency notation

Dependency notation is the powerful tool that makes IEC symbols compact and yet meaningful. With IEC symbols, the relationships between inputs and other inputs, between outputs and other outputs, and between inputs and outputs are clearly illustrated without the necessity to show all elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying-symbols for an element's function.

In dependency notation, the terms "affecting" and "affected" are used. In cases where it is not evident which inputs must be selected as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the most convenient input has been chosen.

The types of dependency described in this section are "G" (AND); "V" (OR); "N" (negate, or EXCLUSIVE-OR); "Z" (interconnection); "C" (control); "S" and "R" (set and reset); "EN" (enable); "M" (mode); and "A" (address).

The general rules applied to dependency notation are:

- the input (or output) affecting other inputs or outputs is labelled with the letter symbol that indicates the relationship involved (e.g. G for AND) followed by an appropriately-chosen identifying number; and
- each input or output affected by that affecting input (or output) is labelled with that same number.

If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together (see Fig. 4).

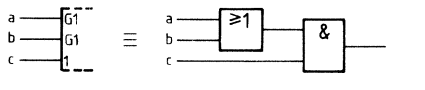


Fig. 4 ORed affecting inputs.

If an input or output is affected by more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal reading order of these numbers is the same as the sequence of the affecting relationships (see Fig. 5).

Fig. 5 Input affected by more than one input.

If the labels denoting the function of affected inputs or outputs are numbers, (e.g., inputs or outputs of a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, e.g., Greek letters (see Fig. 6).

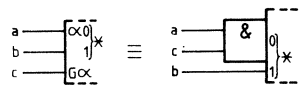


Fig. 6 Substitution for numbers.

If it is the complement of the input's (or output's) internal logic state that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (see Fig. 7).

If the affected input or output has a label to denote its function (e.g. "D"), this label will have the identifying number of the affecting input as a prefix (see Fig. 13).

G-dependency

The traditional method of showing an AND relationship was to use an explicit drawing of an AND gate with the signals connected to the inputs of the gate. With IEC symbology (see Fig. 7), input "b" and input "a" are ANDed together and the complement of "b" is ANDed with "c". The letter G has been chosen to indicate AND relationships and is placed at input "b", within the outline. A number considered appropriate by the designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input "c".

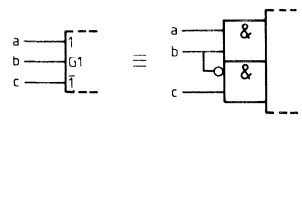


Fig. 7 G-dependency between inputs.

In Fig. 8, output "b" affects input "a" with an AND relationship. The lower example shows it is the internal logic state of "b", unaffected by the negation sign, that is ANDed.

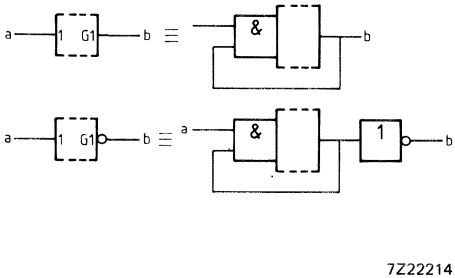


Fig. 8 G-dependency between outputs and inputs.

In Fig. 9, input "a" is ANDed with the dynamic input "b".

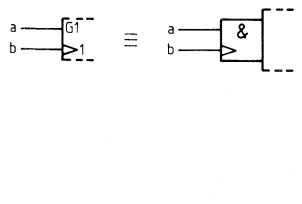


Fig. 9 G-dependency with a dynamic input.

To summarize G-dependency using input G and allotted number m: when a Gm-input (Gm-output) is at internal logic "1", all inputs and outputs affected by Gm will be at their normally defined internal logic states. When the Gm-input (Gm-output) is at internal logic "0", all inputs and outputs affected will be at internal logic "0".

V-dependency

When a Vm-input (Vm-output) is at internal logic "1", all inputs and outputs affected by Vm will be at internal logic "1". When the Vm-input (Vm-output) is at internal logic "0", all inputs and outputs affected by Vm will be at their normally defined internal logic states (see Fig. 10).

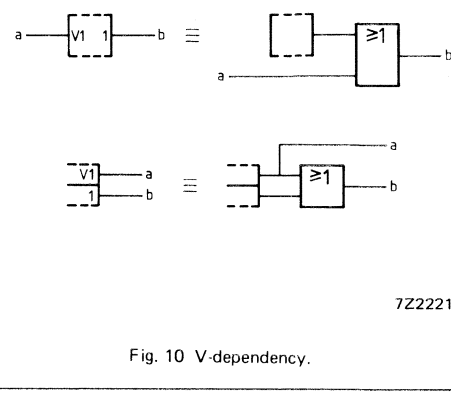


Fig. 10 V-dependency.

N-dependency

Each input or output affected by an Nm-input (or output) is EXCLUSIVE-ORed with the Nm-input (or output) (see Fig. 11).

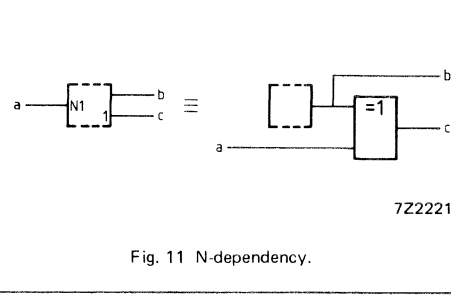


Fig. 11 N-dependency.

When an Nm-input (Nm-output) is at internal logic "1", the internal logic state of each input and each output affected by Nm will be complemented. When an Nm-input (Nm-output) is at internal logic "0", all inputs and outputs affected by Nm will be at their normally defined internal logic states.

DEPENDENCY NOTATION (continued)

Z-dependency

Interconnection dependency is used to indicate internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

All inputs or outputs affected by a Zm-input (or output) will take on the same internal logic state as the Zm-input (or output), unless modified by additional dependency notation (see Fig. 12).

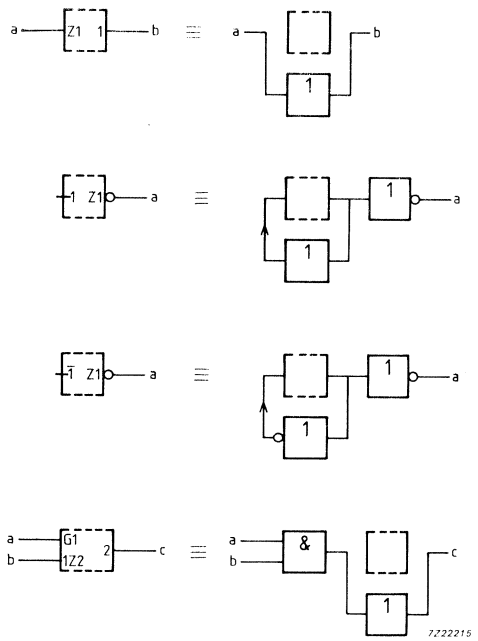


Fig. 12 Z-dependency.

C-dependency

Control inputs enable or disable the data (D, J, K, R or S) inputs of storage elements (see Fig. 13).

When a Cm-input is at internal logic "1", the inputs affected by Cm have their normal effect on the function of the element, i.e. these inputs are enabled. When a Cm-input is at internal logic "0", the inputs affected by Cm are disabled and have no effect on the function of the element.

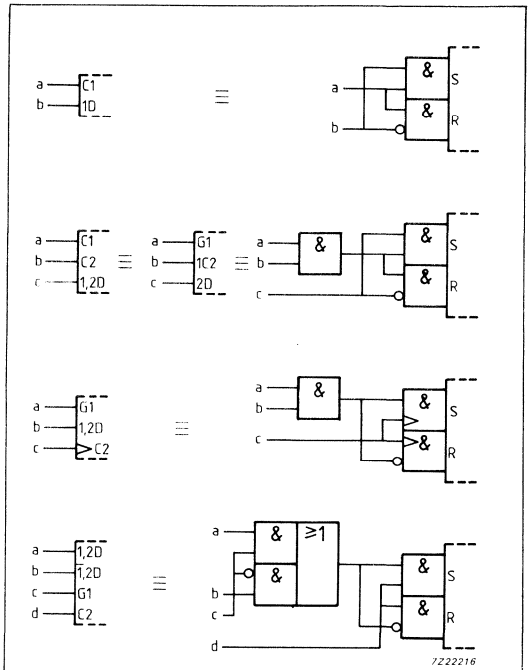
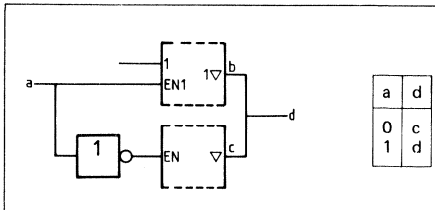


Fig. 13 C-dependency.

EN-dependency

An ENm-input has the same effect on outputs as an EN-input (see Table 1) but it affects both inputs and outputs that have the identifying number "m", whereas an EN-input affects all outputs and no inputs.

The effect of an ENm-input on an affected input is identical to that of a Cm-input (see Fig. 14).



a	d
0	c
1	d

Fig. 14 EN-dependency.

When an ENm-input is at internal logic "1", inputs and outputs affected by ENm are enabled.

When an ENm-input is at internal logic "0": inputs and outputs affected by ENm are disabled; open outputs are turned OFF; passive pull-up outputs will be high-impedance "L" level; passive pull-down outputs will be high-impedance "H" level; 3-state outputs will have their normally defined internal logic states but externally exhibit high-impedance; and all other inputs (e.g., totem-pole outputs) will be at internal logic "0".

S and R-dependencies

Set and reset dependencies are used if the effect of the combination R=S=1 on a bistable element must be specified. Figure 15a does not use S or R-dependency (? = not specified).

When an Sm-input is at internal logic "1", outputs affected by the Sm-input will react, regardless of the state of an R-input, as they would normally react to the combination S =1, R=0 (see Fig. 15b).

When an Rm-input is at internal logic "1", outputs affected by the Rm-input will react, regardless of the state of an S-input, as they would normally react to the combination S=0, R=1 (see Fig. 15c).

The non-complementary output patterns in Figs 15d and 15e are only pseudo-stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.

When an Sm or Rm input is an internal logic "0", it has no effect.

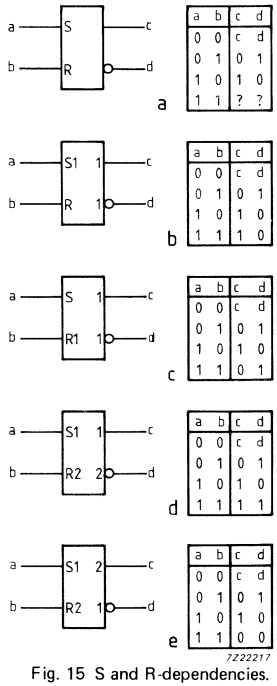


Fig. 15 S and R-dependencies.

M-dependency

Mode dependency indicates that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

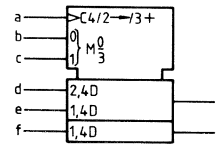
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting Mm-inputs will appear in parentheses, separated by solidi, in the label of the affected input or output (see Fig. 20).

M-dependency affecting inputs

When an Mm-input (Mm-output) is at internal logic "1", the inputs affected by this Mm-input (Mm-output) will be enabled.

When an Mm-input (Mm-output) is at internal logic "0", the inputs affected by this Mm-input (Mm-output) will be disabled. When an affecting input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the Mm-input (Mm-output) appears has no effect and is to be ignored. This represents the disabling of some of the functions of a multi-function input.

The circuit in Fig. 16 has two inputs, "b" and "c", these control the one of four modes (0, 1, 2 or 3) that will exist at any time. Inputs "d", "e", and "f" are D-inputs subject to dynamic control (clocking) by the "a" input. The numbers 1 and 2 identify the operating modes, and so inputs "e" and "f" are only enabled in mode 1 (for parallel loading) and input "d" is only enabled in mode 2 (for serial loading). Input "a" has three functions: it is the clock for entering data; in mode 2 it causes right-shifting of data (shifts away from the control block); and in mode 3 it causes the contents of the register to be incremented by one.



All operations are synchronous.

Mode 0 (b=0, c=0):
The outputs remain at their existing states as the inputs have no effect.

Mode 1 (b=1, c=0):
Parallel loading takes place through inputs "e" and "f".

Mode 2 (b=0, c=1):
Shifting down and serial loading takes place through input "d".

Mode 3 (b=c=1):
Counting up takes place in increments of 1 per clock pulse.

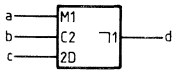
Fig. 16 M-dependency affecting inputs.

DEPENDENCY NOTATION (continued)

M-dependency affecting outputs

When an Mm-input (Mm-output) is at internal logic "1", the affected outputs will be enabled.

When an Mm-input (Mm-output) is at internal logic "0", the affected outputs will be disabled. When an input or output has several different sets of labels separated by solidi (e.g., 2,4/3,5), any set in which the identifying number of the Mm-input (Mm-output) appears is to be ignored.



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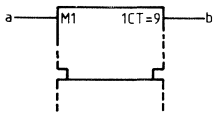
Mode 1 (a=1):
The delayed output symbol is effective only in mode 1 and therefore the device functions as a pulse-triggered D-element.

Mode 2 (a=0):
The delayed output symbol has no effect and therefore the device functions as a transparent latch.

Fig. 17 Flip-flop type determined by mode.



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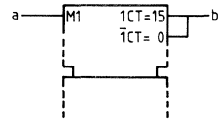
Mode 1 (a=1):
Output "b" will be an internal logic "1" only when the register content equals 9.

Mode 2 (a=0):
Since output "b" is located in the common-control block with no defined function outside of mode 1, this output will be an internal logic "0" when input "a" is an internal logic "0", regardless of the register content.

Fig. 18 Disabling an output of the common-control block.



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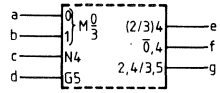
Mode 1 (a=1):
Output "b" will be an internal logic "1" only when the register content equals 15.

Mode 2 (a=0):
Input "a" is an internal logic "0", output "b" will be an internal logic "1" only when the register content equals 0.

Fig. 19 Determining an output's function.



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Inputs "a" and "b" are binary weighted to generate the numbers 0, 1, 2 or 3 to determine which of the four modes exist.

Mode 0 (a=0, b=0):
Since no output label contains a "0", the outputs have their normally defined internal logic states. Output "f" carries a "$\overline{0}$" in its label and this means that output "f" is effected by all modes **except** mode 0.

Mode 1 (a=1, b=0):
Only output "f" is affected by mode 1 and is also affected by input "c" (N4).

Mode 2 (a=0, b=1):
The outputs "e" and "g" are affected in this mode. They are also affected by input "c" (N4) which means that the internal logic state of the output will be negated at N4=1. Output "f" is affected since M0 stands at its internal "0" state.
In addition, output "f" is affected by input "c" (N4).

Mode 3 (a=1, b=1):
All outputs shown are affected in this mode, with outputs "e" and "f" also affected by input "c" (N4) and input "d" also affecting output "g".

Fig. 20 Dependent relationships affected by mode.

A-dependency

Using address-dependency gives a clear representation of elements, particularly memories, that use address control inputs to select sections of a multi-dimensional array. Such a section of a memory array is usually called a word. Address-dependency allows a symbolic representation of an entire array. An array input at a particular element of a general section is common to the corresponding elements of all selected sections of the array. An array output at a particular element of a general section is the result of ORing the outputs of the corresponding elements of selected sections. If the label of an array output at a particular element of a general section indicates that this output is an open-circuit or a 3-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any input have their normal effect on all sections of the array, whereas inputs affected by an address input only have their normal effect on the section selected by that address input.

An affecting address input has the label "A" followed by an identifying number which corresponds to the address of the particular section of the array selected by this input. Within the general section represented by the symbol, inputs and outputs affected by an "Am" input have the label "A", which stands for the identifying numbers, i.e. the addresses of the particular sections.

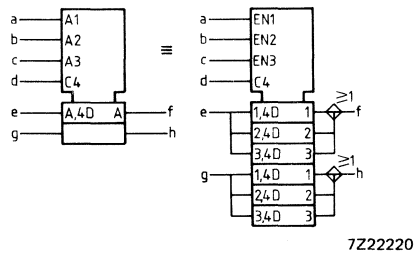


Fig. 21 A-dependency.

Figure 21 shows a 3-word x 2-bit memory having a separate address line for each word; EN-dependency is used to explain the operation. To select word 1, input "a" is forced to logic "1", entering mode 1. Data can now be clocked into the inputs marked "1,4D". Data cannot be clocked into the inputs marked "2,4D" and "3,4D" unless words 2 and 3 are selected. The outputs will be the OR function of the selected outputs, i.e. only those enabled by the active EN functions.

The identifying numbers of affecting inputs correspond to the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, ..), because in the general section represented by the symbol they are replaced by the letter "A".

If there are several sets of affecting "Am" inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter "A" is modified to 1A, 2A, ... These sets of "A" inputs may have the same identifying numbers.

Another illustration of the concept is shown in Fig. 22.

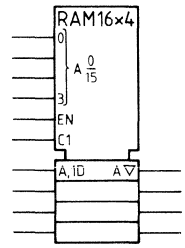


Fig. 22 Array of 15 sections of four transparent latches with 3-state outputs comprising a 16-word x 4-bit random-access memory.

X-dependency

When a Xm-input (Xm-output) is at internal logic "1", transmission paths will be established between the affected inputs and outputs. Transmission paths between an output (input) affected by more than one Xm-input (Xm-output) will be established when all affecting Xm-inputs (Xm-outputs) are at internal logic "1". All inputs and outputs affected by Xm will be at their normal analog signal or internal logic state unless otherwise specified by an additional notation, e.g. dependency notation. When a Xm-input (Xm-output) is at internal logic "0" or modified to have no effect on the function of the element, then transmission paths will not exist.

DEPENDENCY NOTATION (continued)

X-dependency (continued)

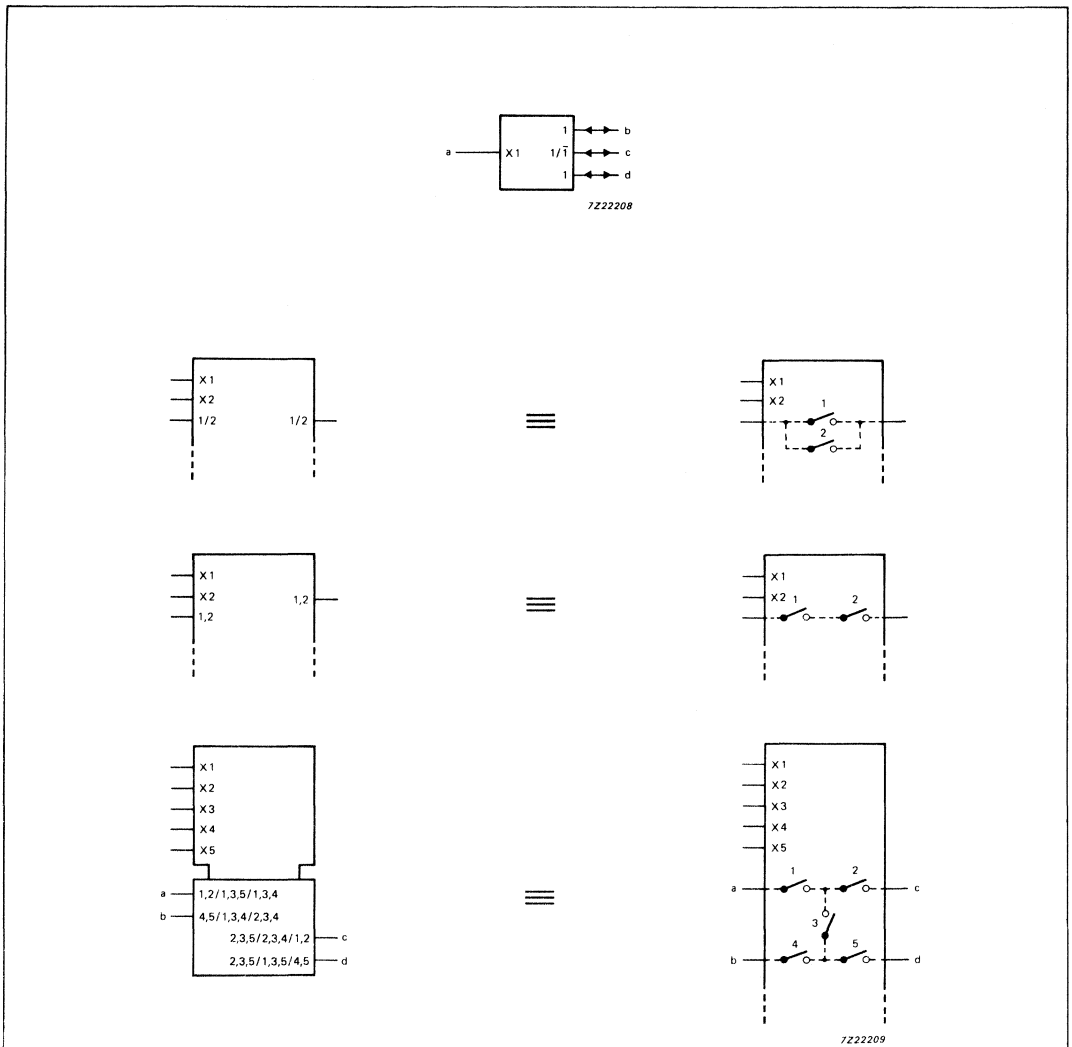


Fig. 23 X-dependency.

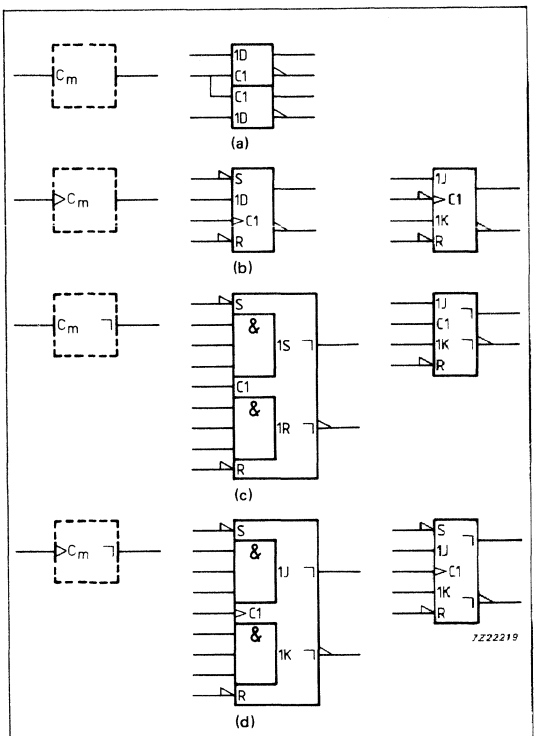
Table 4 Summary of dependency notation

type of dependency	letter-symbol*	affecting input at logic "1"	affecting input at logic "0"
address	A	permits action (address selected)	prevents action (address not selected)
control	C	permits action	prevents action
enable	EN	permits action	prevents action of affected inputs; imposes external high impedance on open circuit and 3-state outputs (internal logic state of 3-state output is unaffected); ⏀ outputs high impedance "H" level; ⏁ outputs high impedance "L" level; other outputs at internal "0" state
AND	G	permits action	imposes "0" state
mode	M	permits action (mode selected)	prevents action (mode not selected)
negate (EXCLUSIVE-OR)	N	complements state	no effect
reset	R	affected output reacts as it would to S = "0", R = "1"	no effect
set	S	affected output reacts as it would to S = "1", R = "0"	no effect
OR	V	imposes "1" state	permits action
inter-connection	Z	imposes "1" state	imposes "0" state
transmission path	X	permits action	permits actions

* These letter symbols appear at the **affecting** input (or output) and are followed by a number. Each input (or output) **affected** by that input is labelled with that same number. The descriptions do not apply when the labels "EN", "R" and "S" appear at inputs without numbers following; the action of these inputs is described in 'Symbols inside the outline'.

BISTABLE ELEMENTS

The dynamic input symbol, the delayed output symbol and dependency notation allow the four main types of bistable elements to be shown and make synchronous and asynchronous inputs easily recognizable (see Fig. 24). A fifth type of bistable, the direct acting "SR" element, is mentioned in 'S and R-dependencies'.



The left-hand column of drawings shows essential distinguishing features of the bistables; the other columns show examples.

Fig. 24 Four types of bistable circuits: (a) latch; (b) edge-triggered; (c) pulse-triggered; (d) data-lock-out.

Transparent latches have a level-operated control input. The D-input is active as long as the C-input is at internal logic "1". The outputs respond immediately. Edge-triggered elements accept data from "D", "J", "K", "R" or "S" inputs on the active transition of "C". Pulse-triggered elements require the data to be set up before the start of the control pulse; the "C" input is considered static since the data must be maintained as long as "C" is at logic "1". The output is delayed until "C" returns to logic "0". The data-lock-out element is similar to the pulse-triggered version except that the "C" input is considered to be dynamic, in that shortly after "C" goes through its active transition, the data inputs are disabled and data does not have to be maintained. However the output is still delayed until the "C" input returns to its initial external level.

Note that synchronous inputs can be recognized easily because of labels (1D, 1J, 1K, 1S, 2R) unlike the asynchronous inputs "S", "R", which are not dependent on the "C" inputs.

CODERS

The general symbol for a coder or code-converter is shown in Fig. 25. The labels "X" and "Y" may be replaced by appropriate indications of the code that is used to represent the information at the respective inputs and outputs.

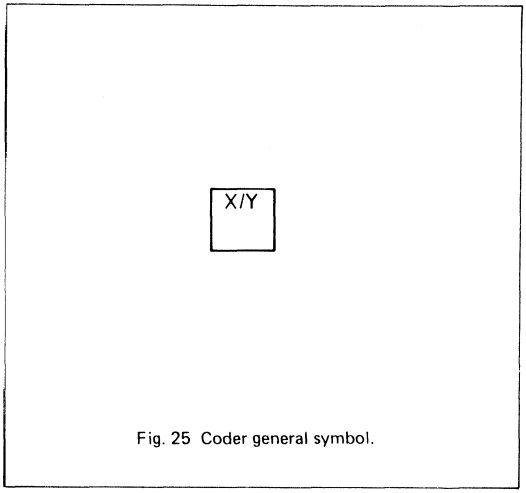


Fig. 25 Coder general symbol.

Indication of code conversion is based on the following rule:

Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

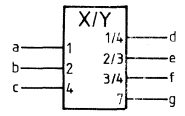
The relationship between the internal logic states of the inputs and the internal value is indicated by:

Labelling the inputs with numbers so that the internal value equals the sum of the weights associated with those inputs that are at internal logic "1"; or by replacing "X" by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationship between the internal value and the internal logic states of the outputs is indicated by:

Labelling each output with a list of numbers representing those internal values that force that output to an internal logic "1". The numbers are separated by solidi (see Fig. 26). This labelling may also be applied when "Y" is replaced by a letter denoting a type of dependency (see 'Use of a coder to produce affecting inputs'). If a continuous range of internal values produces the internal logic "1" at an output, this is indicated by the numbers that begin and end the range, separated by three dots, e.g. "4...9" equals "4/5/6/7/8/9"; or by replacing "Y" with an appropriate indication of the output code and labelling the outputs with characters that refer to this code (see Fig. 27).

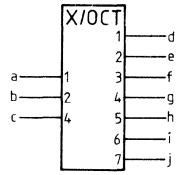
Alternatively the general symbol may be used together with an appropriate reference to a table detailing the relationship between the inputs and outputs. This is a recommended way to symbolize a ROM, or a PROM after it has been programmed.



TRUTH TABLE

inputs			outputs			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Fig. 26 An X/Y code converter.



TRUTH TABLE

inputs			outputs						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Fig. 27 An X/octal code converter.

USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case the symbols for a coder can be used as an embedded symbol (see Fig. 28).

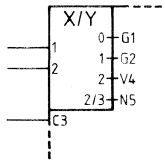


Fig. 28 Producing various types of dependencies.

If all affecting inputs produced by a coder are the same type and their identifying numbers correspond with the numbers shown at the coder outputs, "Y" (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. In this case, affecting input indications should be omitted (see Fig. 29).

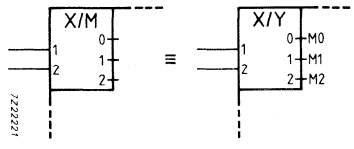


Fig. 29 Producing one type of dependency.

USE OF BIT-GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are the same type and have consecutive identifying numbers (not necessarily corresponding to the numbers that would have been shown at the outputs of the coder) the bit-grouping symbol can be used (see Table 1). Effectively, "k" external lines generate 2^k internal inputs. The bracket precedes the letter denoting the type of dependency which is followed by $^{m1}/_{m2}$. The "m1" is then replaced by the smallest identifying number and "m2" by the largest (see Fig. 30).

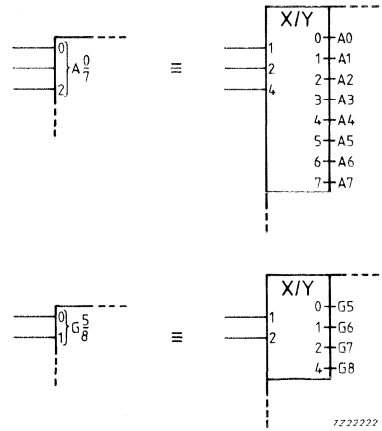


Fig. 30 Use of the bit-grouping symbol.

SEQUENCE OF INPUT LABELS

If an input having a single function is affected by other inputs, the qualifying-symbol (if there is one) for that function is preceded by the labels of the affecting inputs. The left-to-right order of these labels is the sequence in which the effects or modifications must be applied. The affected input has no effect on the element if the logic state of any of the affecting inputs (regardless of the logic states of other affecting inputs) would cause the affected input to have no effect.

If an input has several functions or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of representation is undesirable. In these cases, the input may be shown once with the different sets of labels separated by solidi (see Fig. 31). No meaning is attached to the order of these sets of labels. If one of the functions of an input is as an unlabelled input to an element, a solidus will precede the first set of labels.

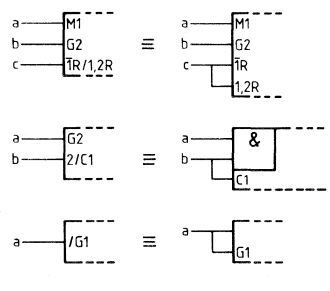


Fig. 31 Input labels.

If all inputs of a combinative element are disabled (have no effect on the function of the element), the internal logic states of the element outputs are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

Labels may be factorized using algebraic techniques (see Fig. 32).

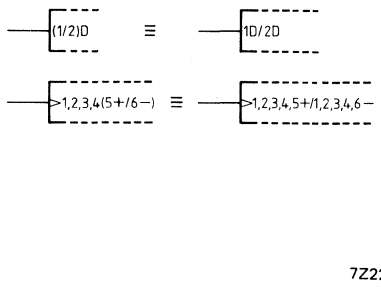


Fig. 32 Factorizing input labels.

When at latched inputs the algebraic factorizing technique is combined with the use of the bit-grouping symbol, the indication "mD" may be placed behind the bit-grouping symbol provided that the proper order of all the other labels is maintained (see Fig. 33).

In "mD", the "m" stands for the identifying numbers of the affecting inputs.

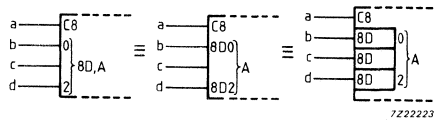


Fig. 33 Algebraic factorizing technique combined with the bit-grouping symbol at "D" inputs.

SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether or not they are identifying numbers of affecting inputs or outputs, these labels are shown in the following order (see Fig. 34):

the delayed output symbol comes first (if to be shown) preceded if necessary by the indications of the inputs to which it must be applied;

followed by the labels indicating modifications to the internal logic state of the output, such that the left-to-right order of these labels is the sequence in which their effects must be applied;

followed by the label indicating the effect of the output on the inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside boundary of the element adjacent to the output line, except when using the bit-grouping symbol (see Fig. 37).

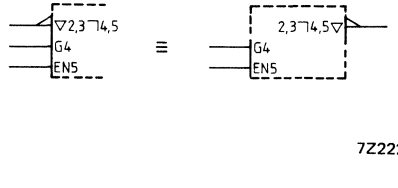


Fig. 34 Placement of 3-state symbols and delayed output symbols.

If an output needs several sets of labels to represent alternative functions, depending on the mode of action, these sets may be shown on different output lines connected together outside the outline. However, there are cases in which this representation is undesirable. In these cases the output may be shown once with the different sets of labels separated by solidi (see Fig. 35).

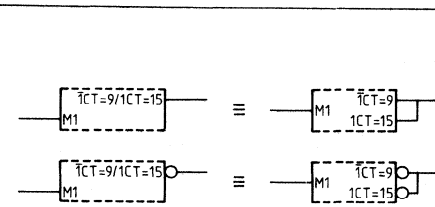


Fig. 35 Output labels.

SEQUENCE OF OUTPUT LABELS (continued)

Adjacent identifying numbers of affecting inputs that are not separated by a non-numeric character are separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting "Mm" input at internal logic "0", this set of labels has no effect on the output.

Labels may be factorized using algebraic techniques (see Fig. 36).

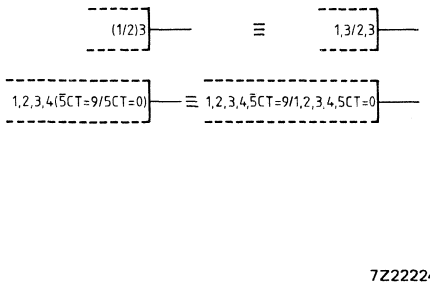


Fig. 36 Factorizing output labels.

If the bit-grouping symbol for outputs is used and the sets of labels of all outputs grouped together differ only in the indications of the weights, the sets of labels may be shown only once between the symbol replacing "*" and the grouping symbol (see Table 3) provided that, except for the grouping symbol and the weights, the proper order of the labels is maintained (see Fig. 37). These sets of labels, therefore, include the symbols for open-circuit, passive pull-down, passive pull-up and 3-state outputs but exclude the indications of weights.

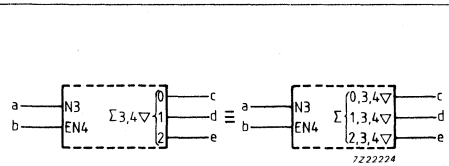


Fig. 37 The bit-grouping symbol at outputs.

RULES FOR SIMPLIFICATION OF SYMBOLS

INTRODUCTION

The IEC symbology can depict a complete integrated circuit but, in many applications, not all available functions are used. For these applications the complete symbol need not be shown and a considerable simplification can be made. To maintain clarity, rules for the simplification of symbols are described in this section.

RULE 1

For an integrated circuit where not all functions are used, the diagram may contain:

a. the complete symbol with indications of which pins are connected to a certain voltage level;

b. a simplified symbol where only the functions used are depicted; the unused pins are detailed in a table including information on whether these pins may remain open (floating) or are to be connected to a certain voltage level.

RULE 2

When two or more pins are shown with a single line, then a comma between the pin numbers means that these pins are connected together; when the pin numbers are separated by a solidus, this means they are separate functions.

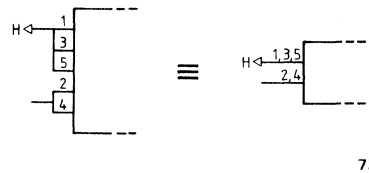


Fig. 39 Example of Rule 2.

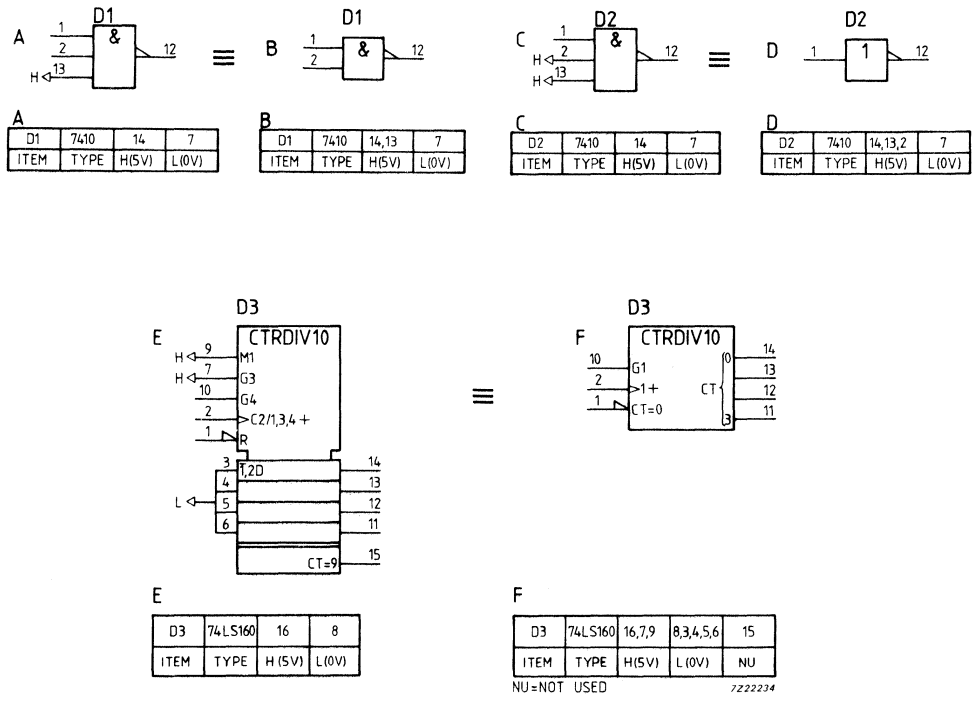


Fig. 38 Examples of Rule 1.

RULE 3

The rules for sets of labels at inputs and outputs using solidi to separate the various parts of a label may be applied when drawing two or more pins with a single line, so the labels must also be joined.

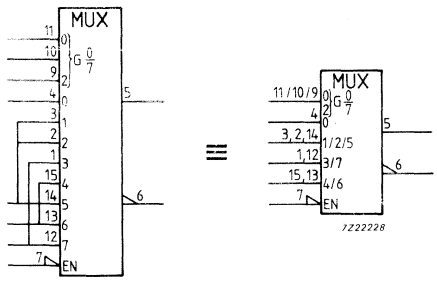


Fig. 40 Example of Rule 3 showing 8-input multiplexer.

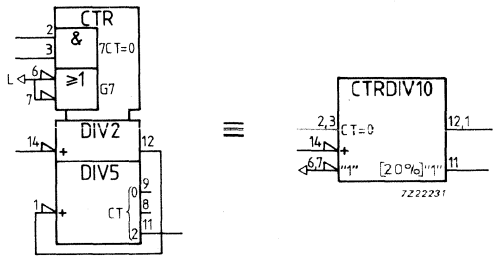


Fig. 42 Example of Rule 4.

RULE 4

An output can be connected to an input of equal polarity as shown in Fig. 41C. If the polarity is different this method does not give sufficient information and the methods of Fig. 41A or B are then adopted.

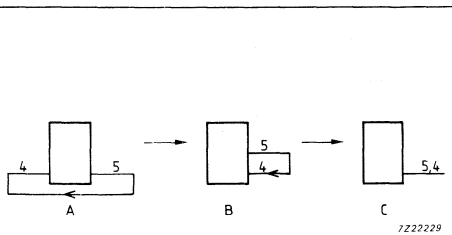


Fig. 41 Examples of Rule 4.

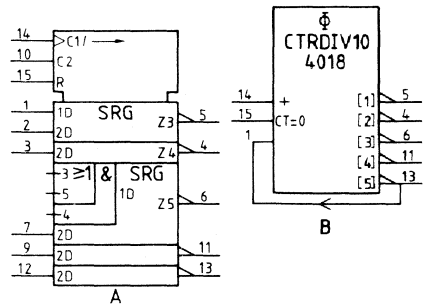


Fig. 43 Example of Rule 4;
the full symbol shown in (A) can be reduced to that of (B) when no parallel loading is applied and the device is used as a divide-by-10 circuit.

RULE 5

Combining elements together to form one element is allowed only if all pin numbers can be shown.

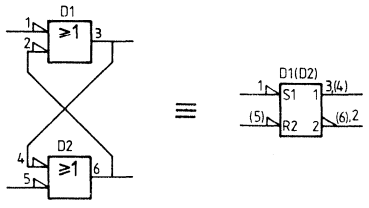


Fig. 44 Example of Rule 5; the pin numbers between parentheses indicate that these belong to another circuit.

RULE 6

A circuit consisting of a combination of two or more elements that appear repeatedly on a diagram, may be replaced by a single symbol. This symbol is used on the diagram, while the complete circuit is shown in an auxiliary diagram elsewhere on the drawing.

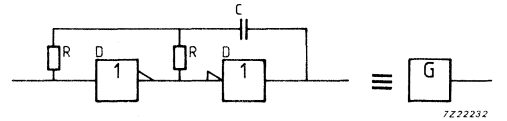


Fig. 45 Example of Rule 6.

RULE 7

A multiple symbol may also be applied for symbols.

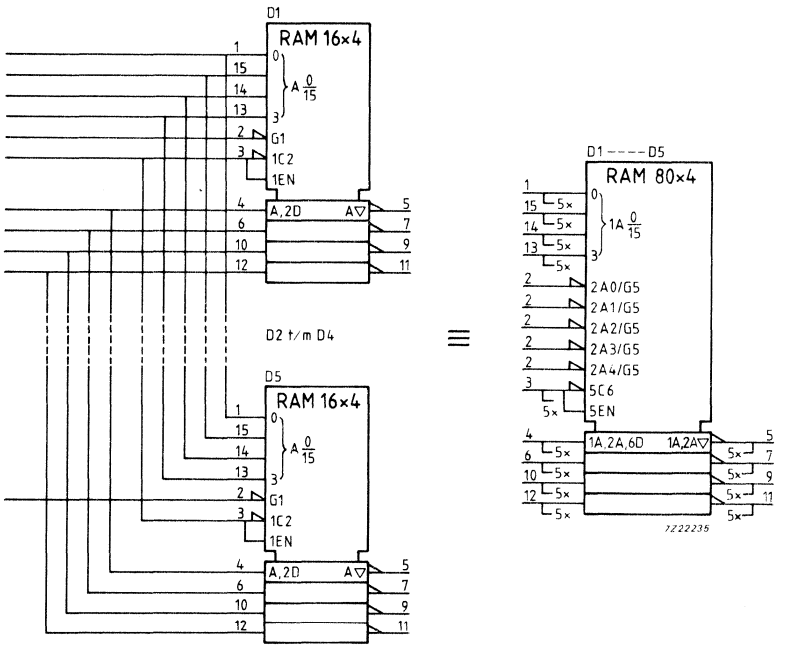


Fig. 46 Example of a multiple symbol showing five 16x4-bit RAMs connected to enlarge the number of words.

RULE 7 (continued)

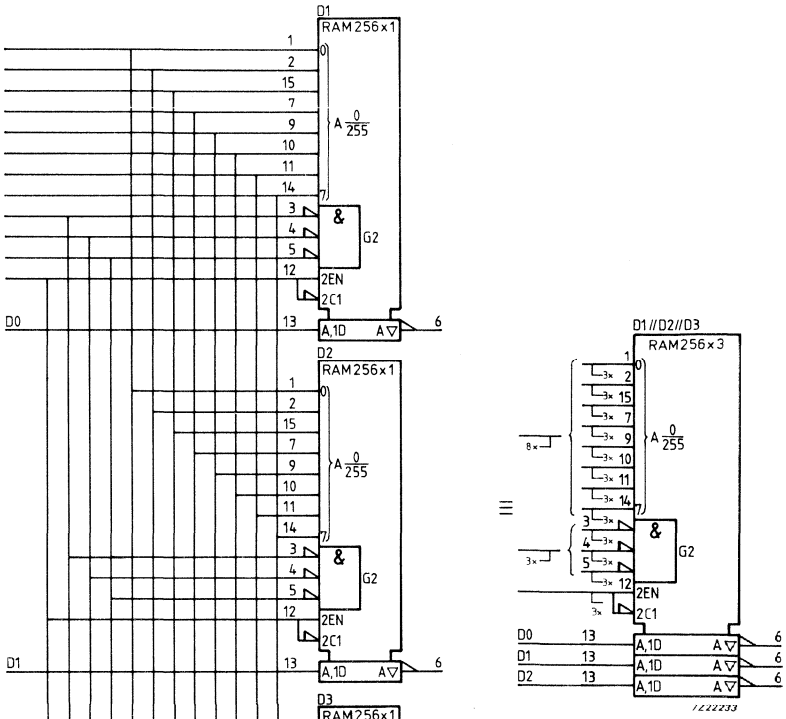


Fig. 47 Example of a multiple symbol showing three 256x1-bit RAMs connected to lengthen the word.

RULE 8

Every(P)ROM may be regarded as an X/Y-code-converter.

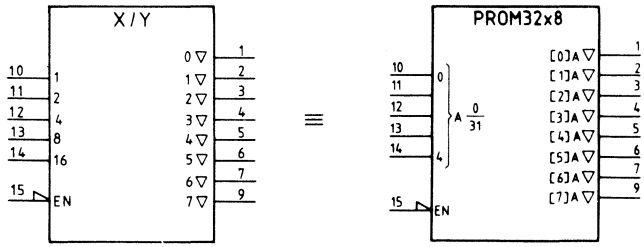
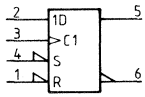


Fig. 48 Example of Rule 8 using Schottky PROM.

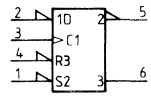
EXAMPLES OF APPLICATION-DEPENDENCY OF SYMBOLS

A symbol depicts the function of an element. In the case of multi-function elements, the functions are depicted separately.

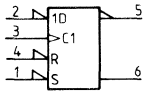
To demonstrate application-dependency of symbols, Fig. 49 shows the basic symbol and eight applications of a D-element with "S" and "R" inputs.



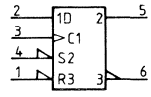
(A) basic symbol



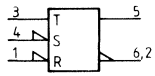
(B) as for (A) but with "R" and "S" dependency



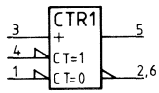
(C) D-input ("L")
(note change of "R" and "S")



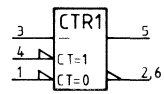
(D) as for (B) but with "S" and "R" dependency



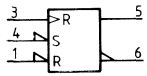
(E) divide-by-2 ("T") element



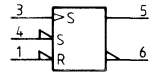
(F) divide-by-2 as a limit case of CTR



(G) as for (F) with down-counter



(H) function at pin 2 = "L", or as indicated in a table



(I) function at pin 2 = "H", or as indicated in a table

7Z22230

Fig. 49 Example of application-dependent symbols for edge-triggered D-element with "R" and "S" inputs.

HE4000B FAMILY-INTRODUCTION

INTRODUCTION TO THE HE4000B FAMILY DATA SHEETS

The LOCMOS HE4000B range is a fully buffered digital integrated circuit family which meets the Jedec-B specification. The members of this family are pin-compatible with the well-known C-MOS 4000 and 14500 ranges. The HE family has the same advantages as conventional C-MOS circuits, plus the additional LOCMOS advantages.

LOCMOS means: Local Oxidation Complementary MOS.

The main effect of LOCMOS is a considerable reduction in the chip area required for a given function. Also important is the reduction in stray capacitance due to the smaller contact areas - hence the higher switching speed. Another benefit, brought about by the manufacturing process, is the self-alignment of the source and drain diffusions. This means that tolerance margins in the diffusions are unnecessary, thus further reducing the stray capacitances.

Advantages of C-MOS:

- low power dissipation - typically 10 nW per gate (static);
- wide operating supply voltage range;
- wide operating temperature range;
  −40 to + 85 °C (HEF range in plastic DIL, ceramic DIL and plastic mini-pack (SO) packages)
  −55 to + 125 °C (HEC range in ceramic DIL packages only);
- high DC fan-out;
- inputs and outputs are protected against electrostatic voltages.

In addition to these, the LOCMOS HE4000B range has:

- buffered outputs on **all** circuits;
- higher speed;
- higher packing density - essential for MSI/LSI;
- excellent noise immunity.

The HE family is designed with standardized output drive characteristics which, combined with relative insensitivity to output capacitance loading, simplify system design.

Note

On page 1 of most of the device data sheets are shown a pinning diagram together with a functional diagram. In addition to this functional diagram, a more detailed logic diagram is given, which also shows the buffered outputs.

BUFFERED OUTPUTS

To minimize any pattern sensitivity of propagation delay, and to standardize delay and output drive, all HE family devices have an output buffer stage (see Fig. 1). Buffering improves the static noise immunity because the increased voltage gain gives nearly ideal transfer characteristics and the low output impedance gives significant improvement of the dynamic noise immunity. Significant pulse shaping is obtained because output transitions are virtually independent of input rise and fall times.

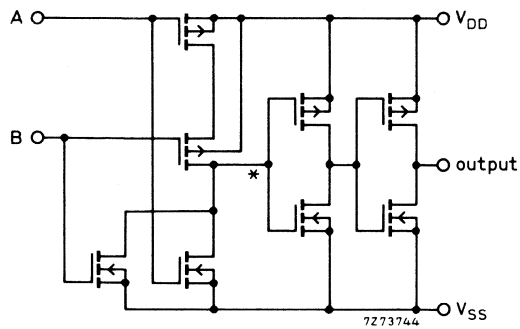


Fig. 1 Two-input NOR gate with fully buffered output; a typical LOCMOS circuit.
In an unbuffered device the output would be taken from the point marked*.

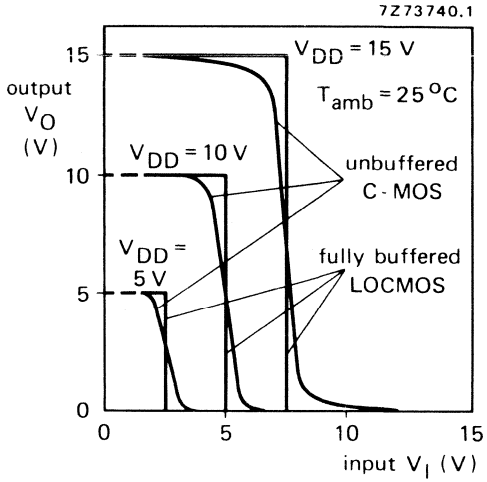


Fig. 2 Typical transfer characteristic showing improvement in buffered LOCMOS device as compared with unbuffered C-MOS device.

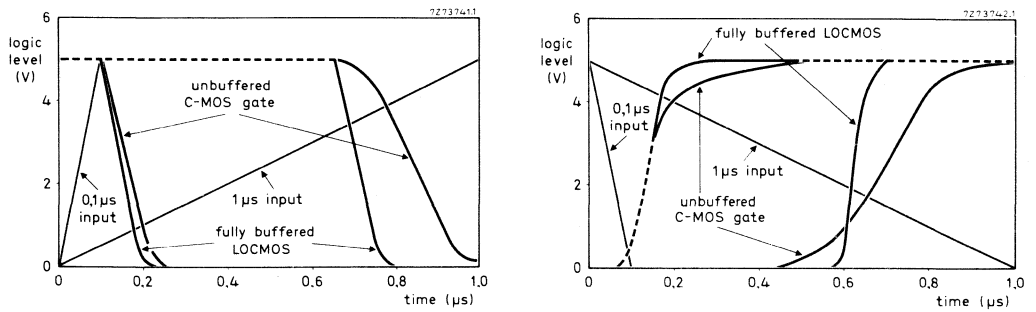


Fig. 3 The two graphs show how the output transitions are independent of input rise time (a) and fall time (b).

DESIGN CONSIDERATIONS

General

Local Oxidation Complementary MOS digital integrated circuits of SSI and MSI complexity have been hailed as the ideal logic family. A few LOCMOS devices, such as bidirectional analogue switches, exploit the unique feature of C-MOS technology; some take advantage of the smaller device size and higher potential packing density to achieve true LSI complexity, and perform logic functions that have been available in TTL for may years. Therefore, it is both helpful and practical to compare the performance of LOCMOS with that of the more familiar TTL (see table below).

LOCMOS speed is about three to six times lower than TTL or low-power Schottky (LS-TTL). Static noise immunity and fan-out are almost ideal, supply voltage is non-critical, and the quiescent power consumption is close to zero — several orders of magnitude lower than for any competing technology.

For dynamic noise immunity, see NOISE IMMUNITY.

	standard TTL	low-power Schottky	4000 LOCMOS 5 V	4000 LOCMOS 10 V	4000 LOCMOS 15 V
propagation delay C_L = 15 pF	10 ns	10 ns	40 ns	20 ns	15 ns
flip-flop clock frequency	35 MHz	45 MHz	8 MHz	16 MHz	20 MHz
quiescent power	10 mW	2 mW	10 nW	10 nW	10 nW
noise immunity	1 V	0,8 V	2,25 V	4,5 V	6,75 V
fan-out	10	10	50 *	50 *	50 *

* Or as determined by permissible propagation delay.

Supply voltage range

LOCMOS is guaranteed to function over the unprecedented range of 3 to 15 V supply voltage. Characteristics are guaranteed for 5, 10 and 15 V operation and can be extrapolated for any voltage in between. Operation below 4,5 V is not very meaningful because of the increase in delay (loss of speed), the increase in output impedance and the loss of noise immunity. Operation above 15 V is not recommended because of high dynamic power consumption and risk of noise spikes on the power supply exceeding the breakdown voltage (typ. $>$ 20 V), causing SCR-latch-up and destroying the device unless the current is externally limited.

The lower limit of power supply voltage, including ripple, is determined by the required noise immunity, propagation delay or interface to TTL. The upper limit of supply voltage, including ripple and transients, is determined by power dissipation or direct interface to other logic. The HEF4049B, HEF4050B and HEF4104B provide level transition between TTL and LOCMOS when LOCMOS supply voltages over 5 V are used.

Low static power consumption combined with wide supply voltage range make LOCMOS the ideal logic family for battery-operated equipment.

Power consumption

Under static conditions, the p-channel and the n-channel transistors are not conducting simultaneously, thus only leakage current flows from the positive (V_{DD}) to the negative (V_{SS}) supply connection. This leakage current is typically 0,5 nA per gate, resulting in a very attractive low power consumption of 2,5 nW per gate (at 5 V).

Whenever a LOCMOS circuit is exercised, when data or clock inputs change, additional power is consumed to charge and discharge capacitances (on-chip parasitic capacitances as well as load capacitances). Moreover, there is a short time during the transition when both the p-channel and n-channel transistors are partially conducting. This dynamic power consumption is obviously proportional to the frequency at which the circuit is exercised, to the load capacitance and to the square of the supply voltage. As shown in Fig. 4, the power consumption of a LOCMOS gate exceeds that of a low-power Schottky gate somewhere between 500 kHz and 2 MHz of actual output frequency. Comparing the power consumption of more complex devices (MSI) in various technologies may show a different result.

In any complex design, only a small fraction of the gates actually switch at the full clock frequency, most gates operate at a much lower average rate and therefore consume much less power. A realistic comparison of power consumption between different technologies involves a thorough analysis of the average switching speed of each gate in the circuit.

The maximum values of the quiescent device current (I_{DD}) are given in the Family Specifications, the typical dynamic power dissipation is given in the individual data sheets. The total device power dissipation is the sum of the quiescent and dynamic power dissipation.

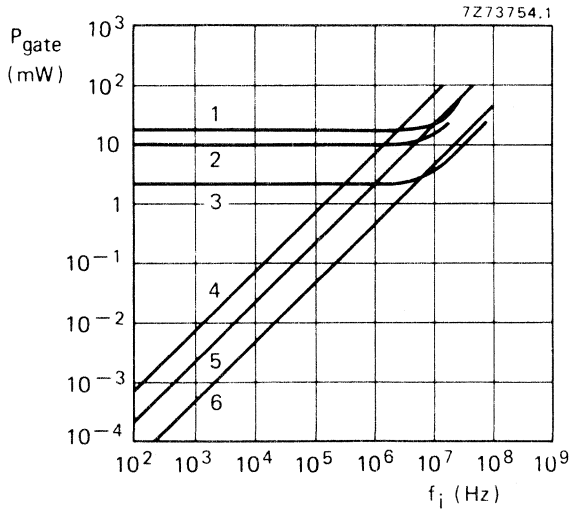


Fig. 4 Typical power dissipation per gate as a function of input frequency for several logic families.

1 Schottky TTL
2 Standard TTL
3 Low-power Schottky
4 LOCMOS (V_{DD} = 15 V)
5 LOCMOS (V_{DD} = 10 V)
6 LOCMOS (V_{DD} = 5 V)

Additional power consumption (due to slow input rise and fall times)

As long as the input voltage of a LOCMOS circuit is below the N-transistor threshold voltage, or higher than the supply voltage minus the P-transistor threshold voltage, one of the input transistors is always in the OFF-state and no 'through' current flows in the input stage.

When the input voltage equals the N-transistor threshold voltage (typ. 1,5 V), the N-transistor starts conducting and a drain current starts to flow.

Figure 5 shows the drain current as a function of the input voltage for a typical LOCMOS input.

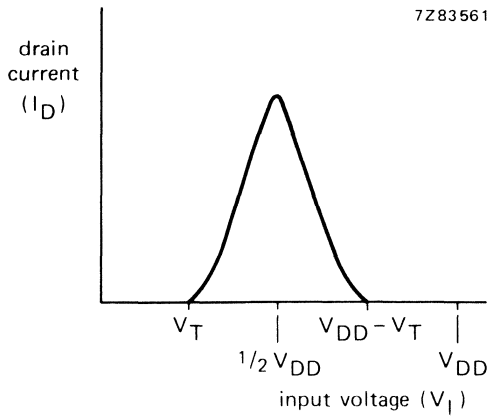


Fig. 5 Drain current as a function of input voltage.

This drain current reaches a maximum at ½ V_{DD} and the peak value depends on the geometrics of the transistors used. This current is proportional to V_{DD}^n, in which $n > 2$.

For Schmitt triggers, unbuffered types, and circuits comprising a single stage inverter, typical current transfer characteristics are given in the device data sheets.

When squarring up slow pulses by means of Schmitt triggers, the through current gives additional power consumption.
By applying RC-oscillators, or oscillators constructed with Schmitt triggers, the phenomenon described gives a frequency-independent power consumption.

Propagation delay

Compared to TTL and LS-TTL, all C-MOS devices are slow and very sensitive to capacitance loading (see Fig. 6).

The HE family uses both advanced processing (LOCMOS) and improved circuit design (buffered gates) to achieve propagation delays and output transition times that are superior to any other junction-isolated C-MOS design.

LOCMOS processing achieves lower parasitic capacitances which reduce the on-chip delay and increase the maximum clock frequency of flip-flops, registers and counters. Buffering all outputs, even on gates, results in lower output impedance and thus reduces the effect of capacitive loading.

Propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

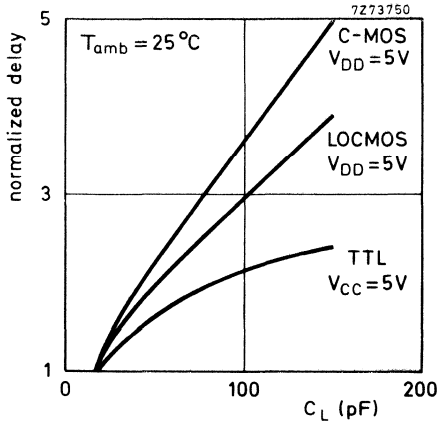


Fig. 6 Normalized propagation delay as a function of load capacitance for TTL, C-MOS and LOCMOS.

Capacitive loading effect

Historically, semiconductor manufacturers have always specified the propagation delay at an output load of 15 pF, not because this was considered a representative systems environment, but rather because it was the lowest practical test-jig capacitance. It also generated the most impressive specifications. For example, TTL with an output impedance in the LOW state of typically 25 Ω is little affected by an increase in capacitive loading. LOCMOS, however, with an output impedance of typically 250 Ω (at 5 V) is 10 times more sensitive to capacitive loading. As an example Fig. 7 shows the positive and negative-going delays as functions of load capacitance for the HEF4011B and Fig. 8 shows the output transition times for standard output stages. For detailed information see Family Specifications and the individual data sheets. It should be noted that most unbuffered gates have an even higher output impedance, a larger dependence on output loading, and do not show the same symmetry.

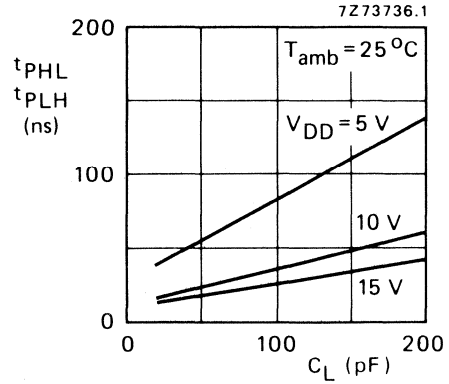


Fig. 7 Positive and negative-going propagation delay as functions of load capacitance for the HEF4011B.

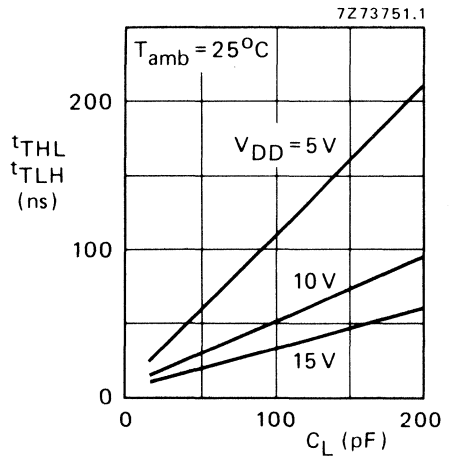


Fig. 8 Output transition times as functions of load capacitance.

Supply voltage effect

1. Speed; Fig. 9 shows propagation delays as functions of supply voltage. The best choice for slow applications is 5 V. For reasonably fast systems, choose 10 or 12 V. Any application requiring 15 V to achieve short delays and fast operation should be investigated for excessive power dissipation and should be weighed against an LS-TTL approach.
2. Noise immunity; improves with higher supply voltage (see NOISE IMMUNITY).

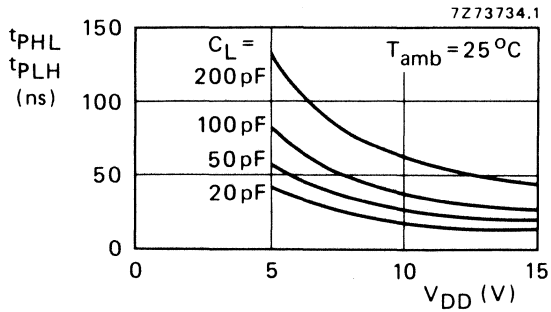


Fig. 9 Propagation delays (symmetrical) as functions of power supply voltage for the HEF4011B.

Temperature effect

The temperature dependence of LOCMOS is much simpler than with TTL, where three factors contribute: increase of beta with temperature, increase of resistor value with temperature, and decrease of junction forward voltage drop with increasing temperature. In LOCMOS, essentially only the carrier mobility changes, thus increasing the impedance, and hence the delay, with temperature. For more details see Family Specifications and the individual data sheets, for example see Fig. 10.

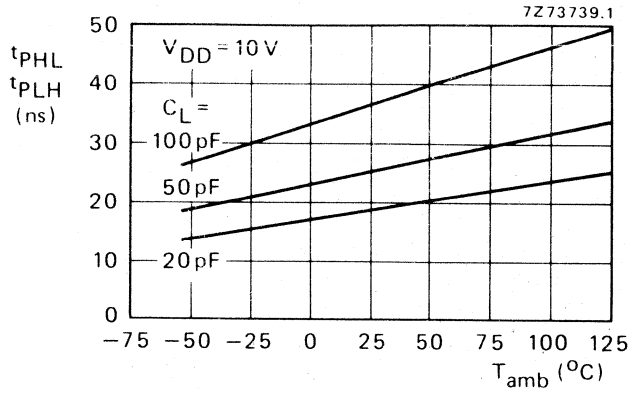


Fig. 10 Propagation delays as functions of ambient temperature, with V_{DD} = 10 V for HEF4011B.

Noise immunity

One of the most advertised and also misunderstood C-MOS features is noise immunity. The input threshold of a C-MOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, LOCMOS can claim very good voltage noise immunity, typically 45% of the supply voltage, i.e., 2,25 V in a 5 V system, 4,5 V in a 10 V system and 6,75 V in a 15 V system. Compare this with the TTL transfer curve in Fig. 11 and its resultant 1 V noise immunity in a lightly loaded system and only 0,4 V worst case. Fig. 12 shows the transfer characteristic between −55 and +125 °C.

Since LOCMOS output impedance, output voltage and input threshold are symmetrical with respect to the supply voltage, the LOW and HIGH level noise immunities are practically equal. Therefore, a LOCMOS system can tolerate ground or V_{DD} drops and noise on these supply lines of more than 1 V, even in a 5 V system. Moreover, the inherent LOCMOS delays act as a noise filter; 10 ns spikes tend to disappear in a chain of LOCMOS gates, but are amplified in a chain of TTL gates. Because of these features, LOCMOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically 'polluted' environment.

Unfortunately these impressive noise margin specifications disregard one important fact: the output impedance of LOCMOS is 3 to 10 times higher than that of TTL. C-MOS interconnections are therefore less 'stiff' and more susceptible to capacitively coupled noise. In terms of such current-injected crosstalk from high noise voltages through small coupling capacitances, the tables on the next page give a comparison between LOCMOS and TTL/LS-TTL.

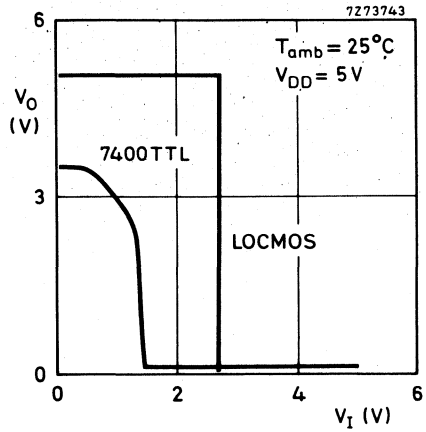


Fig. 11 Typical transfer characteristic for TTL and LOCMOS.

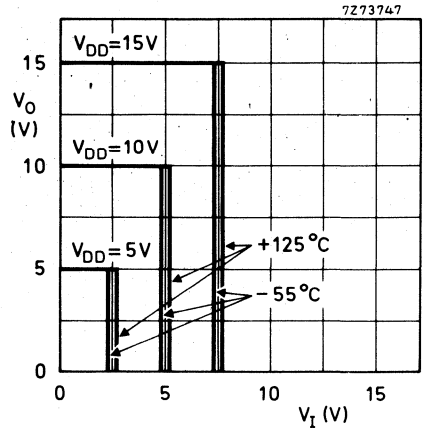


Fig. 12 Voltage transfer characteristic over −55 to + 125 °C range.

LOCMOS/TTL (normalized to TTL)

V_{DD}	5 V	10 V	15 V
factor	0,5	1	2

LOCMOS/LS-TTL (normalized to LS-TTL)

V_{DD}	5 V	10 V	15 V
factor	1	3	5

From the tables can be seen that LOCMOS operating at V_{DD} = 10 V has a dynamic noise immunity which is comparable with TTL and 3 times as good as LS-TTL.

In terms of voltage injected noise the nearly ideal transfer characteristic and the relatively slow response of LOCMOS circuits make them at least 5 times less sensitive to magnetically coupled noise than TTL/LS-TTL.

Input protection

The gate input to any MOS transistor appears like a small value (< 1 pF), very low leakage (< 1 pA) capacitor. Without special precautions, such inputs could be electrostatically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all LOCMOS inputs are protected by a combination of series resistor and shunt diodes. Different manufacturers have different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

With the exception of a few devices, each member of the HE family utilizes a series resistor, nominally 400 Ω, and two diodes, one to V_{DD}, and the other to V_{SS} (see Fig. 13). The resistor is a polysilicon 'true resistor' without a parasitic substrate diode. This ensures that the input impedance is always at least 400 Ω under all biasing conditions, even when V_{DD} is short-circuited to V_{SS}. A parasitic substrate diode would represent a poorly defined shunt to V_{SS} in this particular case.

The diodes exhibit typical forward voltage drops of 0,9 V at 1 mA and reverse breakdown voltages of 20 V. For certain special applications such as oscillators, the diodes actually conduct during normal operation, in this case the current should be limited to 1 mA. Input currents averaging 10 mA or more may destroy the device.

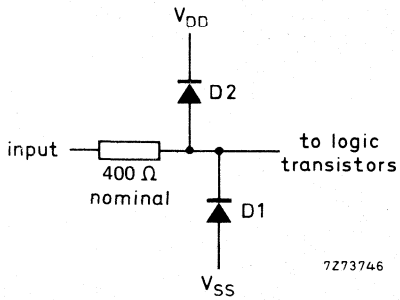


Fig. 13 Standard HE family LOCMOS input protection circuit.

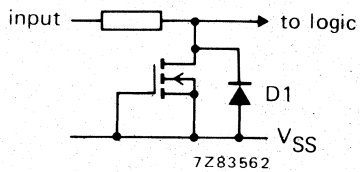


Fig. 14 The input protection for the HEF4049B and HEF4050B.

Figure 14 shows the input protection for the types HEF4049B and HEF4050B. Diode D1 is the inherent drain to V_{SS} diode of the protection device. Under operational conditions, this input may exceed the supply voltage V_{DD}.

Power supply regulation and decoupling

The LOCMOS technology suggests that any supply voltage between 3 and 15 V will do, thus rendering supply voltage regulation unnecessary. However, it must be realized that the supply voltage has influence on the system speed (see Fig. 9), noise immunity (see Figs 11 and 12) and dissipation (see Fig. 4) and see text concerning all these Figures.

Any dynamic system generates voltage spikes on the supply line. These spikes influence the noise immunity, they may damage the circuit, or may have a negative influence on proper operation of the circuit. Therefore a matched decoupling of the supply line is necessary. Generally an electrolytic capacitor of 3 μF per 10 devices is sufficient. However, some circuits require special attention:

1. HEF4511B: BCD to 7-segment latch/decoder/driver; an electrolytic capacitor of 3 μF should be added to each device to avoid excessive voltage spikes due to high di/dt.
2. HEF4528B: dual retriggerable/resettable monostable multivibrator; for circuits of this nature it is recommended to use proper decoupling to avoid pulse length variations due to supply line ripple.
3. Circuits that operate in the linear mode, such as RC or crystal oscillators, a minimum supply voltage of at least 4 V is recommmended.

3-state outputs

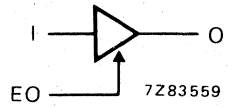


Fig. 15 Logic symbol of a 3-state output.

Function table

inputs		output
I	EO	O
X	L	Z
L	H	L
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance OFF-state

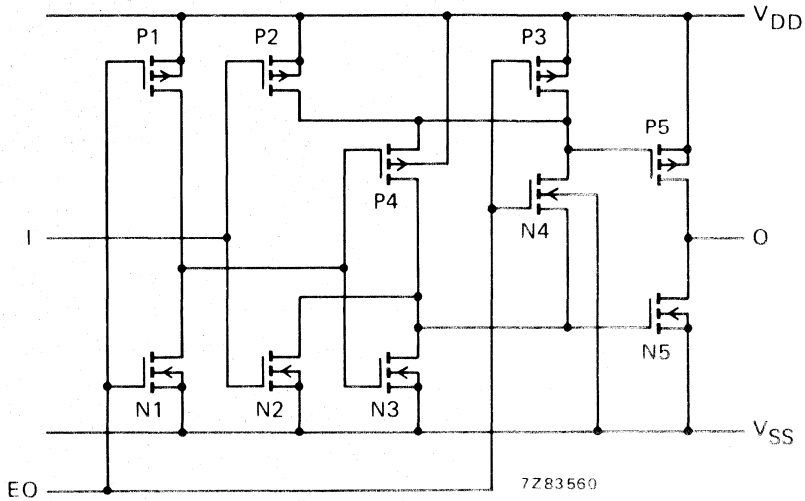


Fig. 16 Circuit diagram of 3-state output.

When EO is HIGH, the output is enabled and the transistors P4 and N4 act as a transmission gate, and they connect the gates of the output transistors together. A LOW level at EO puts the output in the high impedance OFF-state; transistors P3 and N3 function as pull-up and pull-down transistors respectively.

FAMILY SPECIFICATIONS

These specifications cover the common electrical characteristics of the entire HE4000B family, unless otherwise specified in the individual device data sheet.

The LOCMOS HE4000B family devices will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} of 5, 10 and 15 V. Because of the wide operating voltage range, power supply regulation is less critical than with other types of logic. The lower limit of the supply voltage is 3 V, or as determined by required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 15 V or as determined by power dissipation constraints or interface to other logic. Unused inputs must be connected to V_{DD}, V_{SS} or another input. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to + 18	V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5	V
DC current into any input or output	± I	max. 10	mA
Power dissipation per package:			
HEF (plastic and ceramic DIL)			
T_{amb} = −40 to + 70 °C	P_{tot}	max. 500	W
T_{amb} = + 70 to + 85 °C		derate linearly with 8 mW/K	
HEF (plastic SO mini-pack)			
T_{amb} = −40 to + 70 °C	P_{tot}	max. 400	W
T_{amb} = + 70 to + 85 °C		derate linearly with 6 mW/K	
HEC (ceramic DIL)			
T_{amb} = −55 to + 70 °C	P_{tot}	max. 500	W
T_{amb} = + 70 to + 125 °C		derate linearly with 8 mW/K	←
Power dissipation per output	P	max. 100	mW
Storage temperature	T_{stg}	−65 to + 150	°C
Operating ambient temperature (HEF)	T_{amb}	−40 to + 85	°C
Operating ambient temperature (HEC)	T_{amb}	−55 to + 125 °C	←

D.C. CHARACTERISTICS FOR HEF V_{SS} = 0 V; for all devices unless otherwise specified

parameter	V_{DD} V	symbol	T_{amb} (°C)						unit	conditions
			−40		+ 25		+ 85			
			min.	max.	min.	max.	min.	max.		
Quiescent device current										
	5		–	1,0	–	1,0	–	7,5	μA	
gates	10	I_{DD}	–	2,0	–	2,0	–	15,0	μA	
	15		–	4,0	–	4,0	–	30,0	μA	
	5		–	4,0	–	4,0	–	30	μA	
buffers, flip-flops	10	I_{DD}	–	8,0	–	8,0	–	60	μA	
	15		–	16,0	–	16,0	–	120	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}; $I_O = 0$
	5		–	20	–	20	–	150	μA	
MSI	10	I_{DD}	–	40	–	40	–	300	μA	
	15		–	80	–	80	–	600	μA	
	5		–	50	–	50	–	375	μA	
LSI	10	I_{DD}	–	100	–	100	–	750	μA	
	15		–	200	–	200	–	1500	μA	
	5		–	0,05	–	0,05	–	0,05	V	
Output voltage LOW	10	V_{OL}	–	0,05	–	0,05	–	0,05	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1\ \mu A$
	15		–	0,05	–	0,05	–	0,05	V	
	5		4,95	–	4,95	–	4,95	–	V	
Output voltage HIGH	10	V_{OH}	9,95	–	9,95	–	9,95	–	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1\ \mu A$
	15		14,95	–	14,95	–	14,95	–	V	
	5		–	1,5	–	1,5	–	1,5	V	V_O = 0,5 V or 4,5 V
Input voltage LOW	10	V_{IL}	–	3,0	–	3,0	–	3,0	V	V_O = 1,0 V or 9,0 V
(buffered stages only)	15		–	4,0	–	4,0	–	4,0	V	V_O = 1,5 V or 13,5 V; $\lvert I_O \rvert < 1\ \mu A$
	5		3,5	–	3,5	–	3,5	–	V	V_O = 0,5 V or 4,5 V
Input voltage HIGH	10	V_{IH}	7,0	–	7,0	–	7,0	–	V	V_O = 1,0 V or 9,0 V
(buffered stages only)	15		11,0	–	11,0	–	11,0	–	V	V_O = 1,5 V or 13,5 V; $\lvert I_O \rvert < 1\ \mu A$

D.C. CHARACTERISTICS FOR HEF (continued) V_{SS} = 0 V; for all devices unless otherwise specified

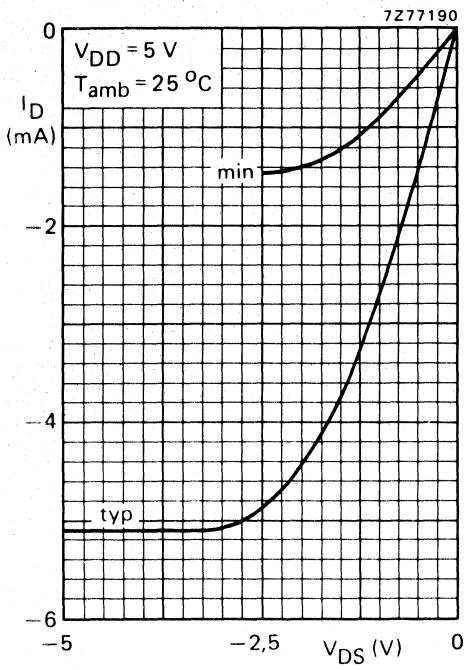
parameter	V_{DD} V	symbol	T_{amb} (°C)						unit	conditions
			−40		+ 25		+ 85			
			min.	max.	min.	max.	min.	max.		
Input voltage LOW	5		–	1	–	1	–	1	V	V_O = 0,5 V or 4,5 V |
(unbuffered stages	10	V_{IL}	–	2	–	2	–	2	V	V_O = 1,0 V or 9,0 V | $\|I_O\| < 1\ \mu A$
only)	15		–	2,5	–	2,5	–	2,5	V	V_O = 1,5 V or 13,5 V |
Input voltage HIGH	5		4	–	4	–	4	–	V	V_O = 0,5 V or 4,5 V |
(unbuffered stages	10	V_{IH}	8	–	8	–	8	–	V	V_O = 1,0 V or 9,0 V | $\|I_O\| < 1\ \mu A$
only)	15		12,5	–	12,5	–	12,5	–	V	V_O = 1,5 V or 13,5 V |
Output (sink)	5		0,52	–	0,44	–	0,36	–	mA	V_O = 0,4 V; V_I = 0 or 5 V
current LOW	10	I_{OL}	1,3	–	1,1	–	0,9	–	mA	V_O = 0,5 V; V_I = 0 or 10 V
	15		3,6	–	3,0	–	2,4	–	mA	V_O = 1,5 V; V_I = 0 or 15 V
Output (source)	5		0,52	–	0,44	–	0,36	–	mA	V_O = 4,6 V; V_I = 0 or 5 V
current HIGH	10	$-I_{OH}$	1,3	–	1,1	–	0,9	–	mA	V_O = 9,5 V; V_I = 0 or 10 V
	15		3,6	–	3,0	–	2,4	–	mA	V_O = 13,5 V; V_I = 0 or 15 V
Output (source) current HIGH	5	$-I_{OH}$	1,7	–	1,4	–	1,1	–	mA	V_O = 2,5 V; V_I = 0 or 5 V
Input leakage current	15	$\pm I_{IN}$	–	0,3	–	0,3	–	1,0	μA	V_I = 0 or 15 V
3-state output leakage current; HIGH	15	I_{OZH}	–	1,6	–	1,6	–	12,0	μA	output returned to V_{DD}
3-state output leakage current; LOW	15	$-I_{OZL}$	–	1,6	–	1,6	–	12,0	μA	output returned to V_{SS}

D.C. CHARACTERISTICS FOR HEC V_{SS} = 0 V; for all devices unless otherwise specified

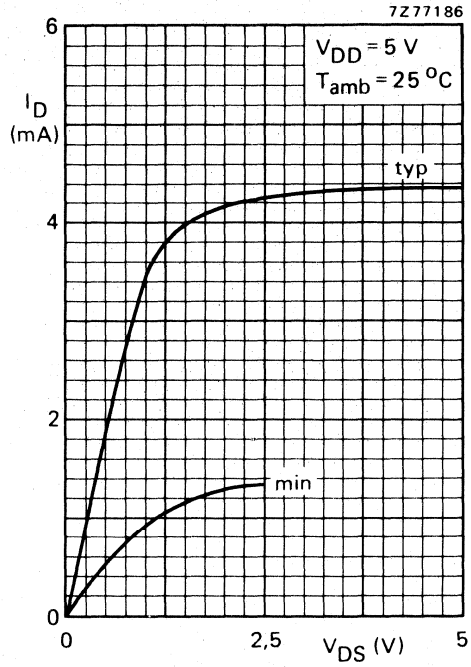
parameter	V_{DD} V	symbol	T_{amb} (°C) –55 min.	–55 max.	+ 25 min.	+ 25 max.	+ 125 min.	+ 125 max.	unit	conditions
Quiescent device current										
	5		–	0,25	–	0,25	–	7,5	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}; I_O = 0
gates	10	I_{DD}	–	0,5	–	0,5	–	15,0	μA	
	15		–	1,0	–	1,0	–	30,0	μA	
	5		–	1,0	–	1,0	–	30	μA	
buffers, flip-flops	10	I_{DD}	–	2,0	–	2,0	–	60	μA	
	15		–	4,0	–	4,0	–	120	μA	
	5		–	5,0	–	5,0	–	150	μA	
MSI	10	I_{DD}	–	10,0	–	10,0	–	300	μA	
	15		–	20,0	–	20,0	–	600	μA	
	5		–	15	–	15	–	375	μA	
LSI	10	I_{DD}	–	25	–	25	–	750	μA	
	15		–	50	–	50	–	1500	μA	
	5		–	0,05	–	0,05	–	0,05	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA
Output voltage LOW	10	V_{OL}	–	0,05	–	0,05	–	0,05	V	
	15		–	0,05	–	0,05	–	0,05	V	
	5		4,95	–	4,95	–	4,95	–	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA
Output voltage HIGH	10	V_{OH}	9,95	–	9,95	–	9,95	–	V	
	15		14,95	–	14,95	–	14,95	–	V	
	5		–	1,5	–	1,5	–	1,5	V	V_O = 0,5 V or 4,5 V; $\lvert I_O \rvert < 1$ μA
Input voltage LOW	10	V_{IL}	–	3,0	–	3,0	–	3,0	V	V_O = 1,0 V or 9,0 V; $\lvert I_O \rvert < 1$ μA
(buffered stages only)	15		–	4,0	–	4,0	–	4,0	V	V_O = 1,5 V or 13,5 V; $\lvert I_O \rvert < 1$ μA
	5		3,5	–	3,5	–	3,5	–	V	V_O = 0,5 V or 4,5 V; $\lvert I_O \rvert < 1$ μA
Input voltage HIGH	10	V_{IH}	7,0	–	7,0	–	7,0	–	V	V_O = 1,0 V or 9,0 V; $\lvert I_O \rvert < 1$ μA
(buffered stages only)	15		11,0	–	11,0	–	11,0	–	V	V_O = 1,5 V or 13,5 V; $\lvert I_O \rvert < 1$ μA

D.C. CHARACTERISTICS FOR HEC (continued) V_{SS} = 0 V; for all devices unless otherwise specified

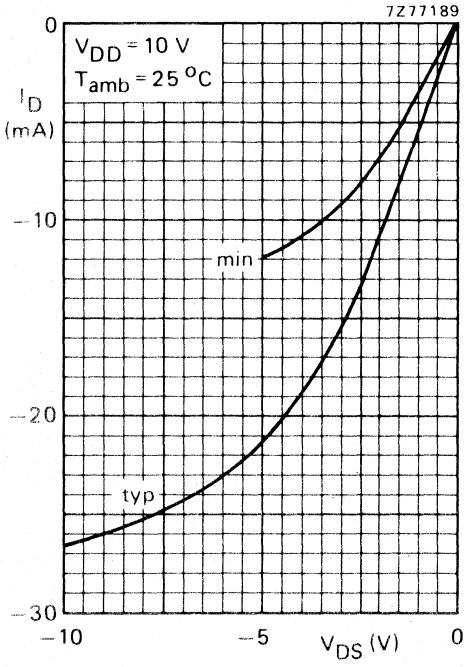
parameter	V_{DD} V	symbol	T_{amb} (°C)						unit	conditions
			−55		+ 25		+ 125			
			min.	max.	min.	max.	min.	max.		
Input voltage LOW	5		–	1	–	1	–	1	V	V_O = 0,5 V or 4,5 V
(unbuffered stages	10	V_{IL}	–	2	–	2	–	2	V	V_O = 1,0 V or 9,0 V } $\lvert I_O \rvert < 1\ \mu A$
only)	15		–	2,5	–	2,5	–	2,5	V	V_O = 1,5 V or 13,5 V
Input voltage HIGH	5		4	–	4	–	4	–	V	V_O = 0,5 V or 4,5 V
unbuffered stages	10	V_{IH}	8	–	8	–	8	–	V	V_O = 1,0 V or 9,0 V } $\lvert I_O \rvert < 1\ \mu A$
only)	15		12,5	–	12,5	–	12,5	–	V	V_O = 1,5 V or 13,5 V
Output (sink)	5		0,64	–	0,5	–	0,36	–	mA	V_O = 0,4 V; V_I = 0 or 5 V
current LOW	10	I_{OL}	1,6	–	1,3	–	0,9	–	mA	V_O = 0,5 V; V_I = 0 or 10 V
	15		4,2	–	3,4	–	2,4	–	mA	V_O = 1,5 V; V_I = 0 or 15 V
Output (source)	5		0,64	–	0,5	–	0,36	–	mA	V_O = 4,6 V; V_I = 0 or 5 V
current HIGH	10	$-I_{OH}$	1,6	–	1,3	–	0,9	–	mA	V_O = 9,5 V; V_I = 0 or 10 V
	15		4,2	–	3,4	–	2,4	–	mA	V_O = 13,5 V; V_I = 0 or 15 V
Output (source) current HIGH	5	$-I_{OH}$	1,7	–	1,4	–	1,1	–	mA	V_O = 2,5 V; V_I = 0 or 5 V
Input leakage current	15	$\pm I_{IN}$	–	0,1	–	0,1	–	1,0	μA	V_I = 0 or 15 V
3-state output leakage current; HIGH	15	I_{OZH}	–	0,4	–	0,4	–	12,0	μA	output returned to V_{DD}
3-state output leakage current; LOW	15	$-I_{OZL}$	–	0,4	–	0,4	–	12,0	μA	output returned to V_{SS}



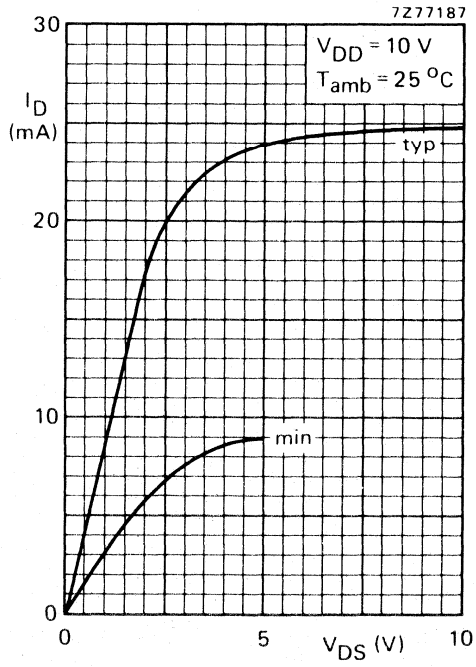
P-channel drain characteristics (source)



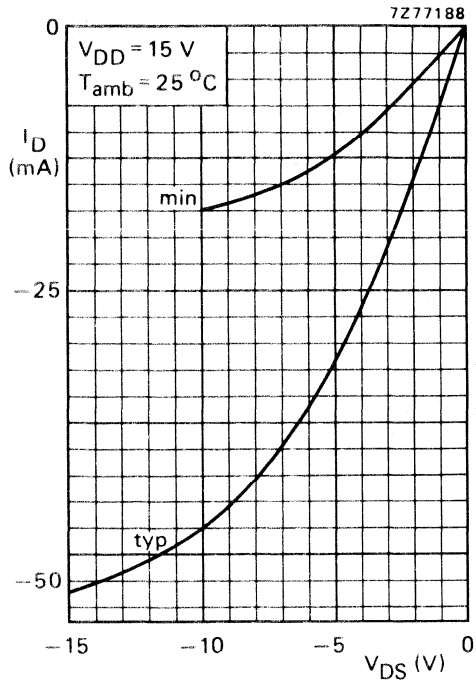
N-channel drain characteristics (sink)



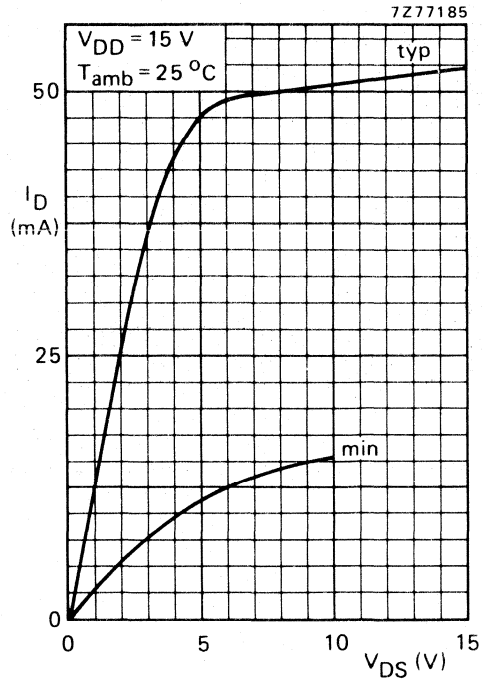
P-channel drain characteristics (source)



N-channel drain characteristics (sink)



P-channel drain characteristics (source)



N-channel drain characteristics (sink)

Note

Temperature coefficient: −0,4%/°C.

A.C. CHARACTERISTICS

Clock input rise and fall times (t_r, t_f)

The upper limits on t_r and t_f vary widely from device to device and with supply voltage. Unless otherwise specified in the individual data sheets it is recommended that input rise and fall times be less than 15 μs for V_{DD} = 5 V; 4 μs for V_{DD} = 10 V; 1 μs for V_{DD} = 15 V.

Output transition times (t_{TLH}, t_{THL})

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times $\leqslant$ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

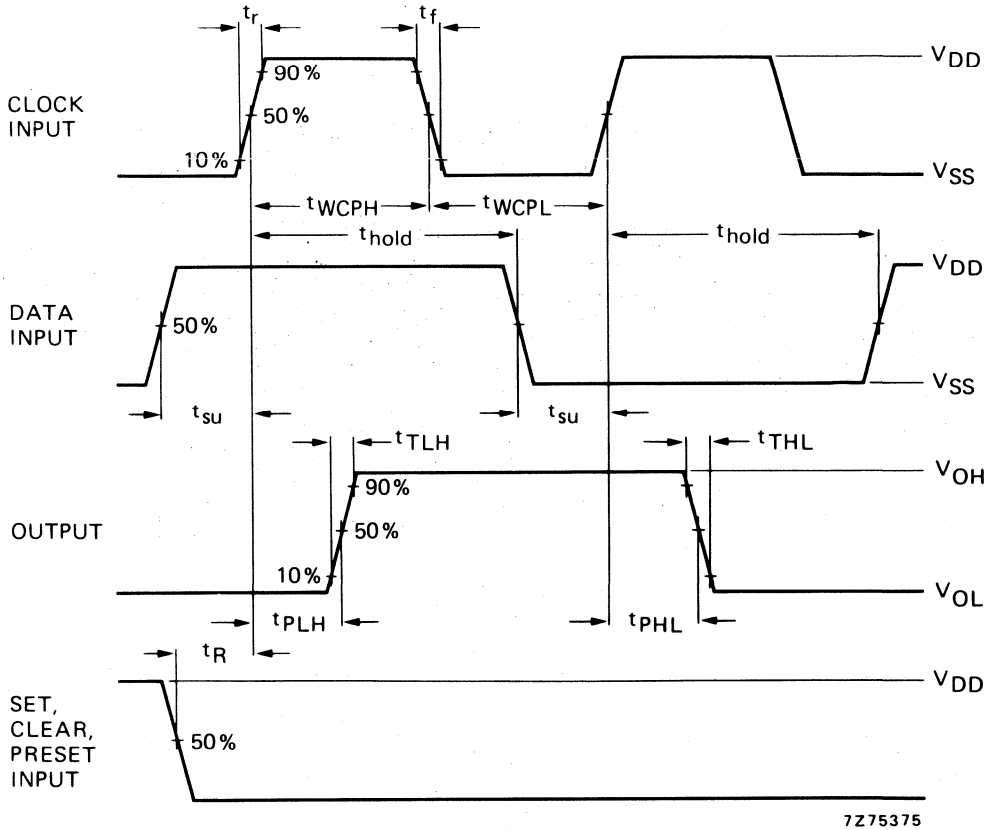
Temperature coefficient (typical values)

Propagation delays	+0,35%/°C
Output transition times	+0,35%/°C

Input capacitance (digital inputs)

Maximum input capacitance C_I = 7,5 pF.

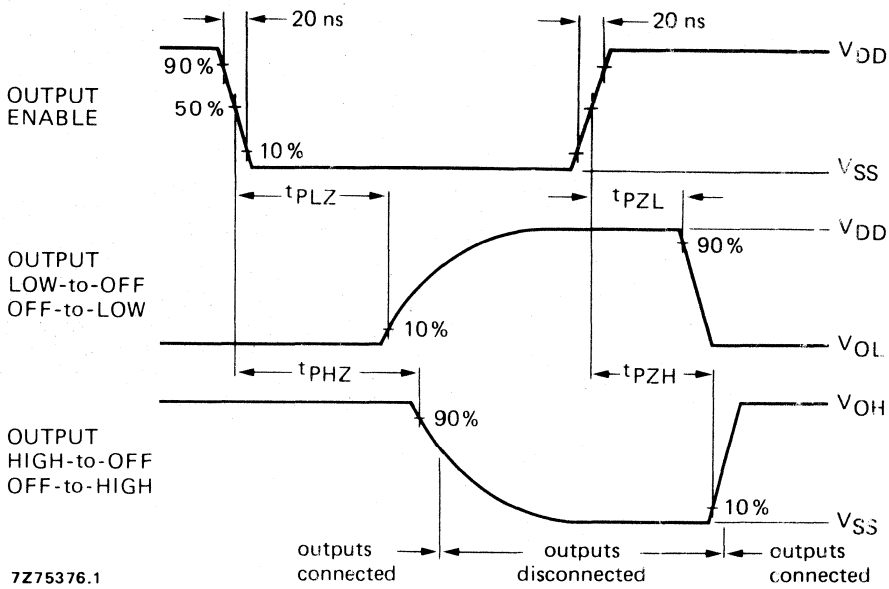
Set-up times, hold times, recovery times and propagation delays for sequential logic circuits.



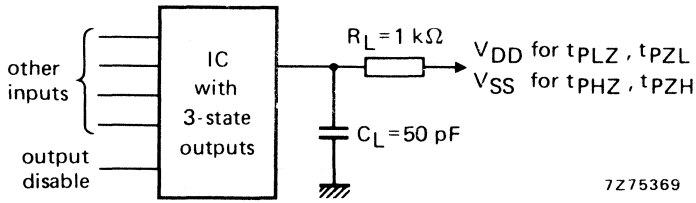
Note

In the waveforms above the active transition of the clock input is going from LOW to HIGH and the active level of the forcing signals (SET, CLEAR and PRESET) is HIGH.
The actual direction of the active transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.

Propagation delays of 3-state outputs.



Test circuit of 3-state output ICs.



DEFINITION OF SYMBOLS AND TERMS USED IN DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{IN} Input current; the current flowing into a device at specified input voltage and V_{DD}.

I_{OH} Output current HIGH; the drive current flowing out of the device at specified HIGH output voltage and V_{DD}.

I_{OL} Output current LOW; the drive current flowing into a device at specified LOW output voltage and V_{DD}.

I_{DD} Quiescent power supply current; the current flowing into the V_{DD} lead at specified input and V_{DD} conditions.

I_{OZ} Output OFF current; the leakage current flowing into or out of the output of a 3-state device in the OFF state when the output is connected to V_{DD} or V_{SS}.

I_{IL} Input current LOW; the current flowing into a device at a specified LOW level input voltage and a specified V_{DD}.

I_{IH} Input current HIGH; the current flowing into a device at a specified HIGH level input voltage and a specified V_{DD}.

I_{DDL} Quiescent power supply current LOW; the current flowing into the V_{DD} lead with a specified LOW level input voltage on all inputs and specified V_{DD} conditions.

I_{DDH} Quiescent power supply current HIGH; the current flowing into the V_{DD} lead with a specified HIGH level input voltage on all inputs and specified V_{DD} conditions.

I_Z OFF state leakage current; the leakage current flowing into the output of a 3-state device in the OFF state at a specified output voltage and V_{DD}.

Voltages

All voltages are referenced to V_{SS}, which is the most negative potential applied to the device.

V_{DD} Supply voltage; the most positive potential on the device.

V_{SS} Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{EE} Supply voltage; one of two (V_{SS} and V_{EE}) negative power supplies. For a device with dual negative power supply, the most negative power supply as a reference level for other voltages.

V_{IH} Input voltage HIGH; the range of input voltages that represents a logic HIGH level in the system.

V_{IL} Input voltage LOW; the range of input voltages that represents a logic LOW level in the system.

V_{OH} Output voltage HIGH; the range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} Output voltage LOW; the range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_P Trigger threshold voltage; positive-going signal.

V_N Trigger threshold voltage; negative-going signal.

Analogue terms

R_{ON} ON resistance; the effective ON state resistance of an analogue transmission gate, at specified input voltage, output load and V_{DD}.

ΔR_{ON} ΔON resistance; the difference in effective ON resistance between any two transmission gates of an analogue device at specified input voltage, output load and V_{DD}.

A.C. switching parameters

f_i Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device truth table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

f_o Output frequency; each output.

f_{max} Clock frequency; clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

t_r, t_f Clock input rise and fall times; 10% to 90% value.

t_{PLH} Propagation delay time; the time between the specified reference points, normally 50% points on the input and output waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation delay time; the time between the specified reference points, normally 50% points on the input and output waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_{TLH} Transition time, LOW-to-HIGH; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW to HIGH.

t_{THL} Transition time, HIGH-to-LOW; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH to LOW.

t_W Pulse width; the time between 50% amplitude points on the leading and trailing edges of pulse.

t_{hold} Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_{su} Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} 3-state output disable time, HIGH to Z; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0,1 V_{OH} drop on the output voltage waveform of a 3-state device, with the output changing from the output HIGH level (V_{OH}) to a high impedance OFF-state.

t_{PLZ} 3-state output disable time, LOW to Z; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0,1 ($V_{DD}-V_{OL}$) rise on the output voltage waveform of a 3-state device, with the output changing from the output LOW level (V_{OL}) to a high impedance OFF-state.

t_{PZH} 3-state output enable time, Z to HIGH; the time between the specified reference points, normally 50% point on the output enable input voltage waveform and a point representing 0,1 V_{OH} voltage rise on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state to the output HIGH level (V_{OH}).

t_{PZL} 3-state output enable time, Z to LOW; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing 0,1 ($V_{DD}-V_{OL}$) voltage drop on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state to the output LOW level (V_{OL}).

t_R Recovery time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at 50% points on both input voltage waveforms.

DEVICE DATA

DUAL 3-INPUT NOR GATE AND INVERTER

The HEF4000B provides the positive dual 3-input NOR function. A single stage inverting function with standard output performance is also accomplished. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

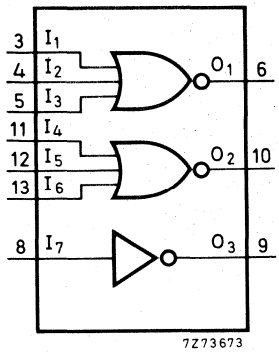


Fig. 1 Functional diagram.

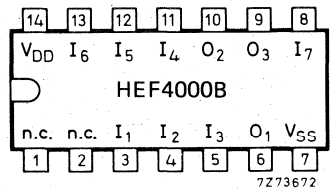


Fig. 2 Pinning diagram.

HEF4000BP : 14-lead DIL; plastic (SOT-27).
HEF4000BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4000BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

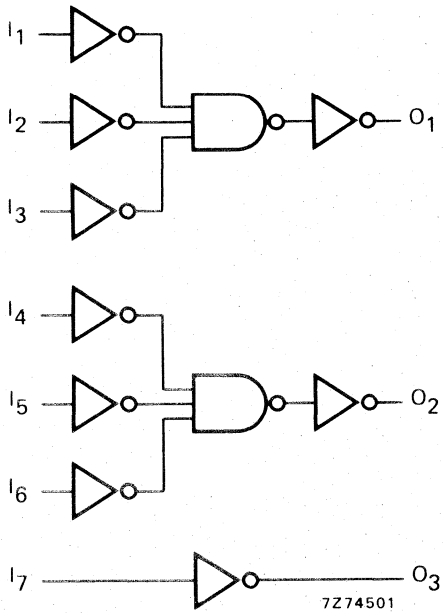


Fig. 3 Logic diagram.

FAMILY DATA | see Family Specifications

I_{DD} LIMITS category GATES

D.C. CHARACTERISTICS

For the single inverter stage (I_7/O_3):

see Family Specifications for input voltages HIGH and LOW (unbuffered stages only).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays	5		70	140	ns	43 ns + (0,55 ns/pF) C_L
I_1 to I_6 → O_1,O_2	10	t_{PHL}; t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5		45	90	ns	18 ns + (0,55 ns/pF) C_L
I_7 → O_3	10	t_{PHL}; t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
(unbuffered output)	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 000 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	7 700 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	
	15	28 700 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	

APPLICATION INFORMATION

The following information (Figs 4 to 7) is only for the single inverter stage (I_7/O_3).

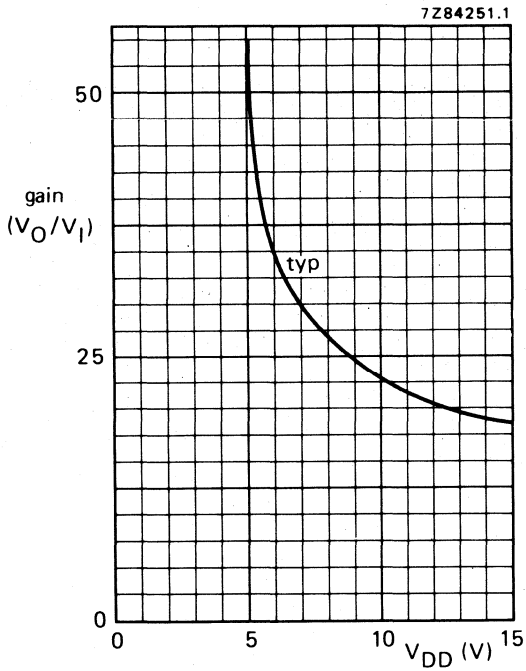


Fig. 4 Voltage gain (V_O/V_I) as a function of supply voltage.

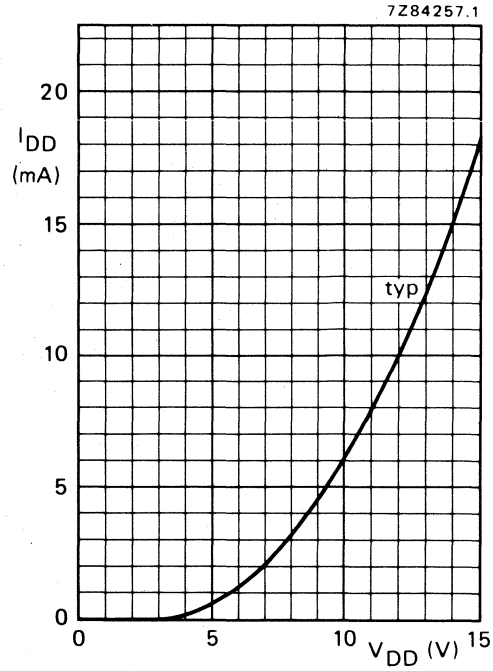


Fig. 5 Supply current as a function of supply voltage.

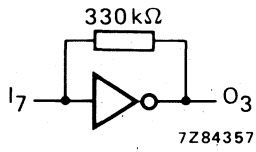


Fig. 6 Test set-up for measuring graphs of Figs 4 and 5.
This is also an example of an analogue amplifier using the single inverter stage (I_7/O_3) of the HEF4000B.

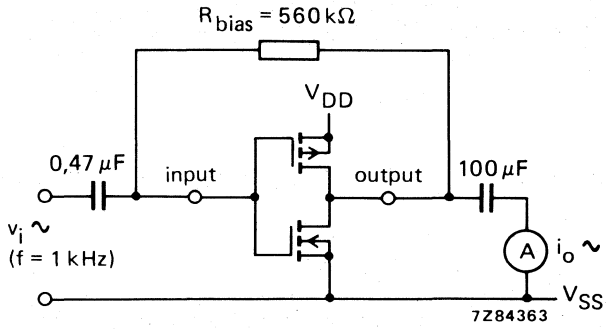
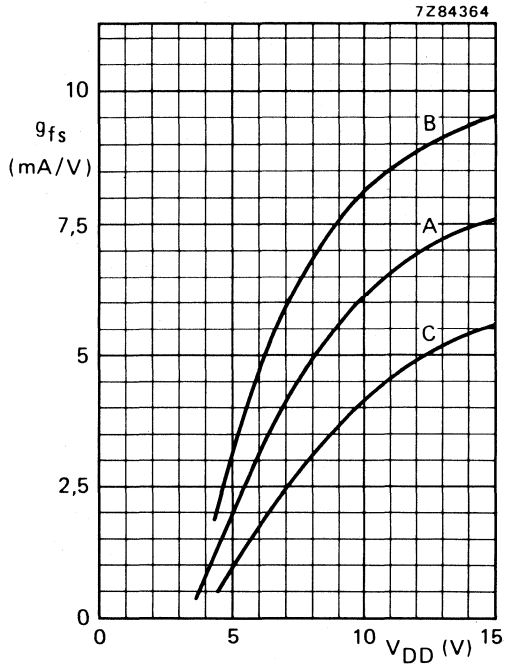


Fig. 7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 8).



Curves in Fig. 8:

A: average
B: average + 2 s,
C: average −2 s, in where:
's' is the observed standard deviation.

Fig. 8 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

QUADRUPLE 2-INPUT NOR GATE

The HEF4001B provides the positive quadruple 2-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

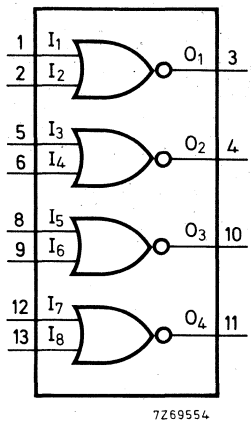


Fig. 1 Functional diagram.

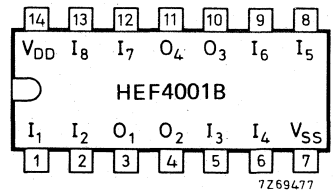


Fig. 2 Pinning diagram.

HEF4001BP : 14-lead DIL; plastic (SOT-27).
HEF4001BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4001BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

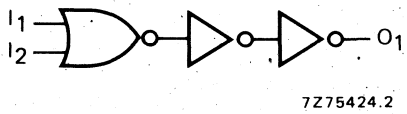


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		60	120	ns	33 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		50	100	ns	23 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	45	ns	14 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	14 200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

QUADRUPLE 2-INPUT NOR GATE

The HEF4001UB is a quadruple 2-input NOR gate. This unbuffered single stage version provides a direct implementation of the NOR function. The output impedance and output transition time depends on the input voltage and input rise and fall times applied.

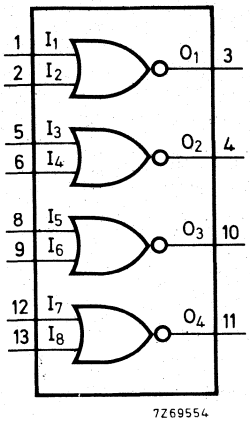


Fig. 1 Functional diagram.

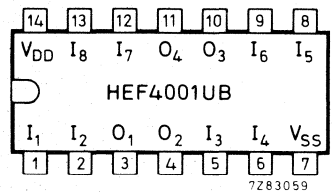


Fig. 2 Pinning diagram.

HEF4001UBP : 14-lead DIL; plastic (SOT-27).
HEF4001UBD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4001UBT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

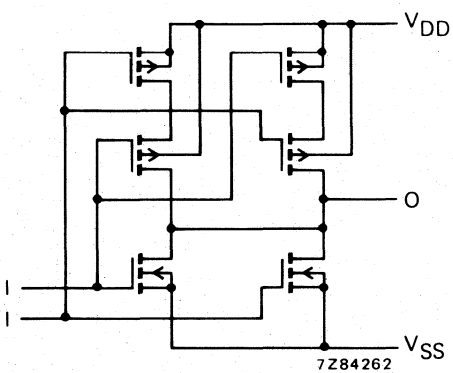


Fig. 3 Schematic diagram (one gate). The splitting-up of the p-transistors provide identical inputs.

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications for V_{IH}/V_{IL} unbuffered stages

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		65	130	ns	30 ns + (0,70 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	17 ns + (0,27 ns/pF) C_L
	15		25	50	ns	15 ns + (0,20 ns/pF) C_L
	5		40	80	ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times	5		75	150	ns	15 ns + (1,20 ns/pF) C_L
	10	t_{THL}	30	60	ns	6 ns + (0,48 ns/pF) C_L
HIGH to LOW	15		20	40	ns	4 ns + (0,32 ns/pF) C_L
	5		60	110	ns	10 ns + (1,00 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
Input capacitance		C_{IN}	–	10	pF	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$30\ 000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

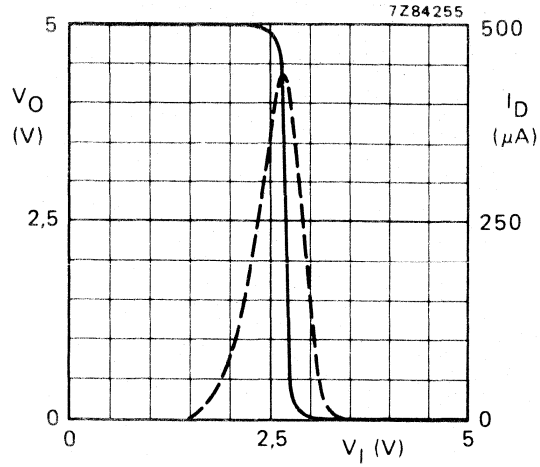


Fig. 4 Typical transfer characteristics; one input, the other input connected to V_{SS}; —— V_O; – – – I_D(drain current); $I_O = 0$; $V_{DD} = 5$ V.

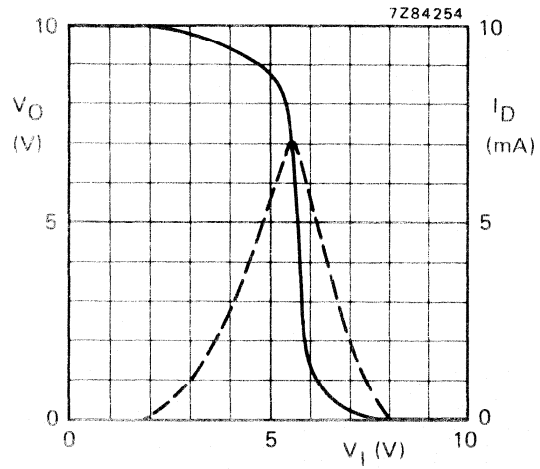


Fig. 5 Typical transfer characteristics; one input, the other input connected to V_{SS}; —— V_O; – – – I_D(drain current); $I_O = 0$; $V_{DD} = 10$ V.

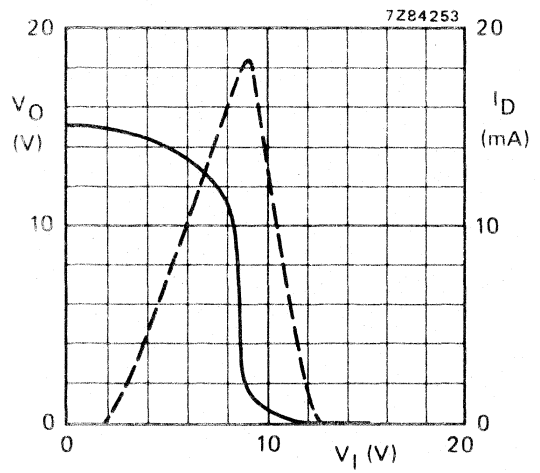


Fig. 6 Typical transfer characteristics; one input, the other input connected to V_{SS}; —— V_O; – – – I_D(drain current); $I_O = 0$; $V_{DD} = 15$ V.

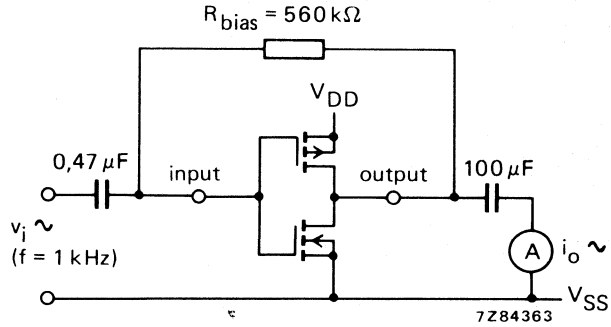
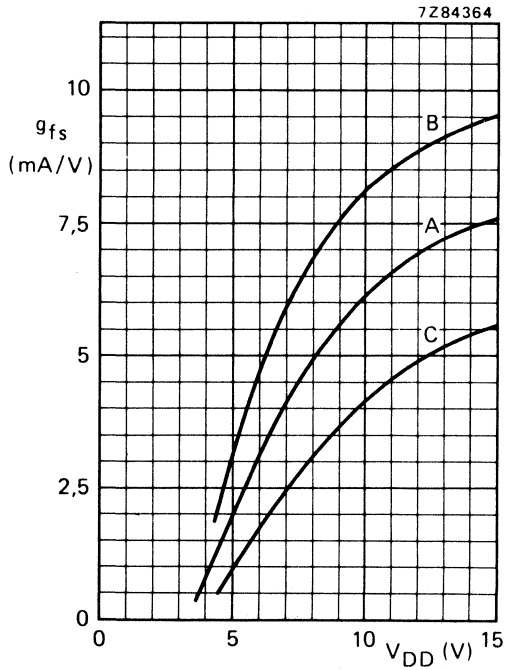


Fig. 7 Test set-up for measuring foward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 8).



Curves in Fig. 8:

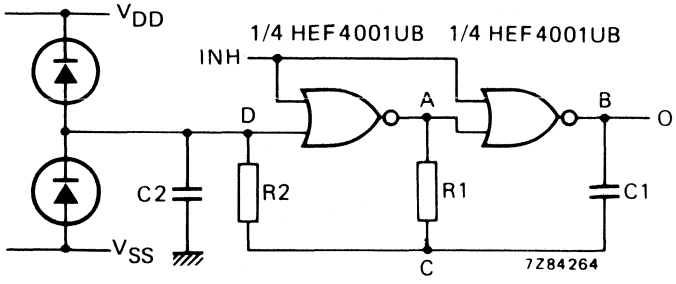
A : average,
B : average + 2 s,
C : average −2 s, in where:
's' is the observed standard deviation.

Fig. 8 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

APPLICATION INFORMATION

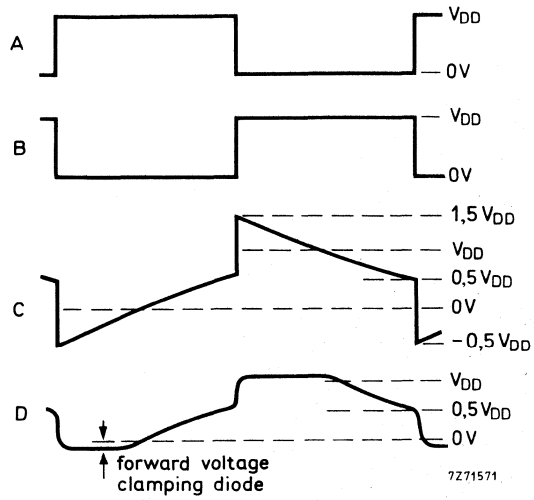
Some examples of applications for the HEF4001UB are shown below.

Because of the fact that this circuit is unbuffered, it is suitable for use in (partly) analogue circuits.



INH	O
H	L
L	OSC

(a)



(b)

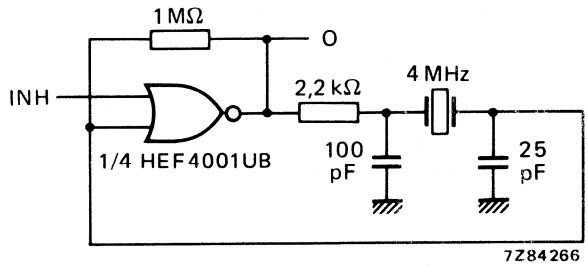
Fig. 9(a) Astable relaxation oscillator using two HEF4001UB gates; the diodes may be BAW62; C2 is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

In Fig. 9 the oscillation frequency is mainly determined by R1C1, provided $R1 << R2$ and $R2C2 << R1C1$.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \text{ and } T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \text{ where}$$

V_{ST} is the signal threshold level of the gate. The period is fairly independent of V_{DD}, V_{ST} and temperature. The duty factor, however, is influenced by V_{ST}.



INH	O
H	L
L	OSC

Fig. 10 Example of a crystal oscillator using one HEF4001UB gate.

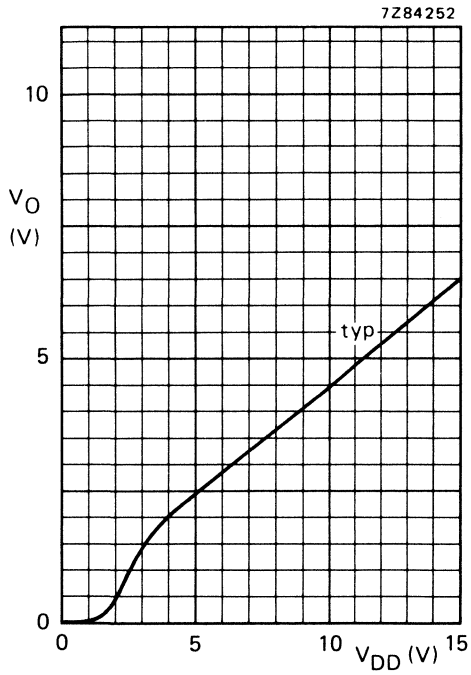


Fig. 11 Output voltages as a function of supply voltage.

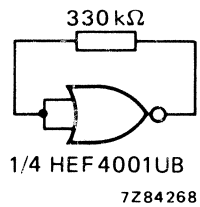


Fig. 12 Test set-up for measuring graph of Fig. 11. Condition: all other inputs connected to ground.

NOTES

If a gate is just used as an amplifying inverter, there are two possibilities:

a. Connecting the inputs together gives simpler wiring, but makes the device output not completely symmetrical.
b. Connecting one input to V_{SS} will give the device a symmetrical output.

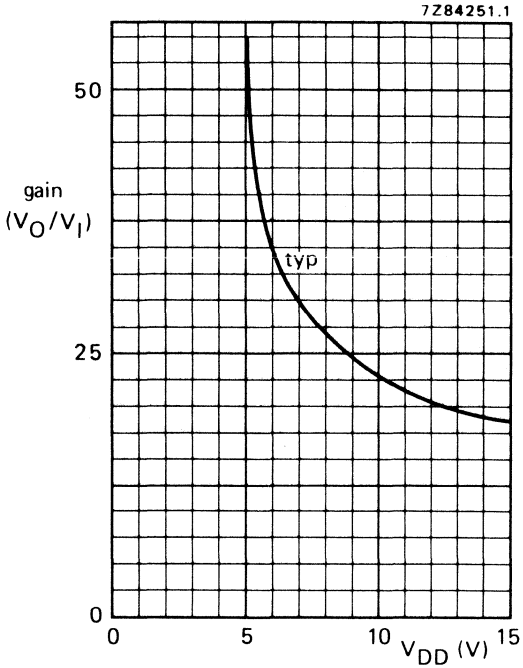


Fig. 13 Voltage gain (V_O/V_I) as a function of supply voltage.

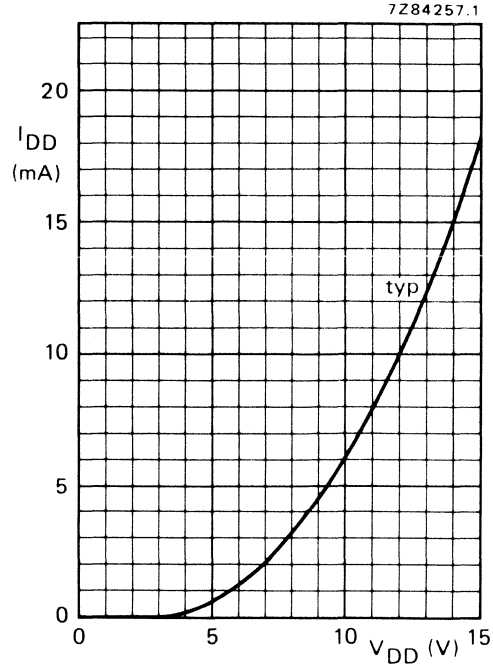


Fig. 14 Supply current as a function of supply voltage.

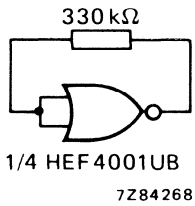


Fig. 15 Test set-up for measuring graphs of Figs 13 and 14. Condition: all other inputs connected to ground.

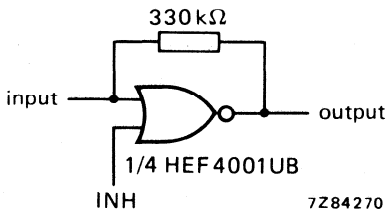


Fig. 16 Example of an analogue amplifier with inhibit using one HEF4001UB gate.

DUAL 4-INPUT NOR GATE

The HEF4002B provides the positive dual 4-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

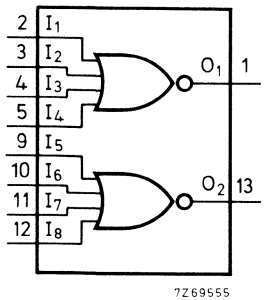


Fig. 1 Functional diagram.

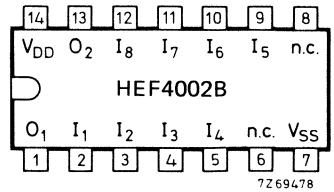


Fig. 2 Pinning diagram.

HEF4002BP : 14-lead DIL; plastic (SOT-27).
HEF4002BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4002BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

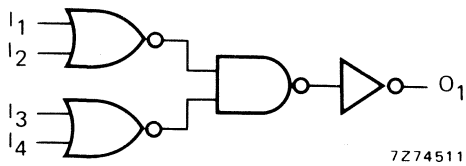


Fig. 3 Logic diagram (one gate).

FAMILY DATA | see Family Specifications

I_{DD} LIMITS category GATES

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays	5		60	120	ns	33 ns + (0,55 ns/pF) C_L
$I_n \longrightarrow O_n$	10	t_{PHL}; t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1050 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4300 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	11 700 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

18-STAGE STATIC SHIFT REGISTER

The HEF4006B is an 18-stage shift register arranged as two 4-stage and two 5-stage shift registers with a common clock input ($\overline{CP}$). The two 4-stage shift registers each have a data input (D_A, D_B) and a data output (O_{3A}, O_{3B}); the two 5-stage shift registers each have a data input (D_C, D_D) and data outputs from the fourth and fifth stages (O_{3C}, O_{4C}, O_{3D}, O_{4D}).

The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data are shifted into the first register position of each register from the data inputs (D_A to D_D) and all the data in each register are shifted one position to the right on the HIGH to LOW transition of $\overline{CP}$.

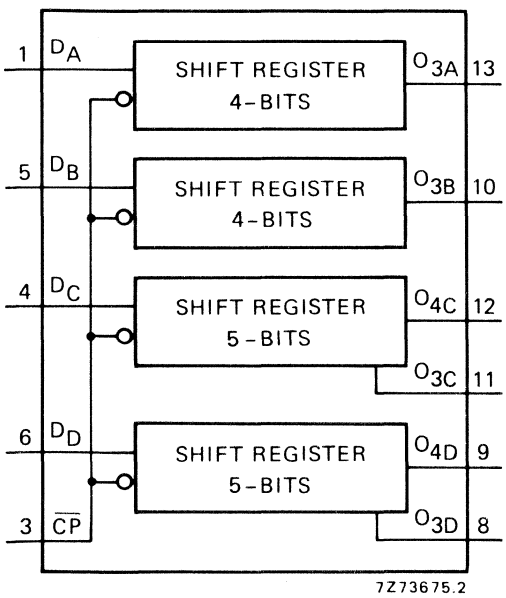


Fig. 1 Functional diagram.

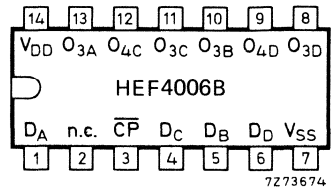


Fig. 2 Pinning diagram.

HEF4006BP : 14-lead DIL; plastic (SOT-27).
HEF4006BD : 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4006BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

FUNCTION TABLE

D_n	$\overline{CP}$	O_n *
D_1	↘	D_1
X	↗	no change

X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition
D_1 = either HIGH or LOW
* The moment D_1 appears at O depends on the register length.

PINNING

D_A to D_D	data inputs
$\overline{CP}$	clock input (HIGH to LOW; edge-triggered)
O_{3A} to O_{3D}; O_{4C}; O_{4D}	data outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

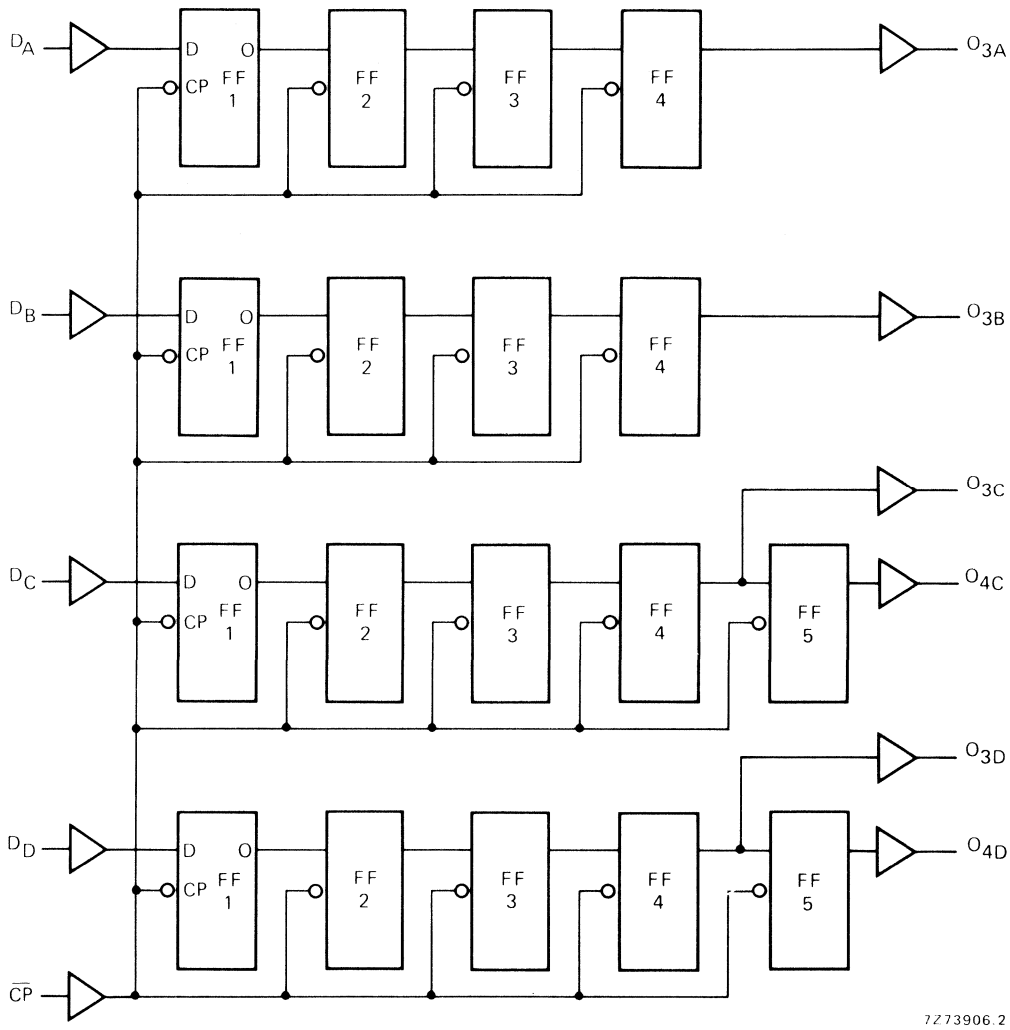


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$\overline{CP} \rightarrow O_n$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum clock pulse width; HIGH	5		60	30		ns	see also waveforms Fig. 4
	10	t_{WCPH}	40	20		ns	
	15		30	15		ns	
Set-up time $D_n \rightarrow \overline{CP}$	5		20	10		ns	
	10	t_{su}	10	5		ns	
	15		5	0		ns	
Hold time $D_n \rightarrow \overline{CP}$	5		5	−5		ns	
	10	t_{hold}	5	0		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5		9	18		MHz	
	10	f_{max}	15	30		MHz	
	15		18	36		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	600 f_i + Σ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	3200 f_i + Σ($f_o C_L$) × V_{DD}^2	
	15	11 600 f_i + Σ($f_o C_L$) × V_{DD}^2	

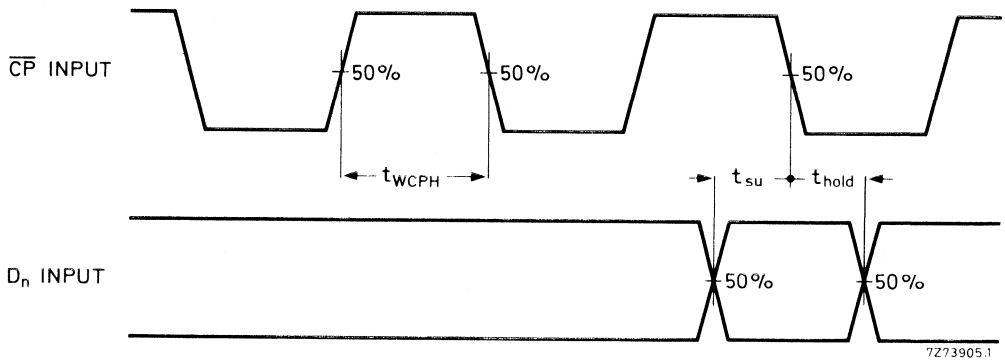


Fig. 4 Waveforms showing minimum clock pulse width, and set-up and hold-times for D_n to $\overline{CP}$. Set-up and hold times are shown as positive values but may be specified as negative values.

DUAL COMPLEMENTARY PAIR AND INVERTER

The HEF4007UB is a dual complementary pair and an inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors.

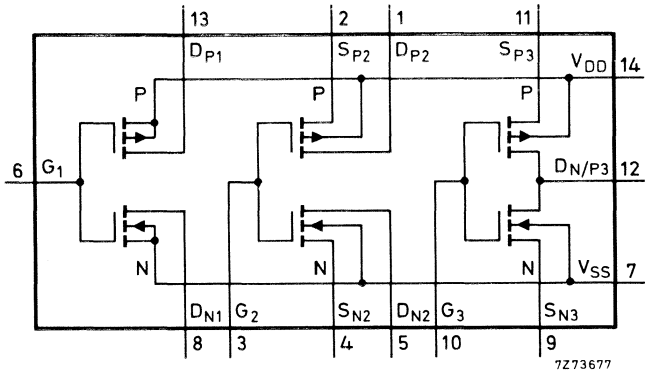


Fig. 1 Schematic diagram.

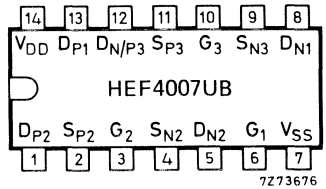


Fig. 2 Pinning diagram.

HEF4007UBP : 14-lead DIL; plastic (SOT-27).
HEF4007UBD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4007UBT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

PINNING

S_{P2}, S_{P3}	source connections to 2nd and 3rd p-channel transistors
D_{P1}, D_{P2}	drain connections from the 1st and 2nd p-channel transistors
D_{N1}, D_{N2}	drain connections from the 1st and 2nd n-channel transistors
S_{N2}, S_{N3}	source connections to the 2nd and 3rd n-channel transistors
$D_{N/P3}$	common connection to the 3rd p-channel and n-channel transistor drains
G_1 to G_3	gate connections to n-channel and p-channel of the three transistor pairs

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications for V_{IH}/V_{IL} unbuffered stages

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$G_n \rightarrow D_N; D_P$	5		40	80	ns	13 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
	5		40	75	ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$4500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$20\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$50\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

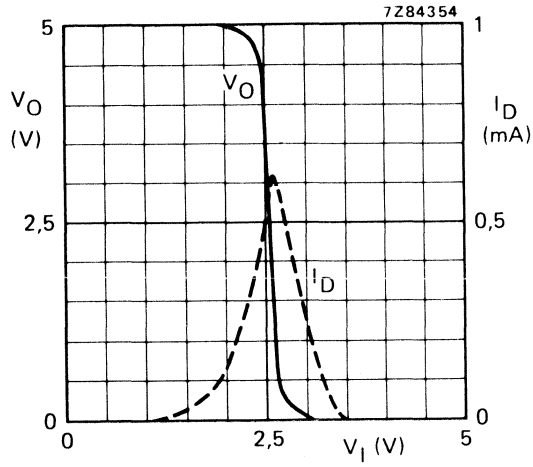


Fig. 3 Typical drain current I_D and output voltage V_O as functions of input voltage; V_{DD} = 5 V; T_{amb} = 25 °C.

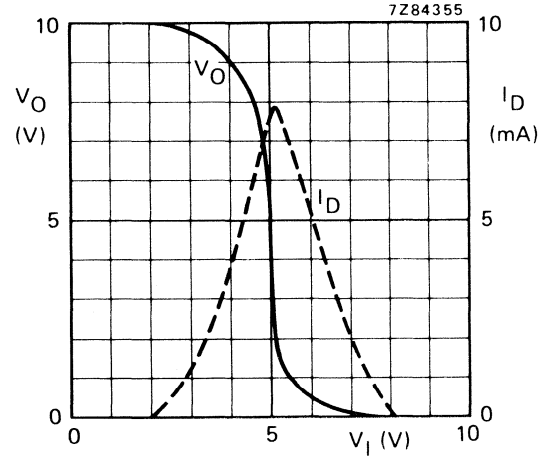


Fig. 4 Typical drain current I_D and output voltage V_O as functions of input voltage; V_{DD} = 10 V; T_{amb} = 25 °C.

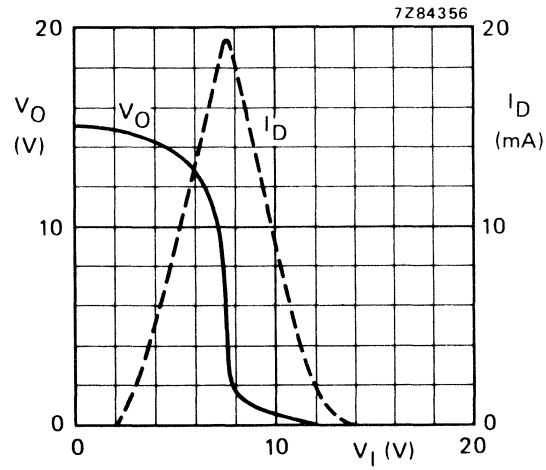


Fig. 5 Typical drain current I_D and output voltage V_O as functions of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

APPLICATION INFORMATION

Some examples of applications for the HEF4007UB are:

- High input impedance amplifiers
- Linear amplifiers
- (Crystal) oscillators
- High-current sink and source drivers
- High impedance buffers.

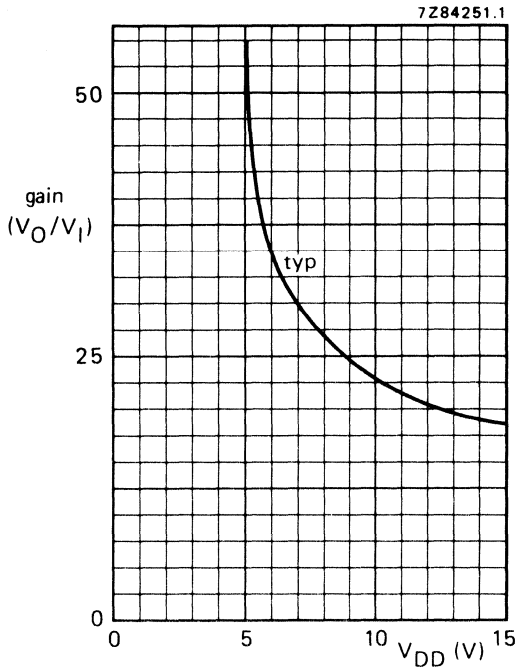


Fig. 6 Voltage gain (V_o/V_i) as a function of supply voltage.

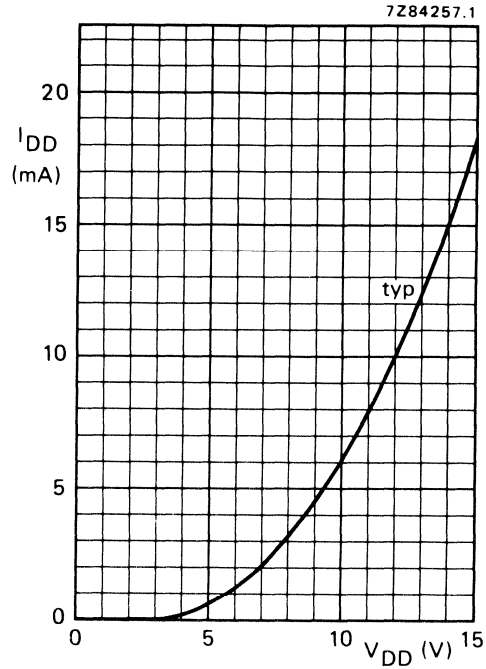


Fig. 7 Supply current as a function of supply voltage.

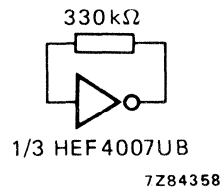


Fig. 8 Test set-up for measuring graphs of Figs 6 and 7.
This is also an example of an analogue amplifier using one HEF4007UB gate.

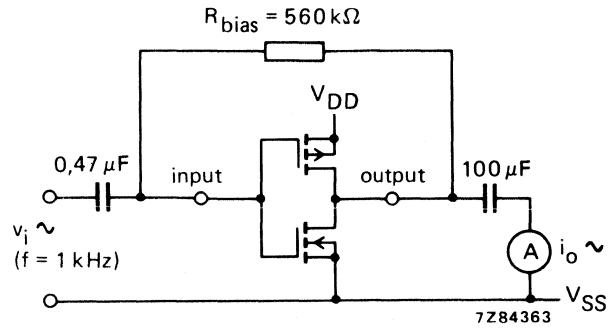
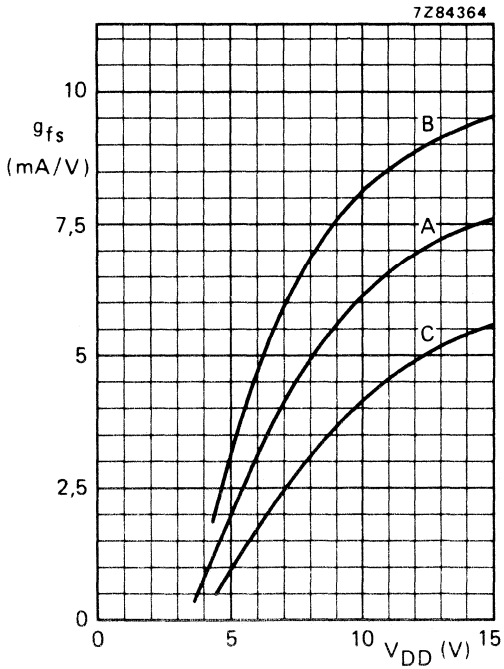


Fig. 9 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 10).



Curves in Fig. 10:

A: average,
B: average + 2 s,
C: average − 2 s, in where 's' is the observed standard deviation.

Fig. 10 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

APPLICATION INFORMATION (continued)

Figures 11 to 14 show some applications in which the HEF4007UB is used.

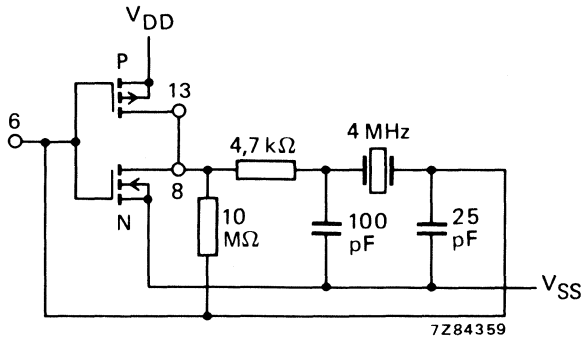


Fig. 11 4 MHz crystal oscillator.

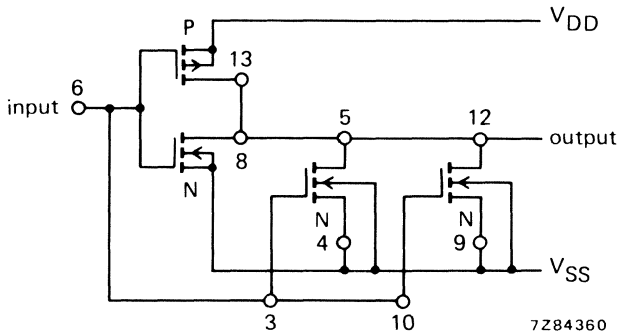


Fig. 12 High current sink driver.

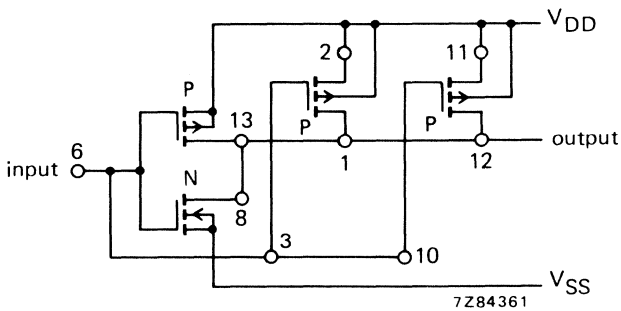


Fig. 13 High current source driver.

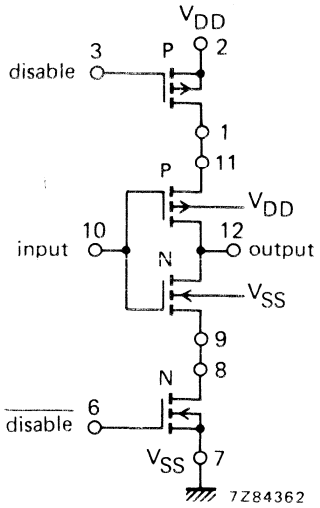


Fig. 14 High impedance buffer.

FUNCTION TABLE for Fig. 14.

input	disable	output
H	L	L
L	L	H
X	H	open

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

NOTE

Rules for maintaining electrical isolation between transistors and monolithic substrate:

Pin number 14 must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.

Pin number 7 must be maintained at the most negative (or equally negative) potential with respect to any other pin of the HEF4007UB.

Violation of these rules will result in improper transistor operation and/or possible permanent damage to the HEF4007UB.

4-BIT BINARY FULL ADDER

The HEF4008B is a 4-bit binary full adder with two 4-bit data inputs (A_0 to A_3, B_0 to B_3), a carry input (C_{IN}), four sum outputs (S_0 to S_3), and a carry output (C_{OUT}). The IC uses full look-ahead across 4 bits to generate C_{OUT}. This minimizes the necessity for extensive look-ahead and carry-cascading circuits.

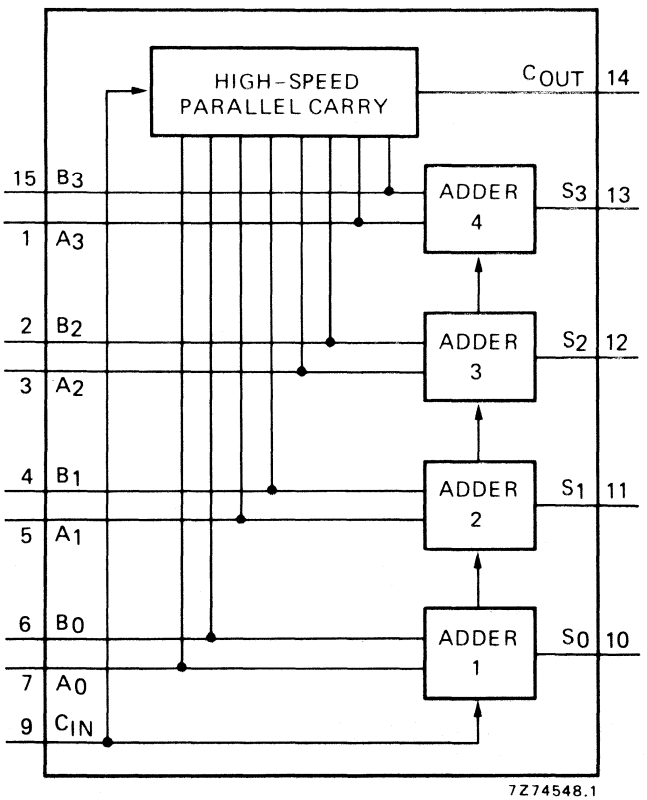


Fig. 1 Functional diagram.

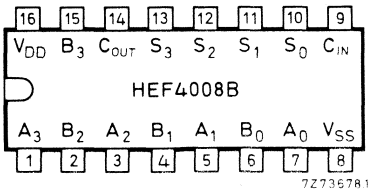


Fig. 2 Pinning diagram.

PINNING

A_0 to A_3	data inputs
B_0 to B_3	data inputs
S_0 to S_3	sum outputs
C_{IN}	carry input
C_{OUT}	carry output

TRUTH TABLE (one adder)

C_{IN}	A	B	C_{OUT}	S
L	L	L	L	L
L	L	H	L	H
L	H	L	L	H
L	H	H	H	L
H	L	L	L	H
H	L	H	H	L
H	H	L	H	L
H	H	H	H	H

HEF4008BP : 16-lead DIL; plastic (SOT-38Z).
HEF4008BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4008BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

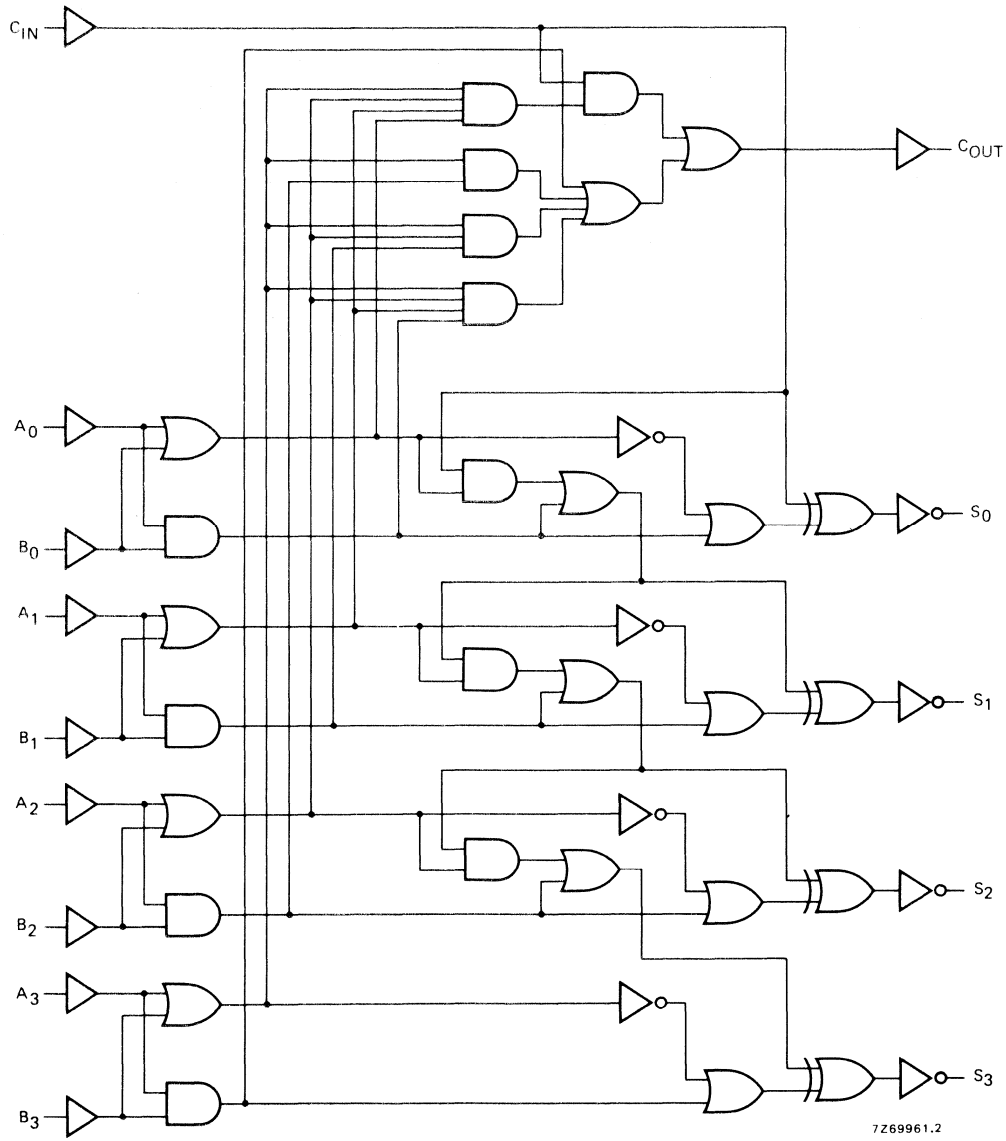


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
sum in → sum out	5			150	300 ns	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			135	270 ns	108 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
sum in → C_{OUT}	5			125	250 ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
	5			100	200 ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90 ns	34 ns + (0,23 ns/pF) C_L
	15			30	60 ns	22 ns + (0,16 ns/pF) C_L
C_{IN} → sum out	5			130	260 ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
	5			115	230 ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
C_{IN} → C_{OUT}	5			90	180 ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70 ns	24 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
	5			75	150 ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70 ns	24 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
Output transition times						
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 500 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	6 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	13 500 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

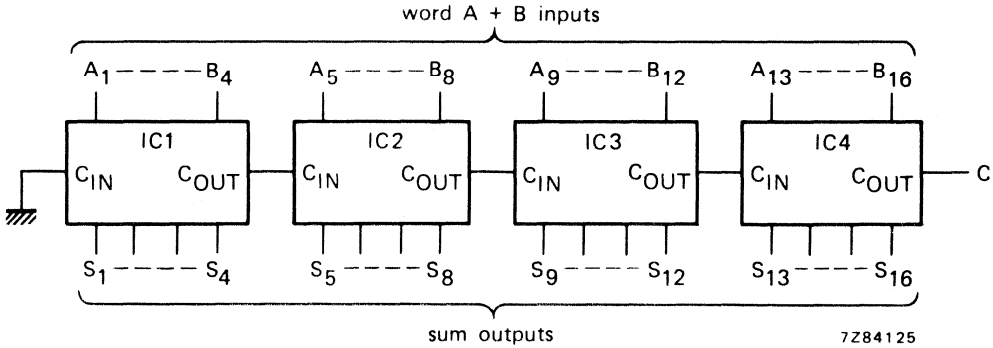


Fig. 4 Example of a 16-bit full adder using 4 HEF4008B ICs.

QUADRUPLE 2-INPUT NAND GATE

The HEF4011B provides the positive quadruple 2-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

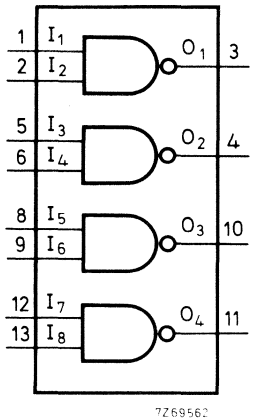


Fig. 1 Functional diagram.

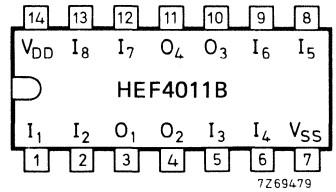


Fig. 2 Pinning diagram.

HEF4011BP : 14-lead DIL; plastic (SOT-27).
HEF4011BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4011BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

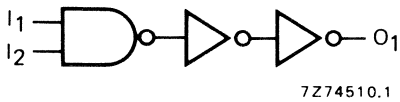


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

Products approved to CECC 90 104-008.

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leqslant 20$ ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$	5	t_{PHL}; t_{PLH}	55	110	ns	28 ns + (0,55 ns/pF) C_L
	10		25	45	ns	14 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L
Output transition times						
HIGH to LOW	5	t_{THL}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$20\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT NAND GATE

The HEF4011UB is a quadruple 2-input NAND gate. This unbuffered single stage version provides a direct implementation of the NAND function. The output impedance and output transition time depends on the input voltage and input rise and fall times applied.

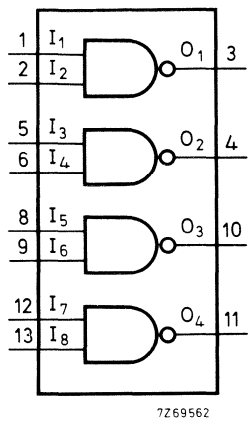


Fig. 1 Functional diagram.

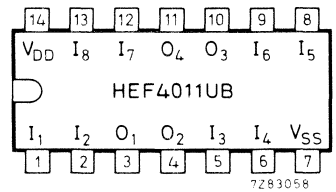


Fig. 2 Pinning diagram.

HEF4011UBP : 14-lead DIL; plastic (SOT-27).
HEF4011UBD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4011UBT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

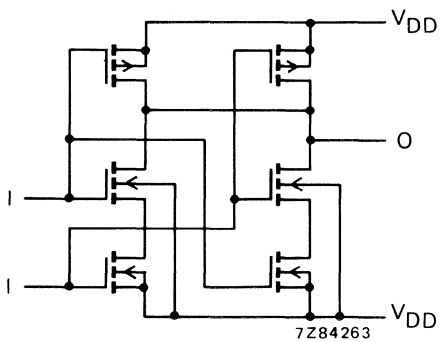


Fig. 3 Schematic diagram (one gate). The splitting-up of the n-transistors provide identical inputs.

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications for V_{IH}/V_{IL} unbuffered stages

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		60	120	ns	25 ns + (0,70 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	12 ns + (0,27 ns/pF) C_L
	15		20	40	ns	10 ns + (0,20 ns/pF) C_L
	5		35	70	ns	8 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		17	35	ns	9 ns + (0,16 ns/pF) C_L
Output transition times	5		75	150	ns	15 ns + (1,20 ns/pF) C_L
	10	t_{THL}	30	60	ns	6 ns + (0,48 ns/pF) C_L
HIGH to LOW	15		20	40	ns	4 ns + (0,32 ns/pF) C_L
	5		60	110	ns	10 ns + (1,00 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
Input capacitance		C_{IN}		10	pF	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$25\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

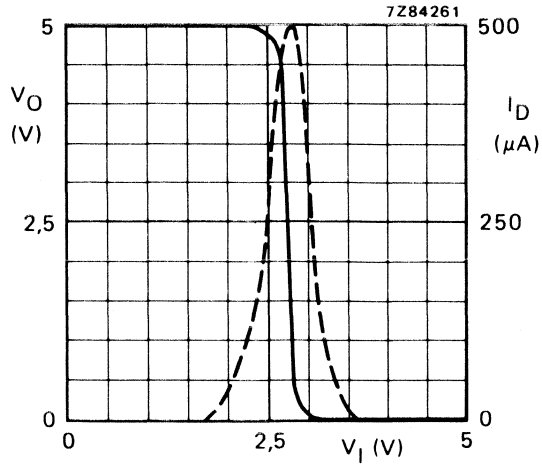


Fig. 4 Typical transfer characteristics; one input, the other input connected to V_{DD}; —— V_O; – – – I_D(drain current); $I_O = 0$; $V_{DD} = 5$ V.

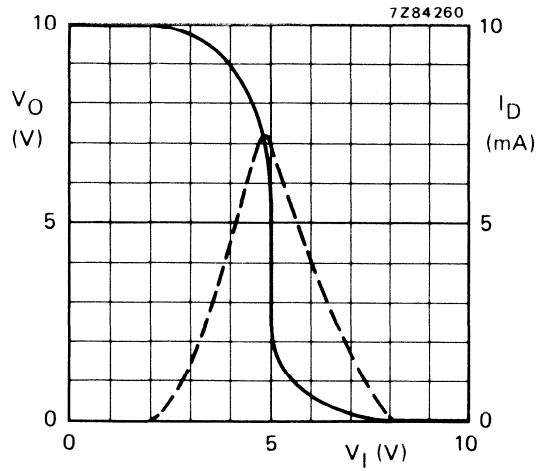


Fig. 5 Typical transfer characteristics; one input, the other input connected to V_{DD}; —— V_O; – – – I_D(drain current); $I_O = 0$; $V_{DD} = 10$ V.

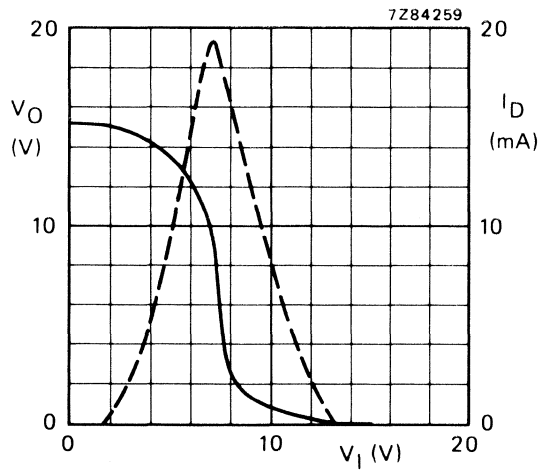


Fig. 6 Typical transfer characteristics; one input, the other input connected to V_{DD}; —— V_O; – – – I_D(drain current); $I_O = 0$; $V_{DD} = 15$ V.

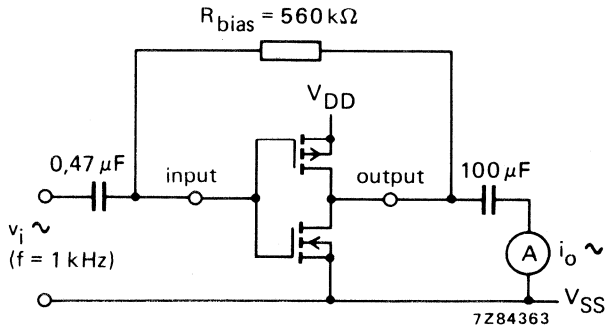
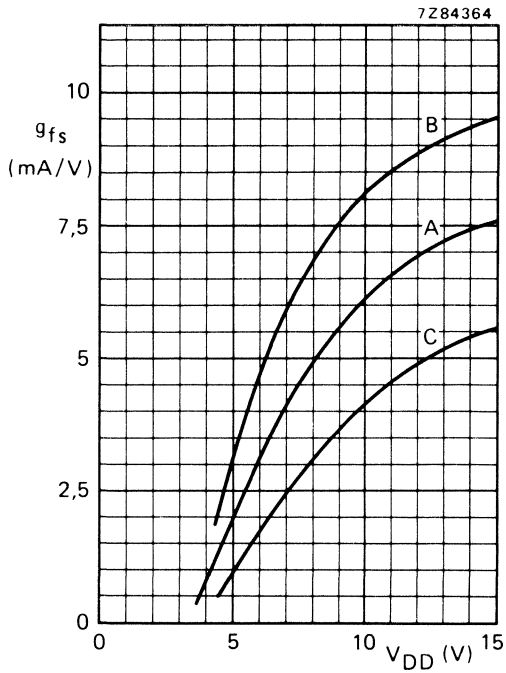


Fig. 7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 8).



Curves in Fig. 8:

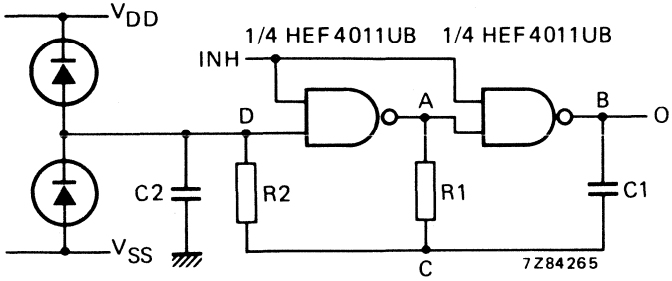
A : average,
B : average + 2 s,
C : average −2 s, in where:
's' is the observed standard deviation.

Fig. 8 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

APPLICATION INFORMATION

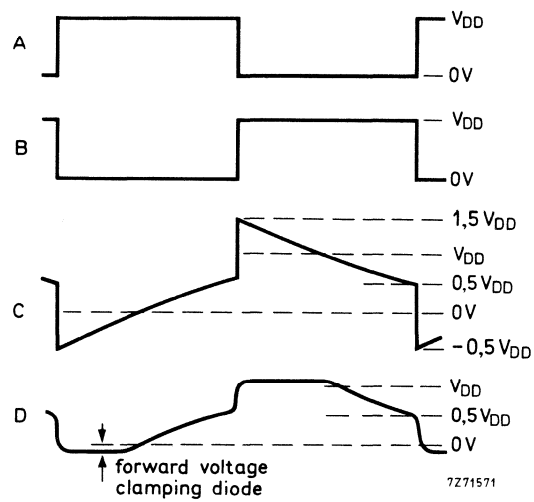
Some examples of applications for the HEF4011UB are shown below.

Because of the fact that this circuit is unbuffered, it is suitable for use in (partly) analogue circuits.



INH	O
L	H
H	OSC

(a)



(b)

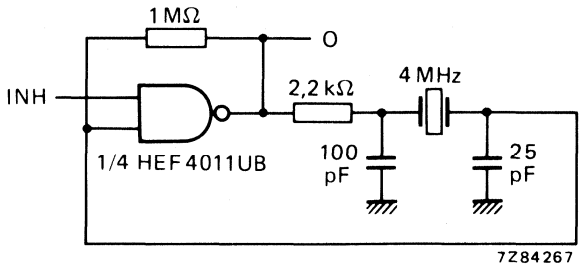
Fig. 9 (a) Astable relaxation oscillator using two HEF4011UB gates; the diodes may be BAW62; C2 is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

In Fig. 9 the oscillation frequency is mainly determined by R1C1, provided $R1 << R2$ and $R2C2 << R1C1$.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \quad \text{and} \quad T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \quad \text{where}$$

V_{ST} is the signal threshold level of the gate. The period is fairly independent of V_{DD}, V_{ST} and temperature. The duty factor, however, is influenced by V_{ST}.



INH	O
L	H
H	OSC

Fig. 10 Example of a crystal oscillator using one HEF4011UB gate.

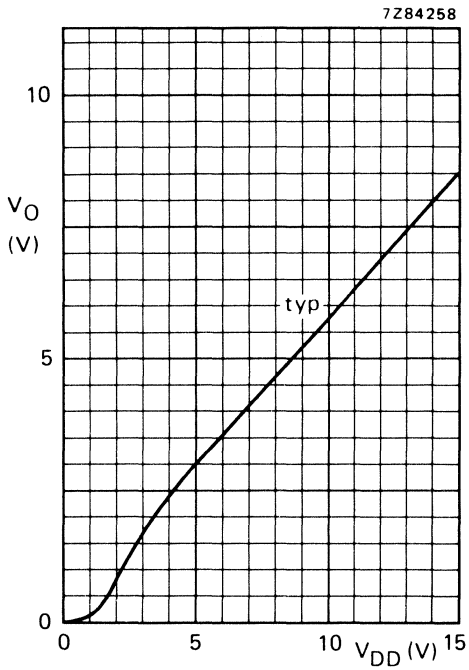


Fig. 11 Output voltage as a function of supply voltage.

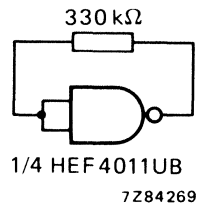


Fig. 12 Test set-up for measuring graph of Fig. 11. Condition: all other inputs connected to ground.

NOTES

If a gate is just used as an amplifying inverter, there are two possibilities:

a. Connecting the inputs together gives simpler wiring, but makes the device output not completely symmetrical.

b. Connecting one input to V_{DD} will give the device a symmetrical output.

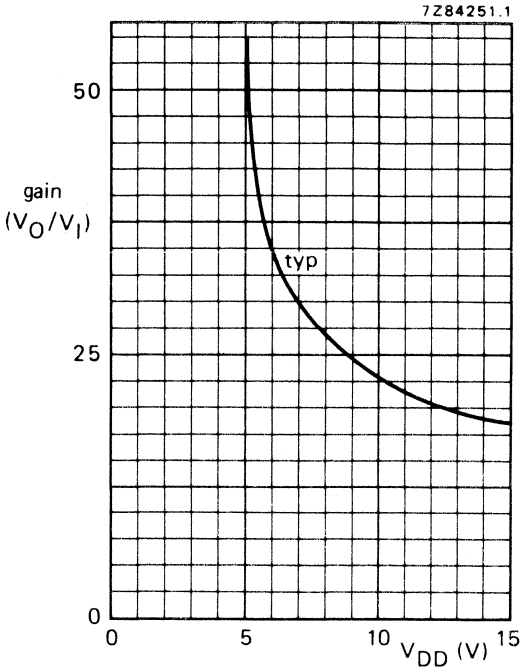


Fig. 13 Voltage gain (V_O/V_I) as a function of supply voltage.

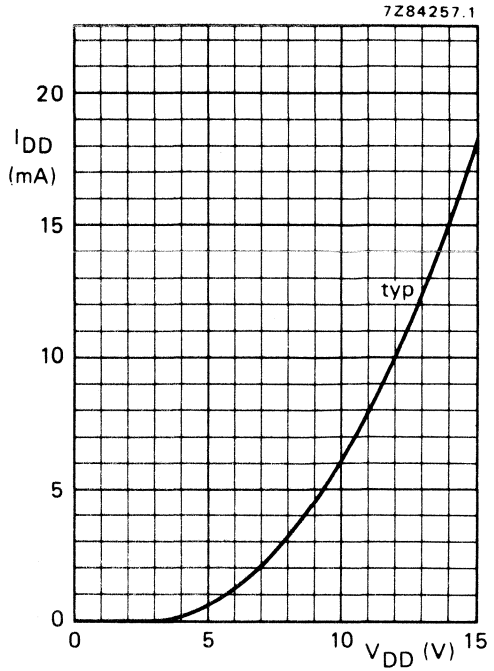


Fig. 14 Supply current as a function of supply voltage.

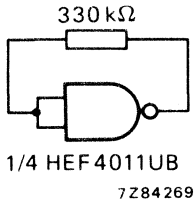


Fig. 15 Test set-up for measuring graphs of Figs 13 and 14. Condition: all other inputs connected to ground.

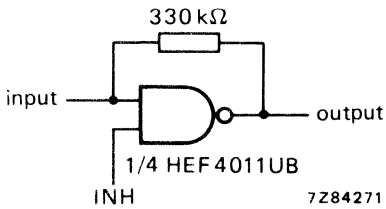


Fig. 16 Example of an analogue amplifier with inhibit using one HEF4011UB gate.

DUAL 4-INPUT NAND GATE

The HEF4012B provides the positive dual 4-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

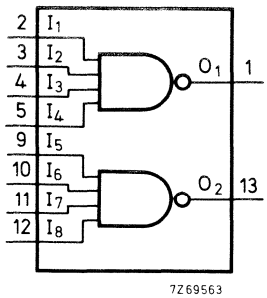


Fig. 1 Functional diagram.

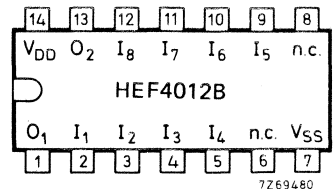


Fig. 2 Pinning diagram.

HEF4012BP : 14-lead DIL; plastic (SOT-27).
HEF4012BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4012BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

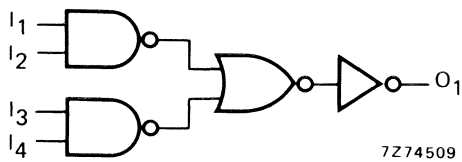


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		70	135	ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L
	5		70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4400 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	12 900 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

DUAL D-TYPE FLIP-FLOP

The HEF4013B is a dual D-type flip-flop which features independent set direct (S_D), clear direct (C_D), clock inputs (CP) and outputs (O,$\overline{O}$). Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the D or CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

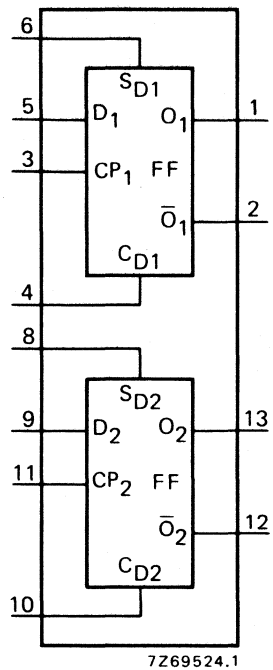


Fig. 1 Functional diagram.

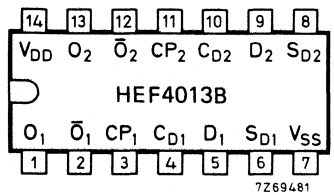


Fig. 2 Pinning diagram.

FAMILY DATA

I_{DD} LIMITS category FLIP-FLOPS

see Family Specifications

FUNCTION TABLES

inputs				outputs	
S_D	C_D	CP	D	O	$\overline{O}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H

inputs				outputs	
S_D	C_D	CP	D	O_{n+1}	$\overline{O}_{n+1}$
L	L	$\int$	L	L	H
L	L	$\int$	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
$\int$ = positive-going transition
O_{n+1} = state after clock positive transition

PINNING

D data inputs
CP clock input (L to H edge-triggered)
S_D asynchronous set-direct input (active HIGH)
C_D asynchronous clear-direct input (active HIGH)
O true output
$\overline{O}$ complement output

HEF4013BP : 14-lead DIL; plastic (SOT-27).
HEF4013BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4013BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

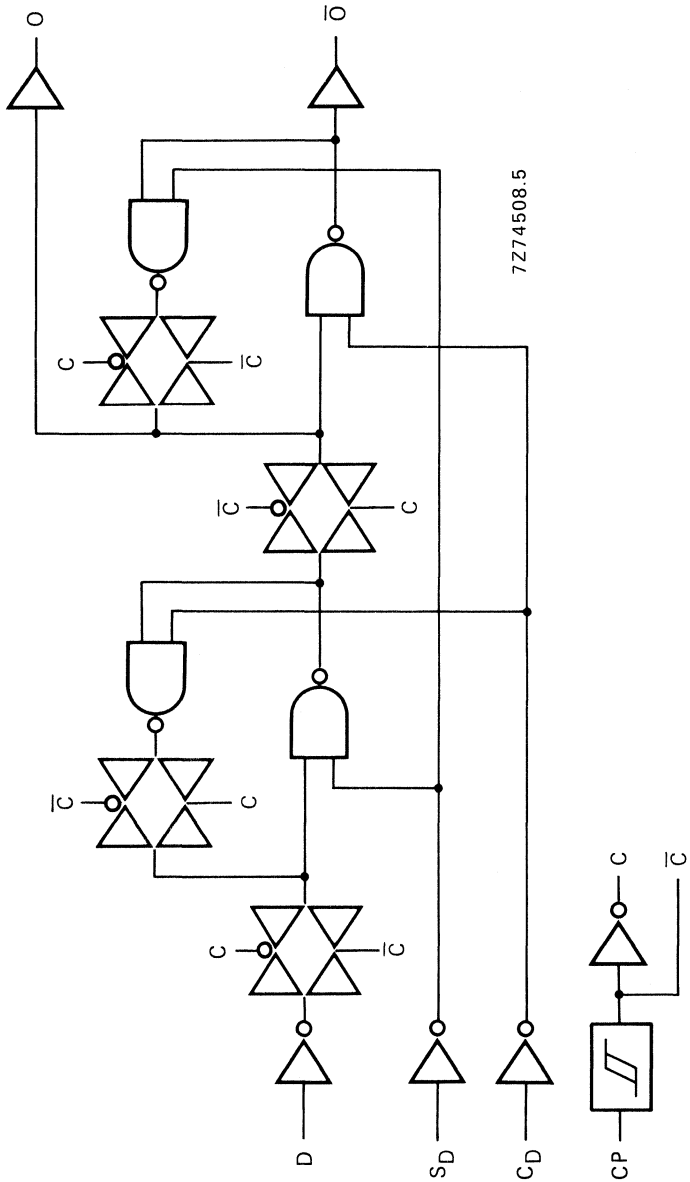


Fig. 3 Logic diagram (one flip-flop).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O, $\overline{O}$	5			110	220	ns	83 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF)C_L
	15			30	60	ns	22 ns + (0,16 ns/pF)C_L
	5			95	190	ns	68 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF)C_L
	15			30	60	ns	22 ns + (0,16 ns/pF)C_L
S_D → $\overline{O}$	5			100	200	ns	73 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF)C_L
	15			30	60	ns	22 ns + (0,16 ns/pF)C_L
S_D → O	5			75	150	ns	48 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF)C_L
	15			25	50	ns	17 ns + (0,16 ns/pF)C_L
C_D → O	5			100	200	ns	73 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF)C_L
	15			30	60	ns	22 ns + (0,16 ns/pF)C_L
C_D → $\overline{O}$	5			60	120	ns	33 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF)C_L
	15			20	40	ns	12 ns + (0,16 ns/pF)C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Set-up time D → CP	5	t_{su}	40	20		ns	see also waveforms Figs 4 and 5
	10		25	10		ns	
	15		15	5		ns	
Hold time D → CP	5	t_{hold}	20	0		ns	
	10		20	0		ns	
	15		15	0		ns	
Minimum clock pulse width; LOW	5	t_{WCPL}	60	30		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum S_D pulse width; HIGH	5	t_{WSDH}	50	25		ns	
	10		24	12		ns	
	15		20	10		ns	
Minimum C_D pulse width; HIGH	5	t_{WCDH}	50	25		ns	
	10		24	12		ns	
	15		20	10		ns	
Recovery time for S_D	5	t_{RSD}	15	−5		ns	
	10		15	0		ns	
	15		15	0		ns	
Recovery time for C_D	5	t_{RCD}	40	25		ns	
	10		25	10		ns	
	15		25	10		ns	
Maximum clock pulse frequency	5	f_{max}	7	14		MHz	
	10		14	28		MHz	
	15		20	40		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$850\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = total load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$9\,000\ f_i + \Sigma(f_o CL) \times V_{DD}^2$	

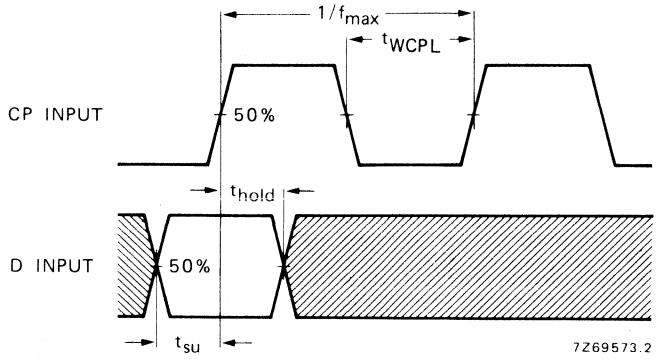


Fig. 4 Waveforms showing set-up times, hold times and minimum clock pulse width.
Set-up and hold times are shown as positive values but may be specified as negative values.

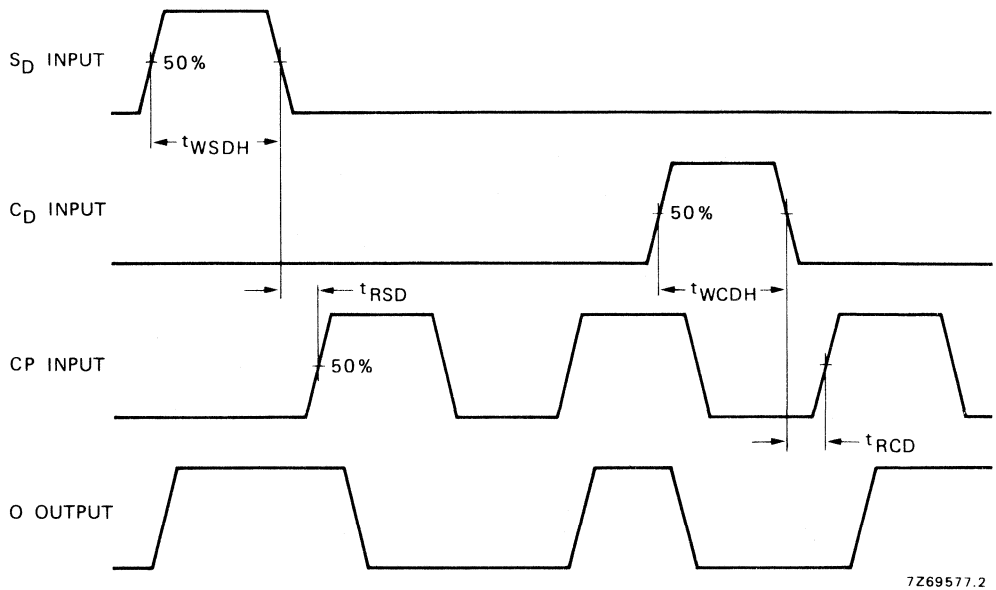


Fig. 5 Waveforms showing recovery times for S_D and C_D; minimum S_D and C_D pulse widths.

APPLICATION INFORMATION

Some examples of applications for the HEF4013B are:

- Counters/dividers
- Registers
- Toggle flip-flops

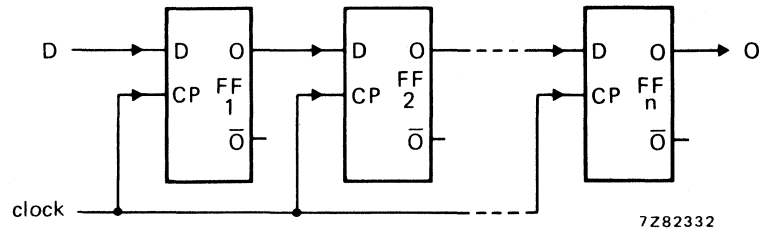


Fig. 6 Typical application of the HEF4013B in an n-stage shift register.

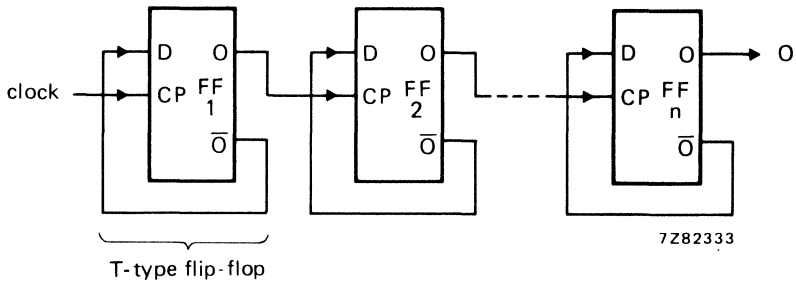


Fig. 7 Typical application of the HEF4013B in a binary ripple up-counter; divide-by-2^n.

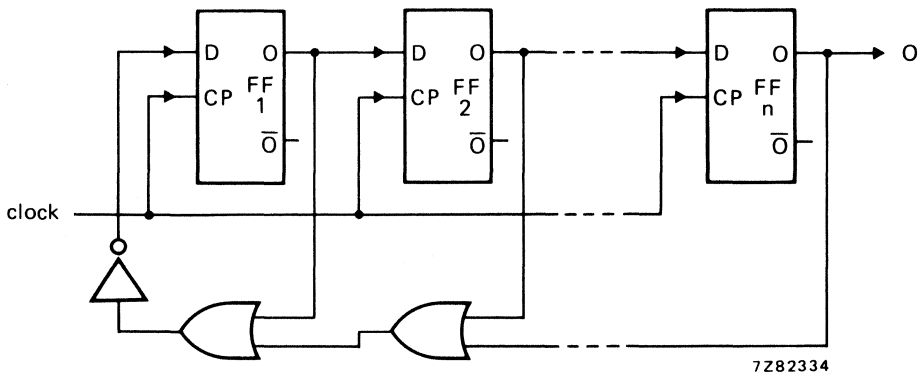


Fig. 8 Typical application of the HEF4013B in a modified ring counter; divide-by-(n + 1).

8-BIT STATIC SHIFT REGISTER

The HEF4014B is a fully synchronous edge-triggered 8-bit static shift register with eight synchronous parallel inputs (P_0 to P_7), a synchronous serial data input (D_S), a synchronous parallel enable input (PE), a LOW to HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages (O_5 to O_7).

Operation is synchronous and the device is edge-triggered on the LOW to HIGH transition of CP. Each register stage is of a D-type master-slave flip-flop. When PE is HIGH, data is loaded into the register from P_0 to P_7 on the LOW to HIGH transition of CP. When PE is LOW, data is shifted to the first position from D_S, and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times

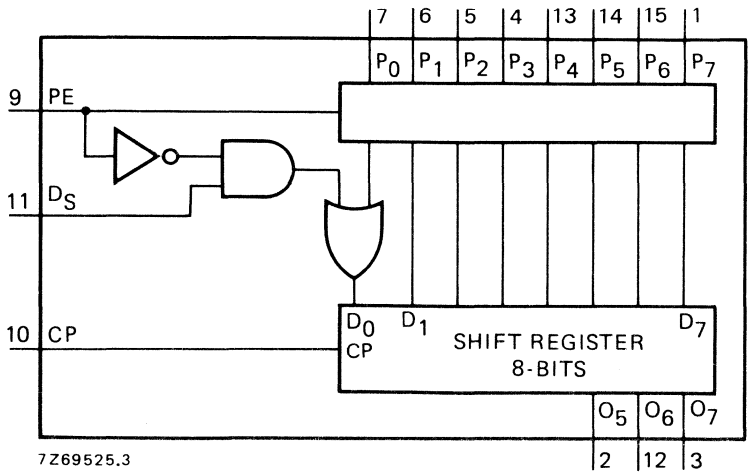


Fig. 1 Functional diagram.

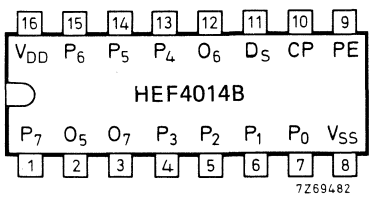


Fig. 2 Pinning diagram.

HEF4014BP : 16-lead DIL; plastic (SOT-38Z).
HEF4014BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4014BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

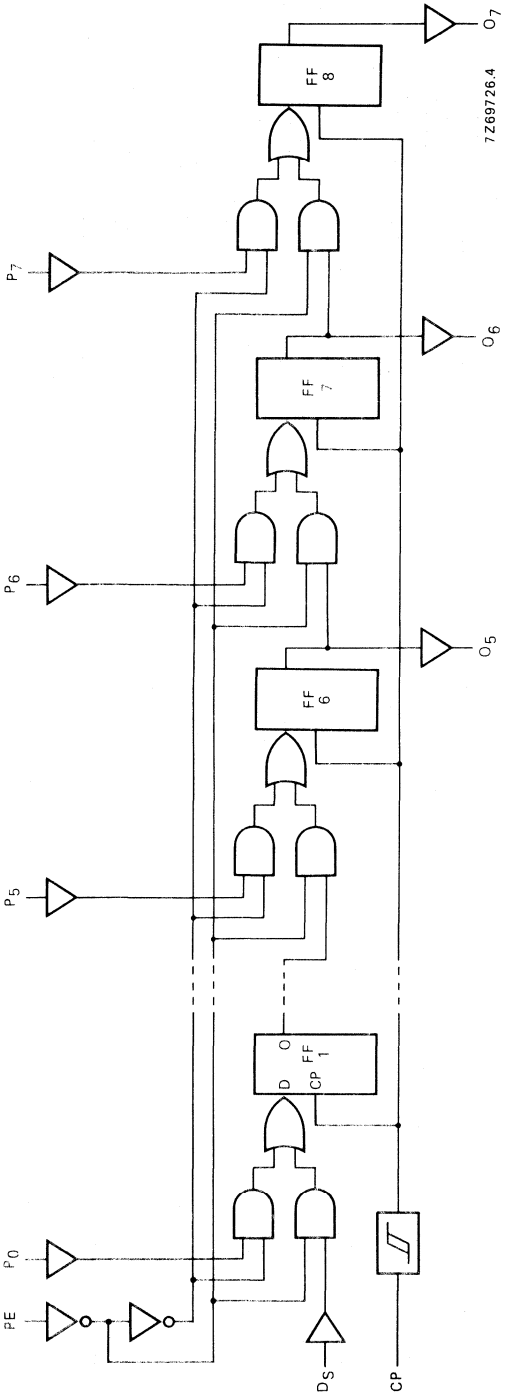


Fig. 3 Logic diagram.

PINNING

PE parallel enable input

P_0 to P_7 parallel data inputs

D_S serial data input

CP clock input (LOW to HIGH edge-triggered)

O_5 to O_7 buffered parallel outputs from the last three stages

FUNCTION TABLES

Serial operation

	inputs			outputs		
n	CP	D_S	PE	O_5	O_6	O_7
1	∫	D_1	L	X	X	X
2	∫	D_2	L	X	X	X
3	∫	D_3	L	X	X	X
6	∫	X	L	D_1	X	X
7	∫	X	L	D_2	D_1	X
8	∫	X	L	D_3	D_2	D_1
	\	X	X	no change		

Parallel operation

	inputs			outputs		
n	CP	D_S	PE	O_5	O_6	O_7
1	∫	X	H	P_5	P_6	P_7
	\	X	X	no change		

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
\ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$900\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,300\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$12\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
C_P → O_n	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up times	5		40	10		ns	
PE → CP	10	t_{su}	25	5		ns	
	15		15	0		ns	
	5		35	−5		ns	
D_S → CP	10	t_{su}	25	−5		ns	
	15		25	0		ns	
	5		35	−5		ns	
P_n → CP	10	t_{su}	25	−5		ns	
	15		25	0		ns	
Hold times	5		25	−5		ns	
PE → CP	10	t_{hold}	20	0		ns	see also waveforms Fig. 4
	15		15	0		ns	
	5		30	15		ns	
D_S → CP	10	t_{hold}	20	10		ns	
	15		15	7		ns	
	5		30	15		ns	
P_n → CP	10	t_{hold}	20	10		ns	
	15		15	7		ns	
Minimum clock pulse width; LOW	5		70	35		ns	
	10	t_{WCPL}	30	15		ns	
	15		24	12		ns	
Maximum clock pulse frequency	5		6	13		MHz	
	10	f_{max}	15	30		MHz	
	15		20	40		MHz	

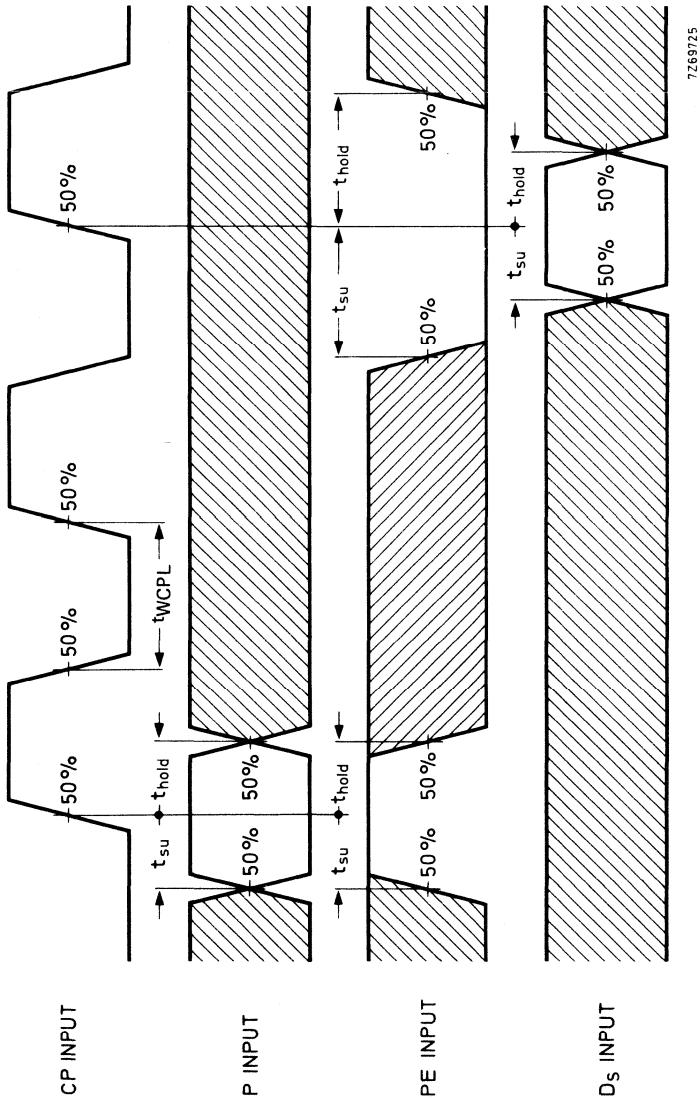


Fig. 4 Waveforms showing minimum clock pulse width, and set-up and hold times for PE to CP, D_S to CP, and P to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF4014B are:

- Parallel-to-serial converter
- Serial data queueing
- General purpose register

DUAL 4-BIT STATIC SHIFT REGISTER

The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs (O_0 to O_3) and an overriding asynchronous master reset input (MR). Information present on D is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. A HIGH on MR clears the register and forces O_0 to O_3 to LOW, independent of CP and D. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

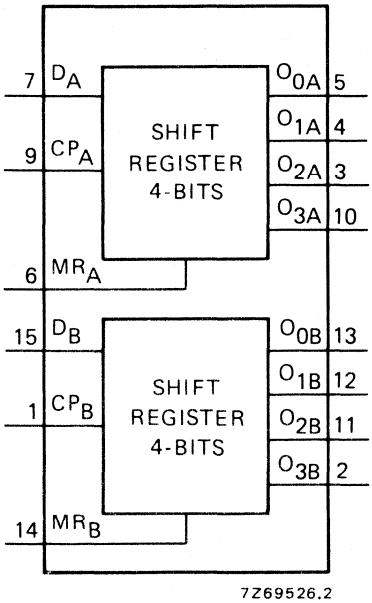


Fig. 1 Functional diagram.

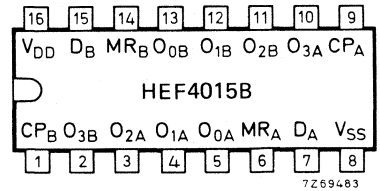


Fig. 2 Pinning diagram.

HEF4015BP : 16-lead DIL; plastic (SOT-38Z).
HEF4015BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4015BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_A, D_B	serial data input
MR_A, MR_B	master reset input (active HIGH)
CP_A, CP_B	clock input (LOW-to-HIGH edge-triggered)
O_{0A}, O_{1A}, O_{2A}, O_{3A}	parallel outputs
O_{0B}, O_{1B}, O_{2B}, O_{3B}	parallel outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4015B are:

- Serial-to-parallel converter
- Buffer stores
- General purpose register

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM (one register)

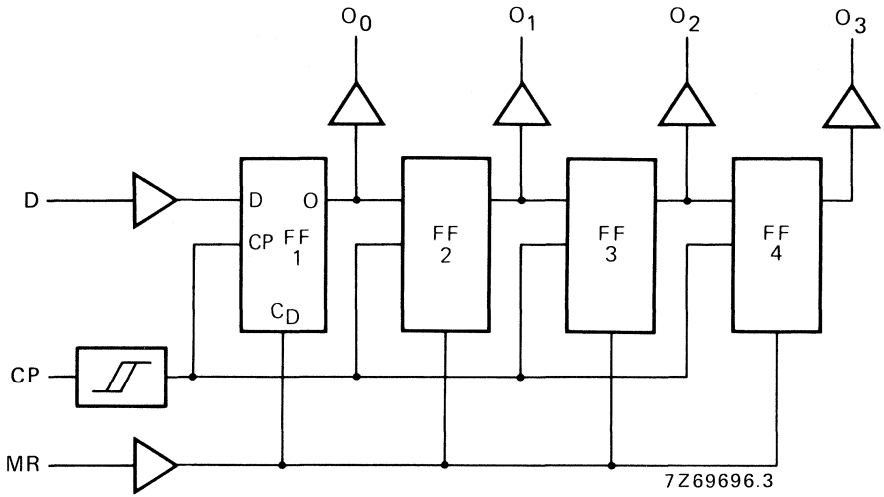


Fig. 3 Logic diagram.

FUNCTION TABLE

	inputs			outputs			
n	CP	D	MR	O_0	O_1	O_2	O_3
1	∫	D_1	L	D_1	X	X	X
2	∫	D_2	L	D_2	D_1	X	X
3	∫	D_3	L	D_3	D_2	D_1	X
4	∫	D_4	L	D_4	D_3	D_2	D_1
	⌝	X	L	no change			
	X	X	H	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌝ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
MR → O_n	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		25	−15		ns	
D → CP	10	t_{su}	25	−10		ns	
	15		20	−5		ns	
Hold time	5		40	20		ns	
D → CP	10	t_{hold}	20	10		ns	
	15		15	8		ns	
Minimum clock pulse width; LOW	5		60	30		ns	see waveforms Figs 4 and 5
	10	t_{WCPL}	30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5		80	40		ns	
	10	t_{WMRH}	30	15		ns	
	15		24	12		ns	
Recovery time for MR	5		50	20		ns	
	10	t_{RMR}	30	10		ns	
	15		20	5		ns	
Maximum clock pulse frequency	5		7	15		MHz	
	10	f_{max}	15	30		MHz	
	15		22	44		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 500 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	6 300 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	
	15	17 000 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	

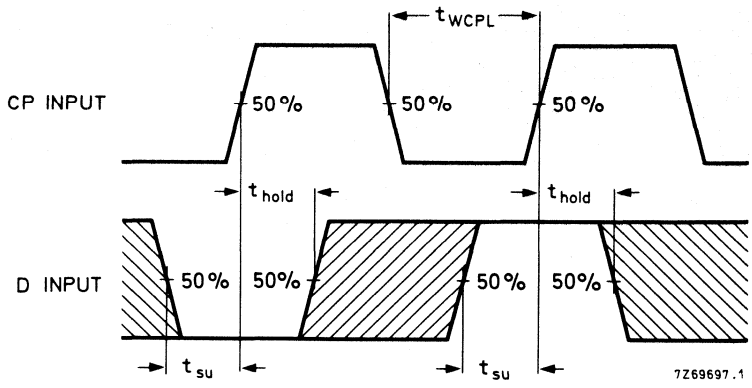


Fig. 4 Waveforms showing set-up times, hold times and minimum clock pulse width.
Set-up and hold times are shown as positive values but may be specified as negative values.

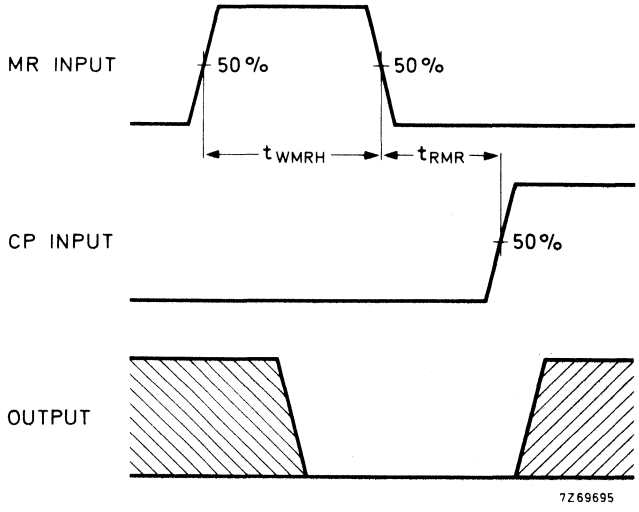


Fig. 5 Waveforms showing recovery time for MR and minimum MR pulse width.

QUADRUPLE BILATERAL SWITCHES

The HEF4016B has four independent analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is disabled and a high impedance between Y and Z is established (OFF condition). Current through a switch will not cause additional V_{DD} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{DD} \geqslant (V_Y, V_Z) \geqslant V_{SS}$. Inputs Y and Z are electrically equivalent terminals.

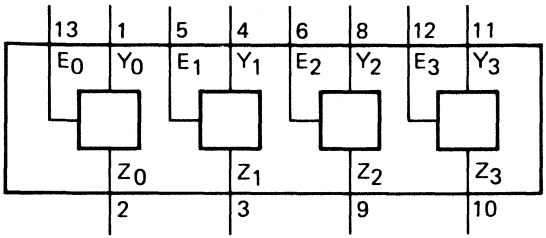


Fig. 1 Functional diagram.

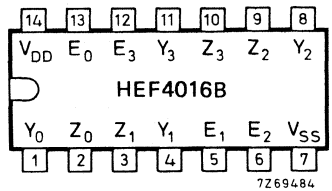


Fig. 2 Pinning diagram.

HEF4016BP: 14-lead DIL; plastic (SOT-27).
HEF4016BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4016BT: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PINNING

E_0 to E_3 enable inputs
Y_0 to Y_3 input/output terminals
Z_0 to Z_3 input/output terminals

APPLICATION INFORMATION

Some examples of applications for the HEF4016B are:

- Signal gating
- Modulation
- Demodulation
- Chopper

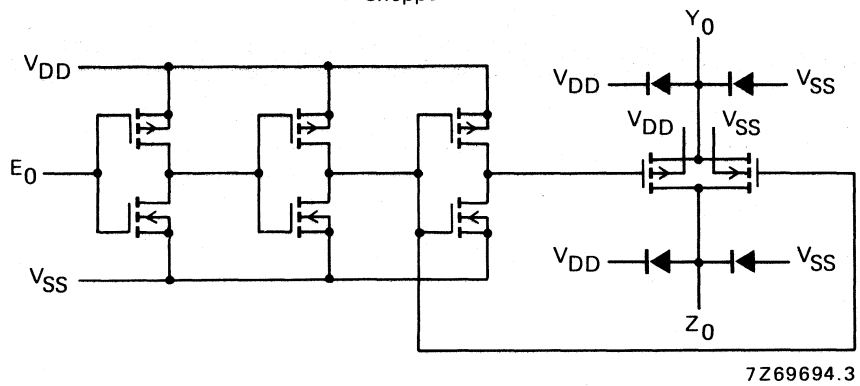


Fig. 3 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch — P max. 100 mW

For other RATINGS see Family Specifications

D.C. CHARACTERISTICS

T_{amb} = 25 °C; V_{SS} = 0 V (unless otherwise specified)

parameter	V_{DD} V	symbol	typ.	max.	unit	conditions
ON resistance	5	R_{ON}	8000	–	Ω	E_n at V_{IH}; V_{is} = 0 to V_{DD}; see Fig. 4
	10		230	690	Ω	
	15		115	350	Ω	
ON resistance	5	R_{ON}	140	425	Ω	E_n at V_{IH}; V_{is} = V_{SS}; see Fig. 4
	10		65	195	Ω	
	15		50	145	Ω	
ON resistance	5	R_{ON}	170	515	Ω	E_n at V_{IH}; V_{is} = V_{DD}; see Fig. 4
	10		95	285	Ω	
	15		75	220	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	200	–	Ω	E_n at V_{IH}; V_{is} = 0 to V_{DD}; see Fig. 4
	10		15	–	Ω	
	15		10	–	Ω	

parameter	V_{DD} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+ 25 min.	+ 25 max.	+ 85 min.	+ 85 max.	unit	condition
Quiescent device current	5	I_{DD}	–	1,0	–	1,0	–	7,5	μA	V_{SS} = 0; all valid input combinations; V_I = V_{SS} or V_{DD}
	10		–	2,0	–	2,0	–	15,0	μA	
	15		–	4,0	–	4,0	–	30,0	μA	
Input leakage current at E_n	15	$\pm I_{IN}$	–	–	–	300	–	1000	nA	E_n at V_{SS} or V_{DD}
OFF-state leakage current, any channel OFF	5	I_{OZ}	–	–	–	–	–	–	nA	E_n at V_{IL}; V_{is} = V_{SS} or V_{DD}; V_{os} = V_{DD} or V_{SS}
	10		–	–	–	–	–	–	nA	
	15		–	–	–	200	–	–	nA	
E_n input voltage LOW	5	V_{IL}	–	1,5	–	1,5	–	1,5	V	switch OFF; see Fig. 9 for I_{OZ}
	10		–	3,0	–	3,0	–	3,0	V	
	15		–	4,0	–	4,0	–	4,0	V	
E_n input voltage HIGH	5	V_{IH}	3,5	–	3,5	–	3,5	–	V	low-impedance between Y and Z (ON condition) see R_{ON} switch
	10		7,0	–	7,0	–	7,0	–	V	
	15		11,0	–	11,0	–	11,0	–	V	

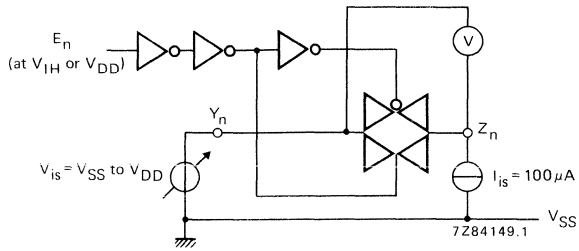


Fig. 4 Test set-up for measuring R_{ON}.

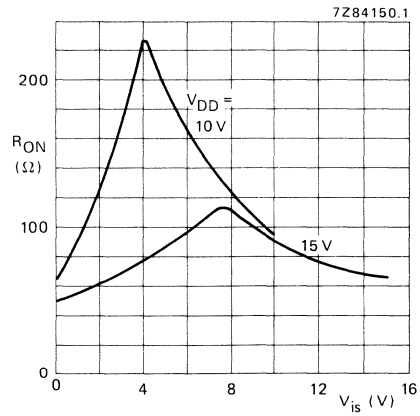


Fig. 5 Typical R_{ON} as a function of input voltage.

$E_n > V_{IH}$
I_{is} = 100 μA
V_{SS} = 0 V

A.C. CHARACTERISTICS V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		25	50	ns	
HIGH to LOW	10	t_{PHL}	10	20	ns	note 1
	15		5	10	ns	
	5		20	40	ns	
LOW to HIGH	10	t_{PLH}	10	20	ns	note 1
	15		5	10	ns	
Output disable times						
$E_n \rightarrow V_{os}$	5		90	130	ns	
HIGH	10	t_{PHZ}	80	110	ns	note 2
	15		75	100	ns	
	5		85	120	ns	
LOW	10	t_{PLZ}	75	100	ns	note 2
	15		75	100	ns	
Output enable times						
$E_n \rightarrow V_{os}$	5		40	80	ns	
HIGH	10	t_{PZH}	20	40	ns	note 2
	15		15	30	ns	
	5		40	80	ns	
LOW	10	t_{PZL}	20	40	ns	note 2
	15		15	30	ns	
Distortion, sine-wave	5		–		%	
response	10		0,08		%	note 3
	15		0,04		%	
Crosstalk between	5		–		MHz	
any two channels	10		1		MHz	note 4
	15		–		MHz	
Crosstalk; enable	5		–		mV	
input to output	10		50		mV	note 5
	15		–		mV	
OFF-state	5		–		MHz	
feed-through	10		1		MHz	note 6
	15		–		MHz	
ON-state frequency	5		–		MHz	
response	10		90		MHz	note 7
	15		–		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)*	5	$550\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$6\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

* All enable inputs switching.

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; E_n = V_{DD}; V_{is} = V_{DD} (square-wave); see Figs 6 and 10.
2. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; E_n = V_{DD} (square-wave);
   V_{is} = V_{DD} and R_L to V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} = V_{SS} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Figs 6 and 11.
3. R_L = 10 kΩ; C_L = 15 pF; E_n = V_{DD}; V_{is} = $\frac{1}{2}V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $\frac{1}{2}V_{DD}$);
   f_{is} = 1 kHz; see Fig. 7.
4. R_L = 1 kΩ; V_{is} = $\frac{1}{2}V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $\frac{1}{2}V_{DD}$);
   $20 \log \frac{V_{os}\,(B)}{V_{is}\,(A)}$ = −50 dB; E_n (A) = V_{SS}; E_n (B) = V_{DD}; see Fig. 8.
5. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; E_n = V_{DD} (square-wave); crosstalk is $|V_{os}|$ (peak value);
   see Fig. 6.
6. R_L = 1 kΩ; C_L = 5 pF; E_n = V_{SS}; V_{is} = $\frac{1}{2}V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $\frac{1}{2}V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}}$ = −50 dB; see Fig. 7.
7. R_L = 1 kΩ; C_L = 5 pF; E_n = V_{DD}; V_{is} = $\frac{1}{2}V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $\frac{1}{2}V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}}$ = −3 dB; see Fig. 7.

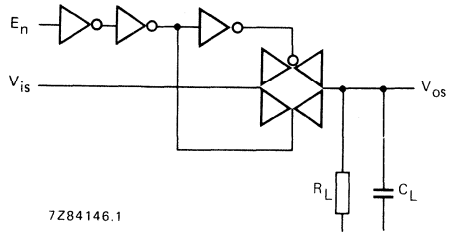


Fig. 6.

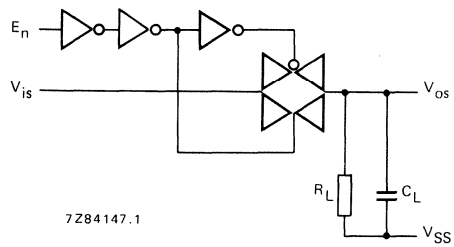
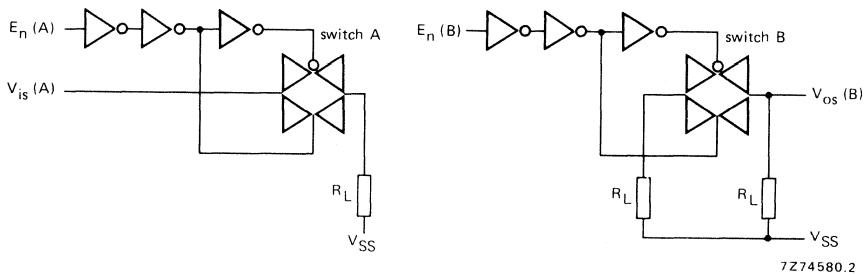


Fig. 7.



(a) (b)

Fig. 8.

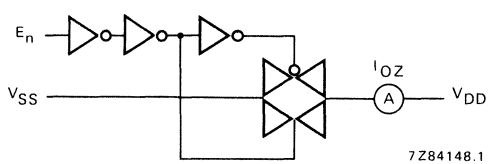


Fig. 9.

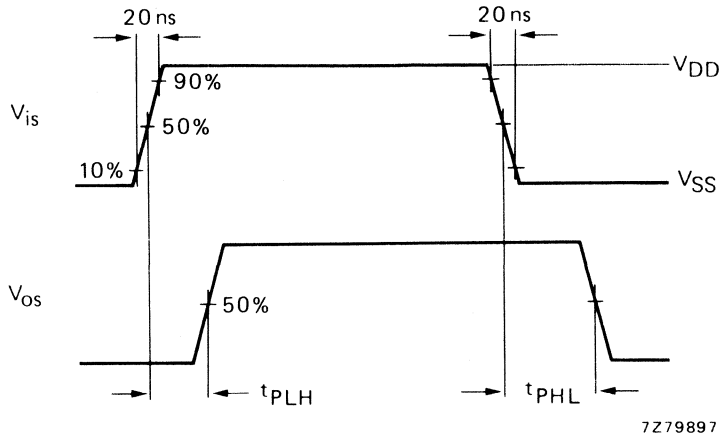
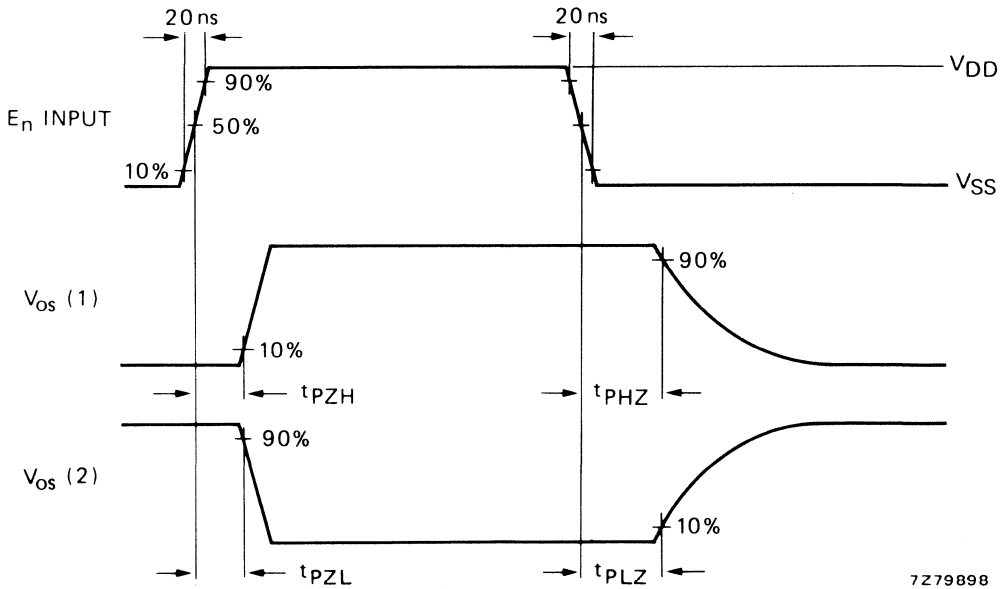


Fig. 10 Waveforms showing propagation delays from V_{is} to V_{os}.



(1) V_{is} at V_{DD}; (2) V_{is} at V_{SS}.

Fig. 11 Waveforms showing output disable and enable times.

5-STAGE JOHNSON COUNTER

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (O_0 to O_9), an active LOW output from the most significant flip-flop ($\overline{O}_{5-9}$), active HIGH and active LOW clock inputs (CP_0, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table).

When cascading counters, the $\overline{O}_{5-9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero (O_0 = $\overline{O}_{5-9}$ = HIGH; O_1 to O_9 = LOW) independent of the clock inputs (CP_0, $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

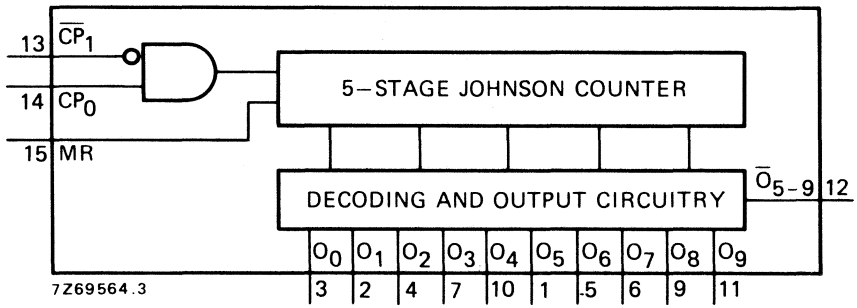


Fig. 1 Functional diagram.

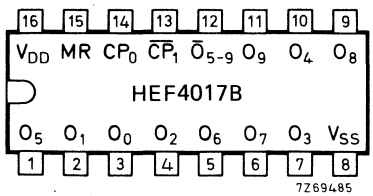


Fig. 2 Pinning diagram.

HEF4017BP : 16-lead DIL; plastic (SOT-38Z).
HEF4017BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4017BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

CP_0	clock input (LOW to HIGH triggered)
$\overline{CP}_1$	clock input (HIGH to LOW triggered)
MR	master reset input
O_0 to O_9	decoded outputs
$\overline{O}_{5-9}$	carry output (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

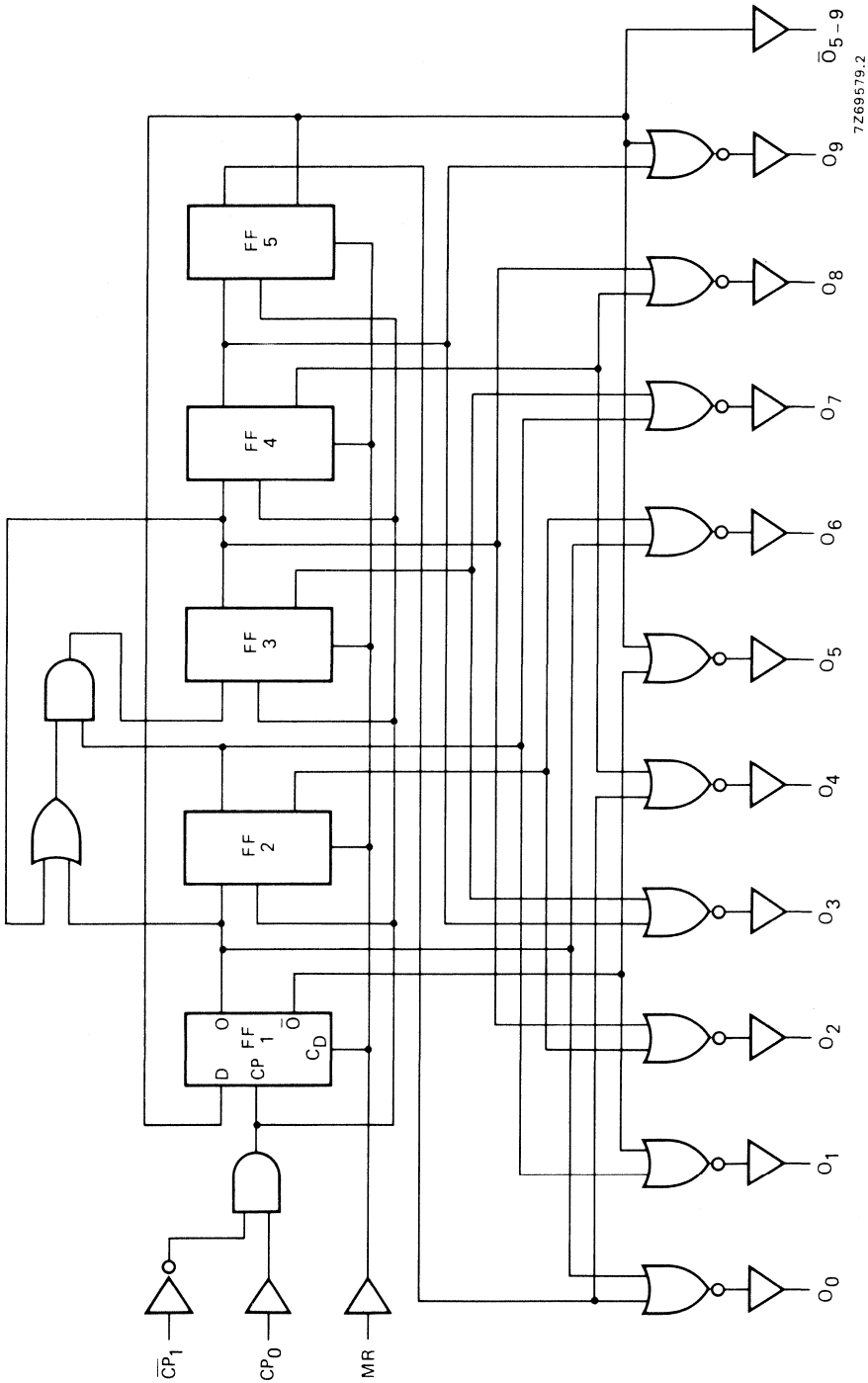


Fig. 3 Logic diagram.

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	operation
H	X	X	$O_0 = \overline{O}_{5\text{-}9}$ = H; O_1 to O_9 = L
L	H	↘	Counter advances
L	↗	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	↗	No change
L	↘	L	No change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$CP_0, \overline{CP}_1 \rightarrow O_0$ to O_9	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5\text{-}9}$	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
MR $\rightarrow$ O_1 to O_9	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
MR $\rightarrow$ $\overline{O}_{5\text{-}9}$	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
MR $\rightarrow$ O_0	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Hold times	5		90	45		ns	
$CP_0 \rightarrow \overline{CP}_1$	10	t_{hold}	40	20		ns	
	15		20	10		ns	
	5		80	40		ns	
$\overline{CP}_1 \rightarrow CP_0$	10	t_{hold}	40	20		ns	
	15		30	10		ns	
Minimum clock pulse width:	5	t_{WCPL} =	80	40		ns	
CP_0 = LOW;	10	t_{WCPH}	40	20		ns	see also waveforms
$\overline{CP}_1$ = HIGH	15		30	15		ns	Figs 4 and 5
Minimum MR pulse width; HIGH	5		50	25		ns	
	10	t_{WMRH}	30	15		ns	
	15		20	10		ns	
Recovery time for MR	5		60	30		ns	
	10	t_{RMR}	30	15		ns	
	15		20	10		ns	
Maximum clock pulse frequency	5		6	12		MHz	
	10	f_{max}	12	24		MHz	
	15		15	30		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$6000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

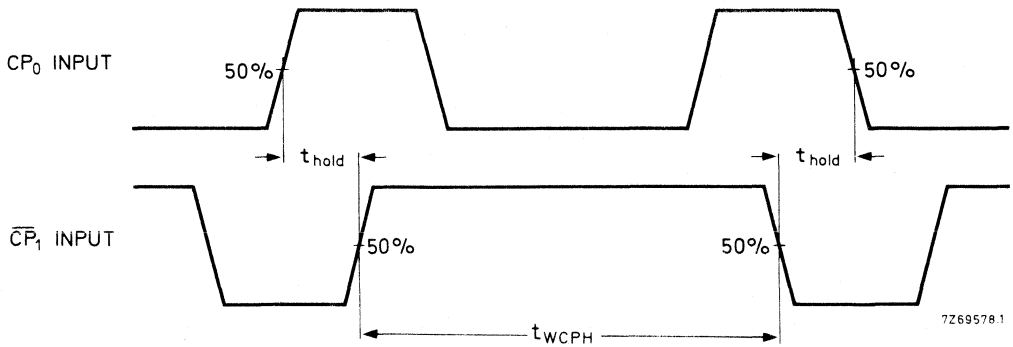


Fig. 4 Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0.
Hold times are shown as positive values, but may be specified as negative values.

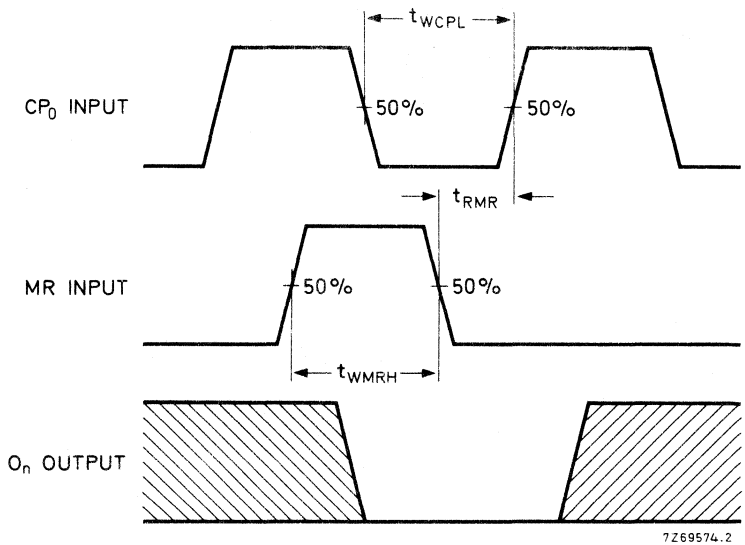


Fig. 5 Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths.

Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition.
t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

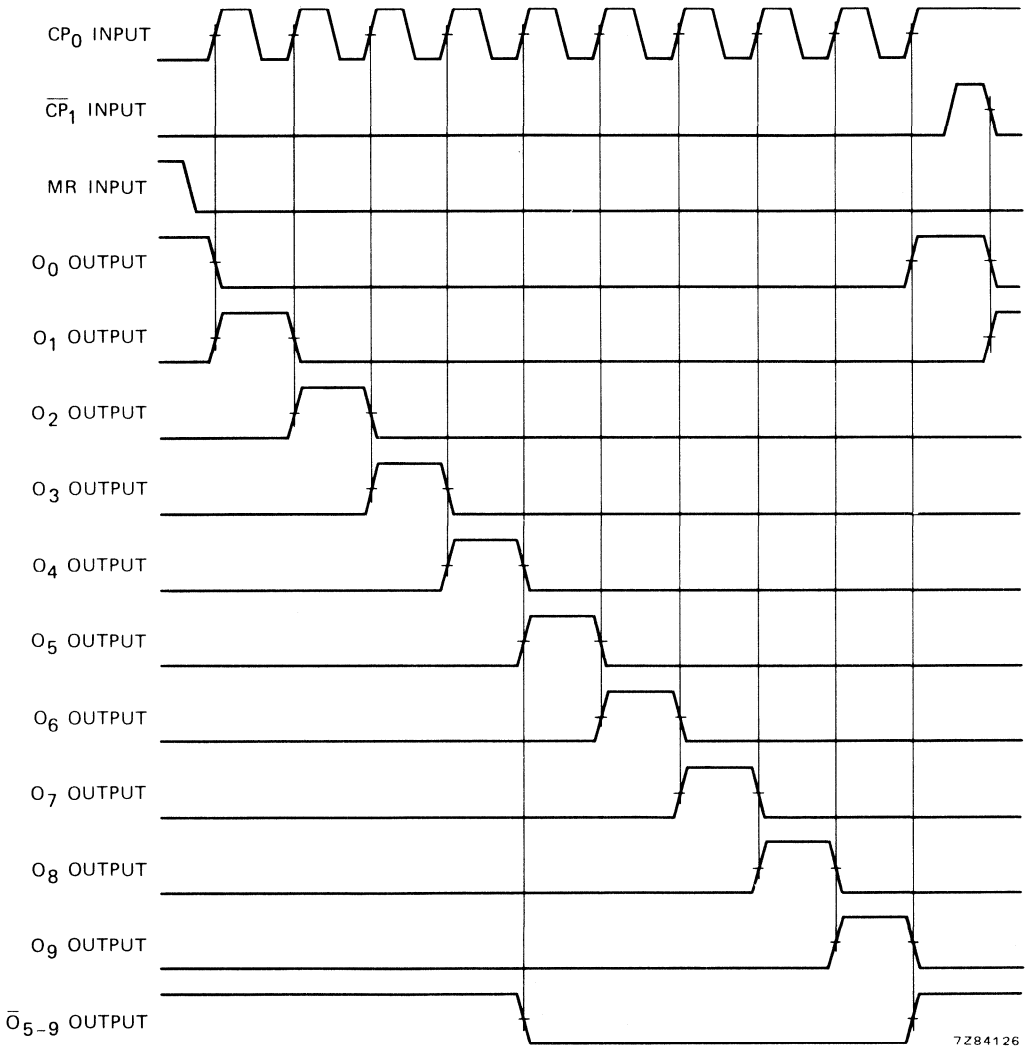


Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4017B are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer.

Figure 7 shows a technique for extending the number of decoded output states for the HEF4017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

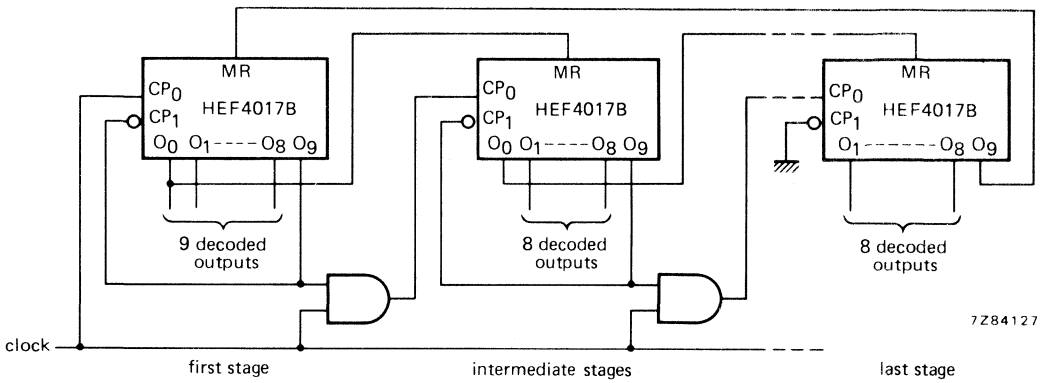


Fig. 7 Counter expansion.

Note

It is essential not to enable the counter on $\overline{CP}_1$ when CP_0 is HIGH, or on CP_0 when $\overline{CP}_1$ is LOW, as the this would cause an extra count.

PRESETTABLE DIVIDE-BY-N COUNTER

The HEF4018B is a 5-stage Johnson counter with a clock input (CP), a data input (D), an asynchronous parallel load input (PL), five parallel inputs (P_0 to P_4), five active LOW buffered outputs ($\overline{O}_0$ to $\overline{O}_4$), and an overriding asynchronous master reset input (MR).
Information on P_0 to P_4 is asynchronously loaded into the counter while PL is HIGH, independent of CP and D inputs. When P_L is LOW, the counter advances on the LOW to HIGH transition of CP. By connecting $\overline{O}_0$ to $\overline{O}_4$ to D, the counter operates as a divide-by-n counter (n = 2 to 10; see also function selection below). Each register stage is a D-type master-slave flip-flop with a set-direct/clear-direct input. An internal code correction circuit provides automatic code correction of the counter. From any illegal code the counter is in a proper counting mode within 11 clock pulses.

A HIGH on MR resets the counter ($\overline{O}_0$ to $\overline{O}_4$ = HIGH) independent of all other inputs.

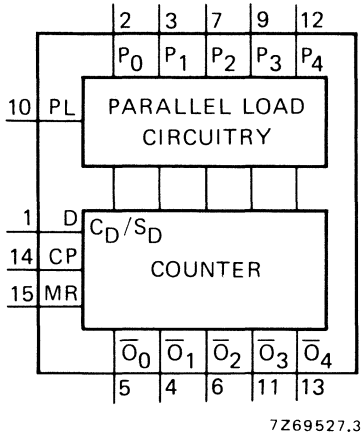


Fig. 1 Functional diagram.

FUNCTION SELECTION

counter mode; divide by	connect D input to	remarks
10 8 6 4 2	$\overline{O}_4$ $\overline{O}_3$ $\overline{O}_2$ $\overline{O}_1$ $\overline{O}_0$	no external components needed
9 7 5 3	$\overline{O}_3 \cdot \overline{O}_4$ $\overline{O}_2 \cdot \overline{O}_3$ $\overline{O}_1 \cdot \overline{O}_2$ $\overline{O}_0 \cdot \overline{O}_1$	AND gate needed; counter skips all HIGH states

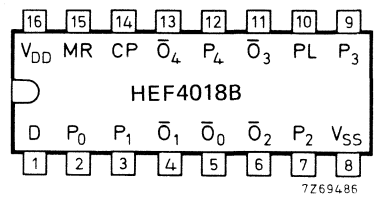


Fig. 2 Pinning diagram.

HEF4018BP : 16-lead DIL; plastic (SOT-38Z).
HEF4018BD : 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4018BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

PL	parallel load input
P_0 to P_4	parallel inputs
D	data input
CP	clock input (LOW to HIGH edge triggered)
MR	master reset input
$\overline{O}_0$ to $\overline{O}_4$	buffered output (active LOW)

APPLICATION INFORMATION

Some examples of applications for the HEF4018B are:

- Programmable divide-by-n counter
- Programmable frequency division
- Timers

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Products approved to CECC 90 104-016.

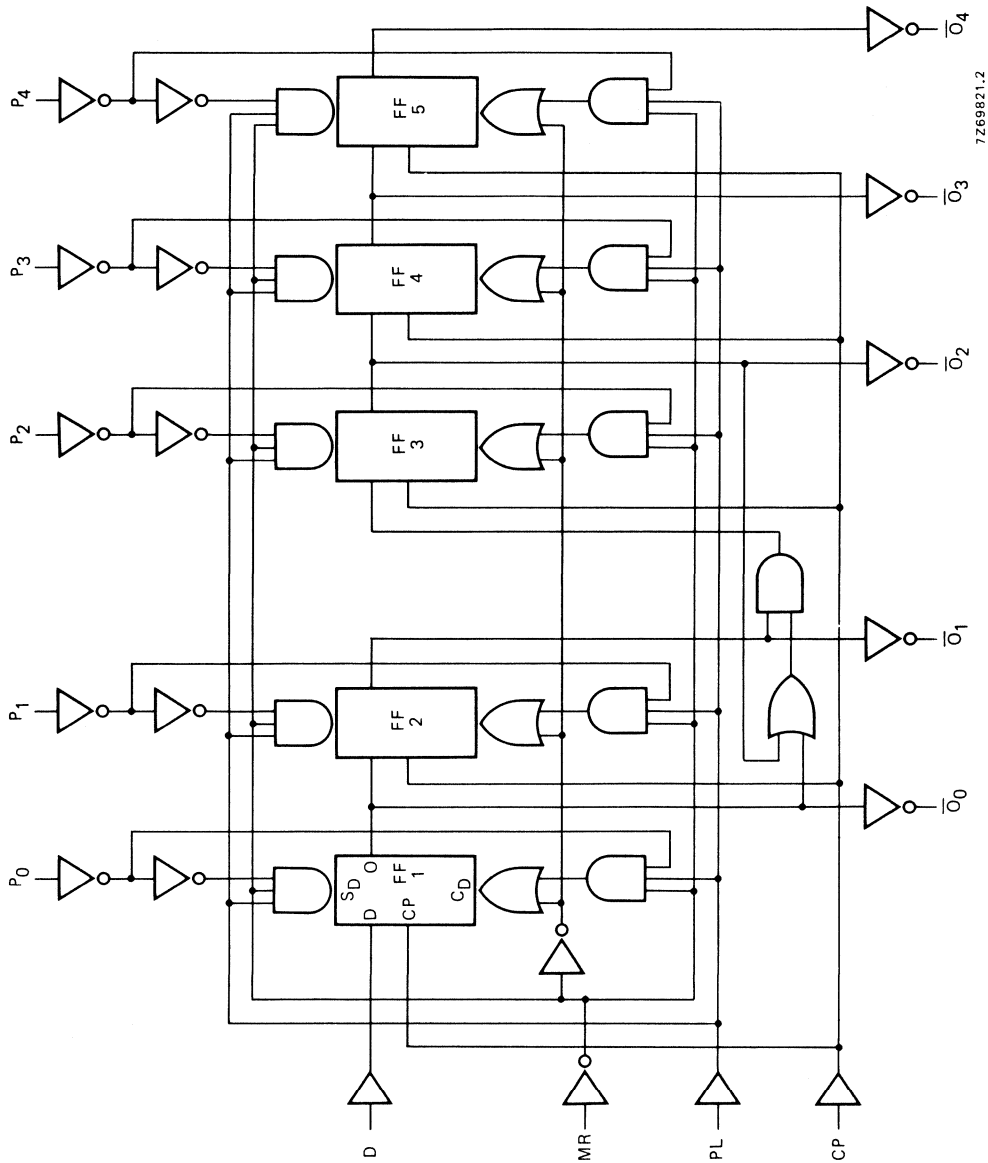


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3450\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → $\overline{O}$	5			185	370	ns	158 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	135	ns	54 ns + (0,23 ns/pF) C_L
	15			50	95	ns	42 ns + (0,16 ns/pF) C_L
	5			145	295	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	85	ns	32 ns + (0,16 ns/pF) C_L
PL → $\overline{O}$	5			205	415	ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
	5			175	350	ns	148 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	125	ns	54 ns + (0,23 ns/pF) C_L
	15			50	95	ns	42 ns + (0,16 ns/pF) C_L
MR → $\overline{O}$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Set-up time D → CP	5	t_{su}	130	65		ns	see also waveforms Figs 4, 5 and 6
	10		40	20		ns	
	15		30	15		ns	
Hold time D → CP	5	t_{hold}	20	−45		ns	
	10		5	−15		ns	
	15		5	−10		ns	
Minimum clock pulse width; LOW	5	t_{WCPL}	140	70		ns	
	10		50	25		ns	
	15		40	20		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	100	50		ns	
	10		35	20		ns	
	15		25	15		ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	145	75		ns	
	10		50	25		ns	
	15		35	20		ns	
Recovery time for MR	5	t_{RMR}	135	70		ns	
	10		40	20		ns	
	15		25	15		ns	
Recovery time for PL	5	t_{RPL}	170	85		ns	
	10		55	30		ns	
	15		40	20		ns	
Maximum clock pulse frequency	5	f_{max}	2	4		MHz	
	10		6	11		MHz	
	15		8	16		MHz	

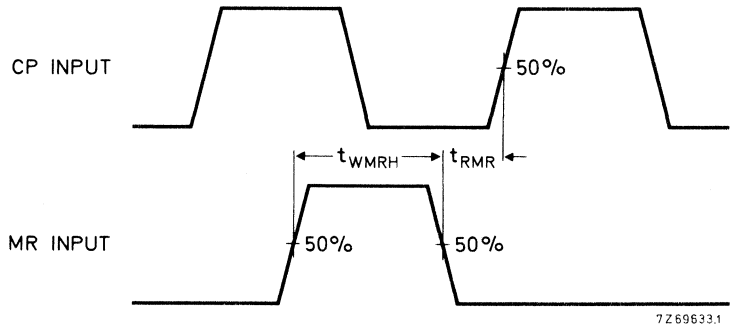


Fig. 4 Waveforms showing minimum MR pulse width and MR recovery time.

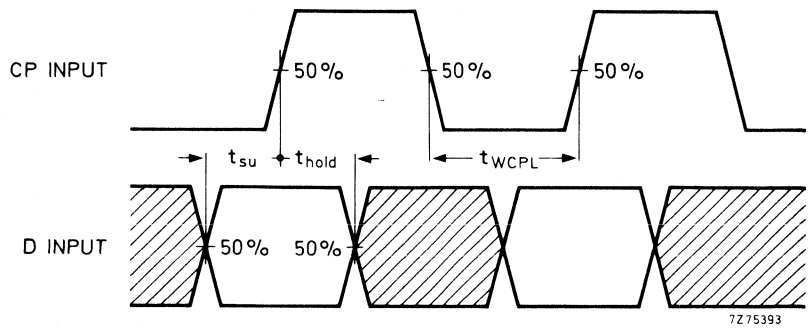


Fig. 5 Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D.

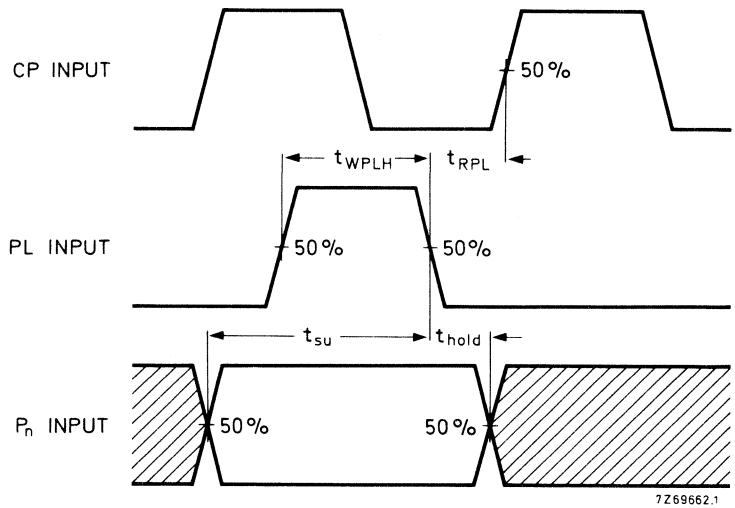


Fig. 6 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

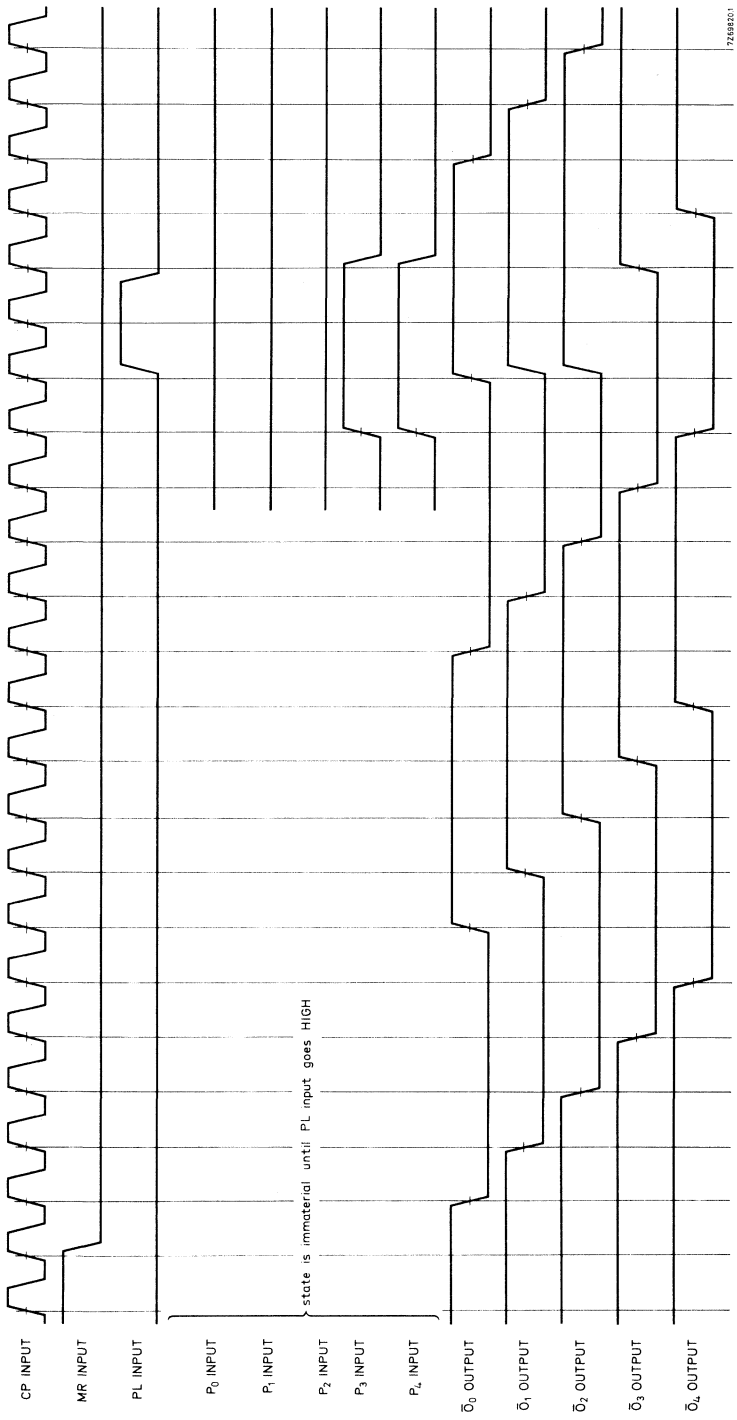


Fig. 7 Timing diagram.

Note

D input connected to $\overline{O}_4$ for decade counter configuration.

QUADRUPLE 2-INPUT MULTIPLEXER

The HEF4019B provides four multiplexing circuits with common select inputs (S_A, S_B); each circuit contains two inputs (A_n, B_n) and one output (O_n). It may be used to select four bits of information from one of two sources.

The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, output (O_n) is the logical OR of the A_n and B_n inputs ($O_n = A_n + B_n$). When S_A and S_B are LOW, output (O_n) is LOW independent of the multiplexer inputs.

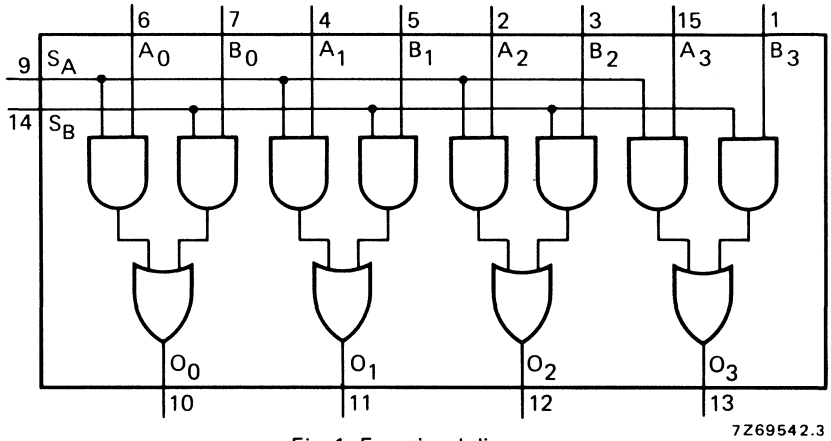
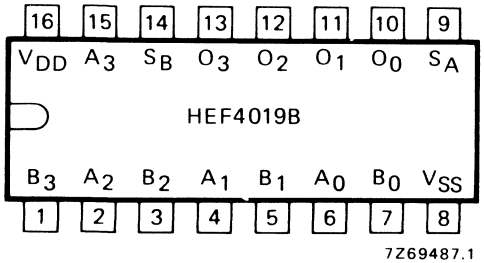


Fig. 1 Functional diagram.



HEF4019BP : 16-lead DIL; plastic (SOT-38Z).
HEF4019BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4019BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

PINNING

S_A, S_B	select inputs (active HIGH)	B_0 to B_3	multiplexer inputs
A_0 to A_3	multiplexer inputs	O_0 to O_3	multiplexer outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

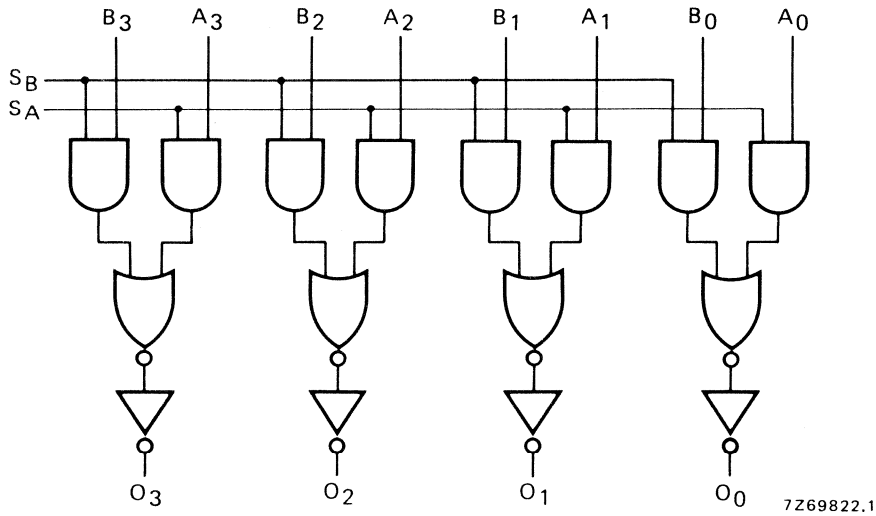


Fig. 3 Logic diagram.

TRUTH TABLE

select		inputs		output
S_A	S_B	A_n	B_n	O_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
A_n, B_n, S_A, S_B → O_n	5		70	145	ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
	5		60	130	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		15	35	ns	7 ns + (0,16 ns/pF) C_L
Output transition times						
HIGH to LOW	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1200 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5100 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	18 700 f_i + Σ($f_o C_L$) x V_{DD}^2	

APPLICATION INFORMATION

An example of an application for the HEF4019B is:

- True/complement selection.

14-STAGE BINARY COUNTER

The HEF4020B is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0, O_3 to O_{13}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. A feature of the HEF4020B is: high speed (typ. 35 MHz at V_{DD} = 15 V).

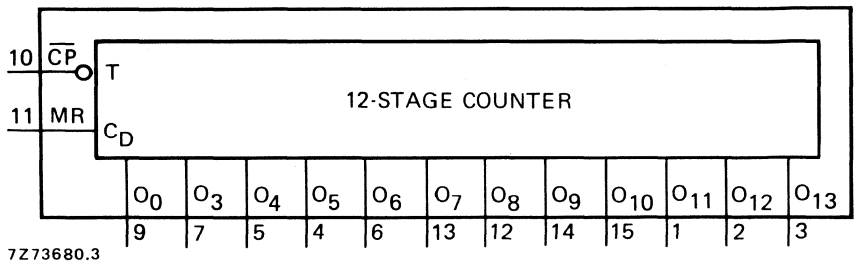


Fig. 1 Functional diagram.

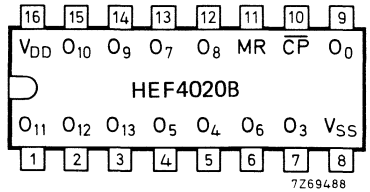


Fig. 2 Pinning diagram.

HEF4020BP : 16-lead DIL; plastic (SOT-38Z).
HEF4020BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4020BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{CP}$	clock input (HIGH to LOW edge triggered)
MR	master reset input (active HIGH)
O_0, O_3 to O_{13}	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

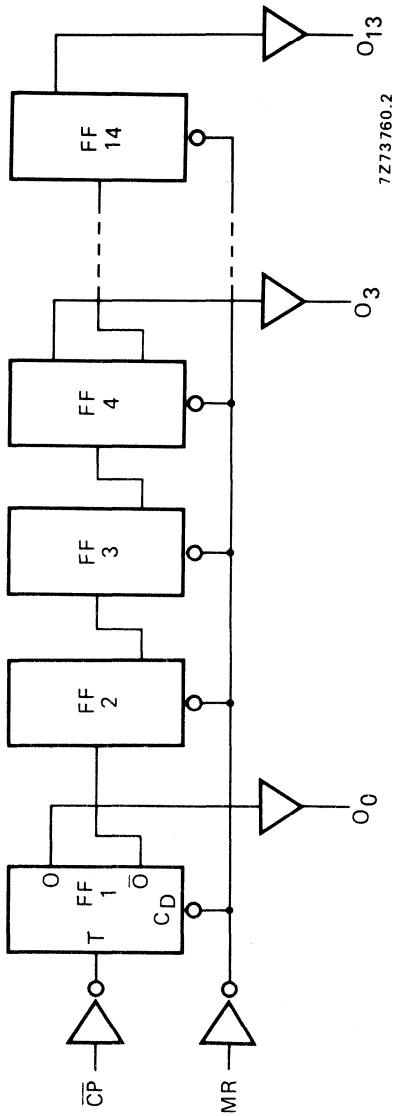


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{CP} \longrightarrow O_0$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$O_n \longrightarrow O_n + 1$	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
	5			70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
$MR \longrightarrow O_n$	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum clock pulse width; HIGH	5		50	25		ns	
	10	t_{WCPH}	25	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5		130	65		ns	
	10	t_{WMRH}	95	50		ns	
	15		90	45		ns	
Recovery time for MR	5		115	60		ns	
	10	t_{RMR}	65	35		ns	
	15		55	25		ns	
Maximum clock pulse frequency	5		5	10		MHz	
	10	f_{max}	13	25		MHz	
	15		18	35		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	600 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2800 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	8200 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

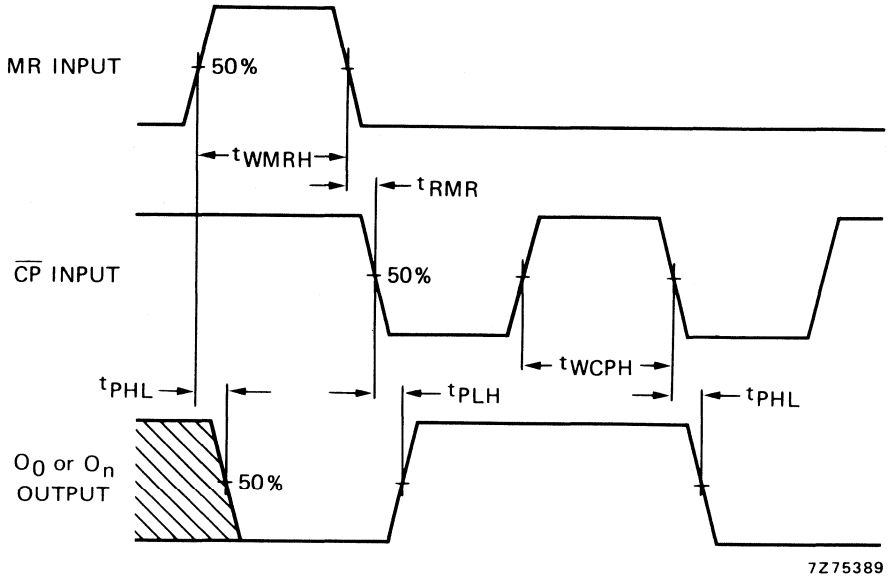


Fig. 4 Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths.

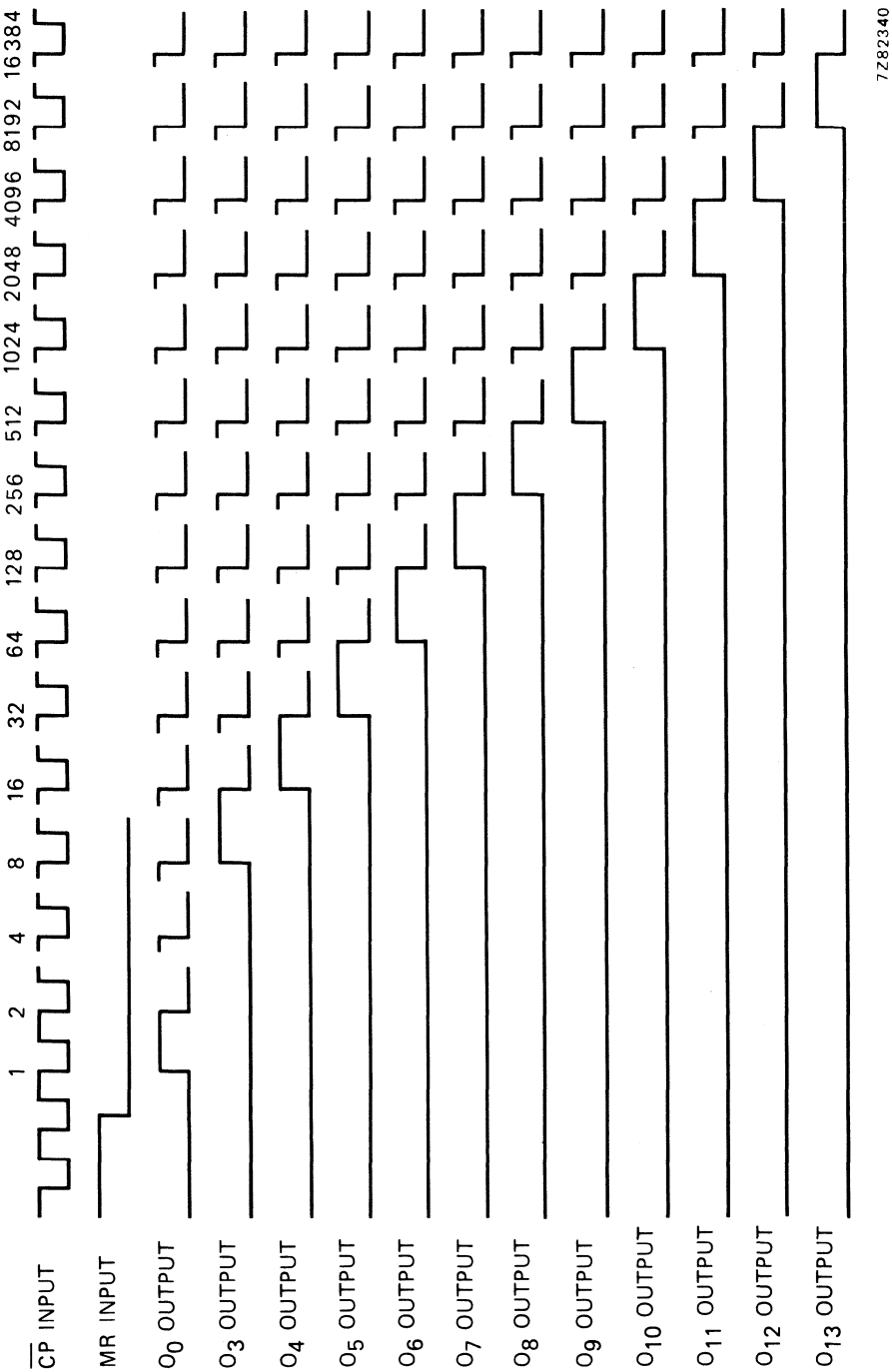


Fig. 5 Timing diagram.

8-BIT STATIC SHIFT REGISTER

The HEF4021B is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (D_S), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (P_0 to P_7) and buffered parallel outputs from the last three stages (O_5 to O_7).

Each register stage is a D-type master-slave flip-flop with a set direct/clear direct input. Information on P_0 to P_7 is asynchronously loaded into the register while PL is HIGH, independent of CP and DS. When PL is LOW, data on D_S is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

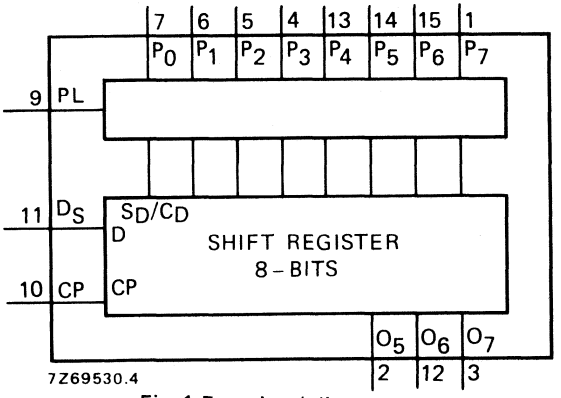


Fig. 1 Functional diagram.

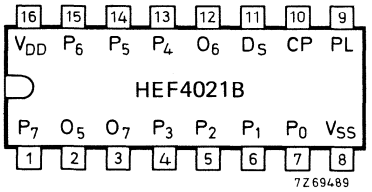


Fig. 2 Pinning diagram.

HEF4021BP : 16-lead DIL; plastic (SOT-38Z).
HEF4021BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4021BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

PL	parallel load input
P_0 to P_7	parallel data inputs
D_S	serial data input
CP	clock input (LOW to HIGH edge-triggered)
O_5 to O_7	buffered parallel outputs from the last three stages

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

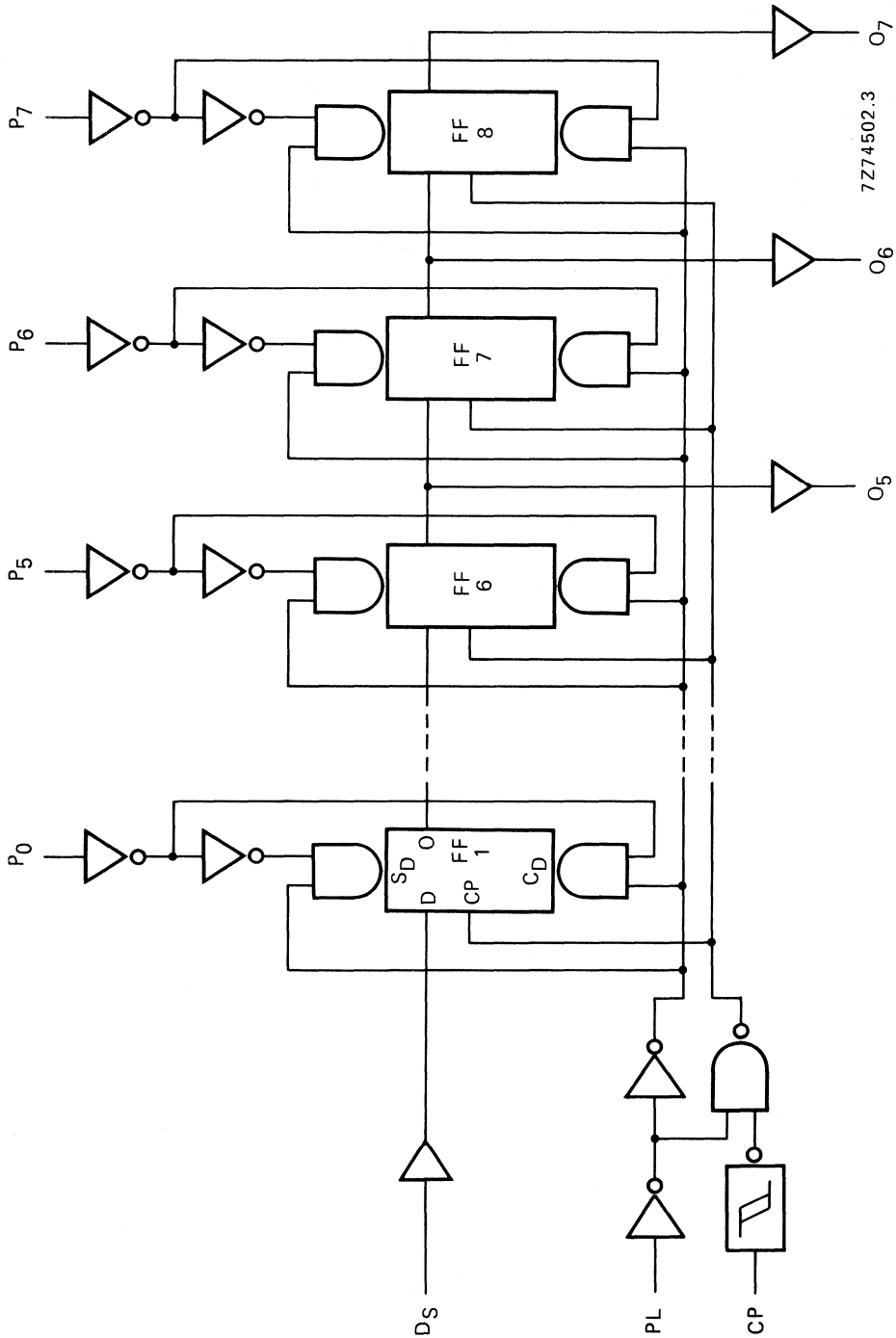


Fig. 3 Logic diagram.

FUNCTION TABLES

Serial operation

	inputs			outputs		
n	CP	D_S	PL	O_5	O_6	O_7
1	∫	D_1	L	X	X	X
2	∫	D_2	L	X	X	X
3	∫	D_3	L	X	X	X
6	∫	X	L	D_1	X	X
7	∫	X	L	D_2	D_1	X
8	∫	X	L	D_3	D_2	D_1
	⌝	X	L	no change		

Parallel operation

	inputs			outputs		
n	CP	D_S	PL	O_5	O_6	O_7
	X	X	H	P_5	P_6	P_7

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌝ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			125	250	ns	98 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF)C_L
	15			40	80	ns	32 ns + (0,16 ns/pF)C_L
	5			115	230	ns	88 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF)C_L
	15			40	80	ns	32 ns + (0,16 ns/pF)C_L
PL → O_n	5			120	240	ns	93 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF)C_L
	15			40	80	ns	32 ns + (0,16 ns/pF)C_L
	5			105	210	ns	78 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF)C_L
	15			40	80	ns	32 ns + (0,16 ns/pF)C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Set-up times	5		25	−15		ns	see also waveforms Figs 4 and 5
$D_S \rightarrow CP$	10	t_{su}	25	−10		ns	
	15		15	−5		ns	
	5		50	25		ns	
$P_n \rightarrow PL$	10	t_{su}	30	10		ns	
	15		20	5		ns	
Hold times	5		40	20		ns	
$D_S \rightarrow CP$	10	t_{hold}	20	10		ns	
	15		15	8		ns	
	5		15	−10		ns	
$P_n \rightarrow PL$	10	t_{hold}	15	0		ns	
	15		15	0		ns	
Minimum clock pulse width; LOW	5		70	35		ns	
	10	t_{WCPL}	30	15		ns	
	15		24	12		ns	
Minimum PL pulse width; HIGH	5		70	35		ns	
	10	t_{WPLH}	30	15		ns	
	15		24	12		ns	
Recovery time for PL	5		50	10		ns	
	10	t_{RPL}	40	5		ns	
	15		35	5		ns	
Maximum clock pulse frequency	5		6	13		MHz	
	10	f_{max}	15	30		MHz	
	15		20	40		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$12\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

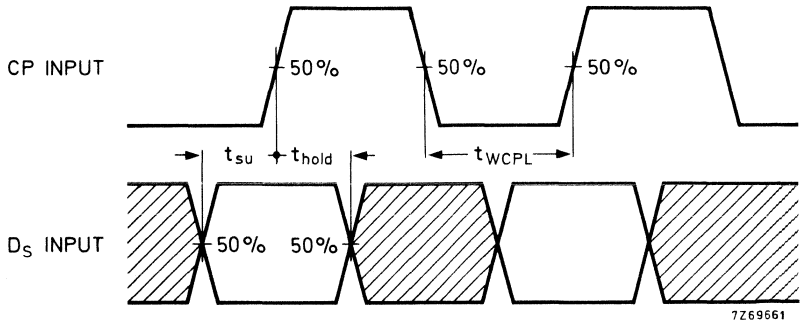


Fig. 4 Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D_S.

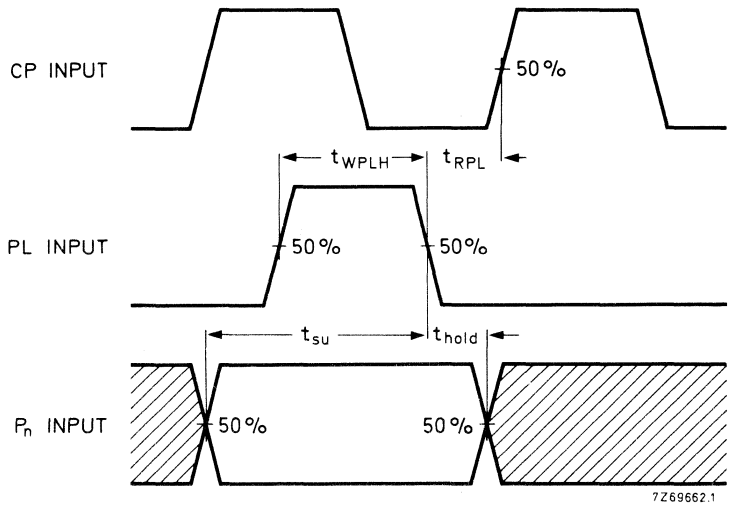


Fig. 5 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

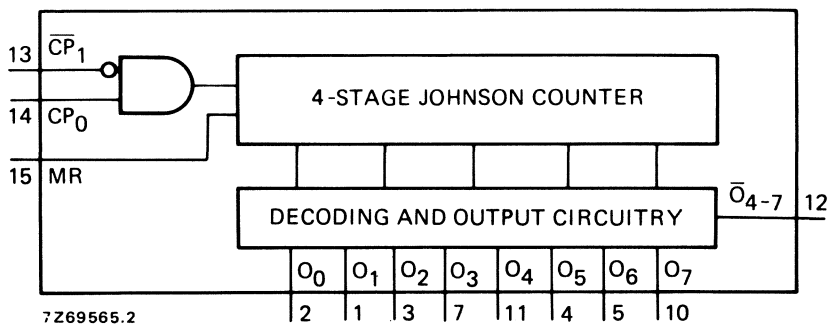
4-STAGE DIVIDE-BY-8 JOHNSON COUNTER

The HEF4022B is a 4-stage divide-by-8 Johnson counter with eight spike-free decoded active HIGH outputs (O_0 to O_7), an active LOW output from the most significant flip-flop ($\overline{O}_{4-7}$), active HIGH and active LOW clock inputs (CP_0, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table). Either CP_0 or $\overline{CP}_1$ may be used as clock input to the counter and the other clock input may be used as a clock enable input. When cascading counters, the $\overline{O}_{4-7}$ output, which is LOW while the counter is in states, 4, 5, 6 and 7, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{4-7}$ = HIGH; O_1 to O_7 = LOW) independent of the clock inputs (CP_0, $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit, following any illegal code the counter returns to a proper counting mode within 11 clock pulses.



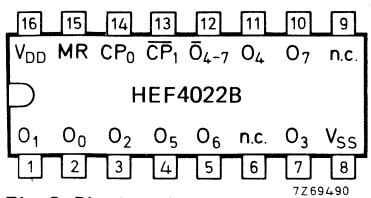


Fig. 2 Pinning diagram.

Fig. 1 Functional diagram.

HEF4022BP : 16-lead DIL; plastic (SOT-38Z).
HEF4022BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4022BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

CP_0	clock input (LOW to HIGH; edge-triggered)
$\overline{CP}_1$	clock input (HIGH to LOW; edge-triggered)
MR	master reset input
O_0 to O_7	decoded outputs
$\overline{O}_{4-7}$	carry output (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

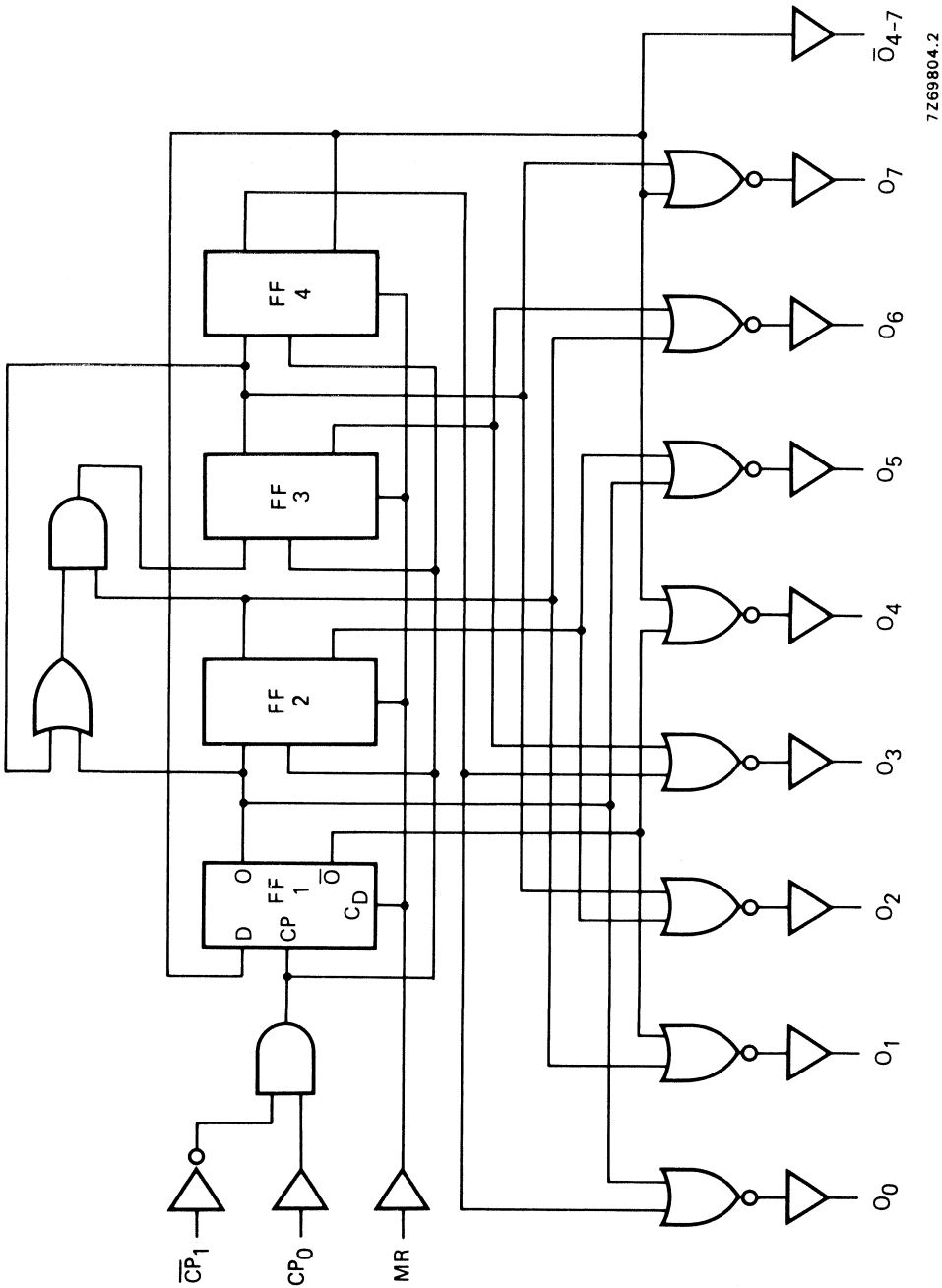


Fig. 3 Logic diagram.

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	operation
H	X	X	$O_0 = \overline{O}_{4\text{-}7} = H$; O_1 to $O_7 = L$
L	H	↘	Counter advances
L	↗	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	↗	No change
L	↘	L	No change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP_0, $\overline{CP}_1$ → O_n	5			195	390 ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	145 ns	64 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
	5			245	485 ns	218 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		95	195 ns	84 ns + (0,23 ns/pF) C_L
	15			60	125 ns	52 ns + (0,16 ns/pF) C_L
CP_0, $\overline{CP}_1$ → $\overline{O}_{4\text{-}7}$	5			245	485 ns	218 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	185 ns	79 ns + (0,23 ns/pF) C_L
	15			60	120 ns	52 ns + (0,16 ns/pF) C_L
	5			190	380 ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	145 ns	64 ns + (0,23 ns/pF) C_L
	15			50	105 ns	42 ns + (0,16 ns/pF) C_L
MR → O_1 to O_7	5			130	260 ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105 ns	44 ns + (0,23 ns/pF) C_L
	15			40	75 ns	32 ns + (0,16 ns/pF) C_L
MR → O_0	5			130	260 ns	103 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	105 ns	44 ns + (0,23 ns/pF) C_L
	15			40	75 ns	32 ns + (0,16 ns/pF) C_L
MR → $\overline{O}_{4\text{-}7}$	5			110	220 ns	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90 ns	34 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
Output transition times						
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Hold times							see also waveforms Figs 4 and 5
$CP_0 \rightarrow \overline{CP}_1$	5	t_{hold}	140	70		ns	
	10		50	25		ns	
	15		30	15		ns	
$\overline{CP}_1 \rightarrow CP_0$	5	t_{hold}	170	85		ns	
	10		60	30		ns	
	15		40	20		ns	
Minimum clock pulse width	5	t_{WCP}	75	35		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	70	35		ns	
	10		30	15		ns	
	15		20	10		ns	
Recovery time for MR	5	t_{RMR}	30	10		ns	
	10		15	5		ns	
	15		10	5		ns	
Maximum clock pulse frequency	5	f_{max}	3	6		MHz	
	10		8	16		MHz	
	15		12	24		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$475\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$6700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

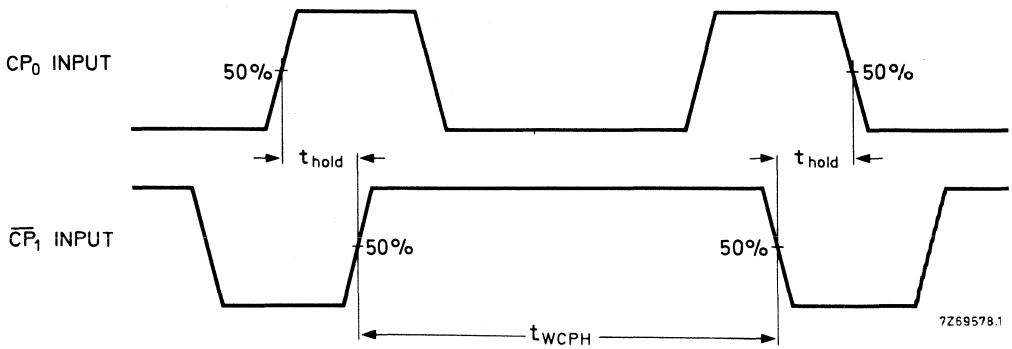


Fig. 4 Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0.
Hold times are shown as positive values, but may be specified as negative values.

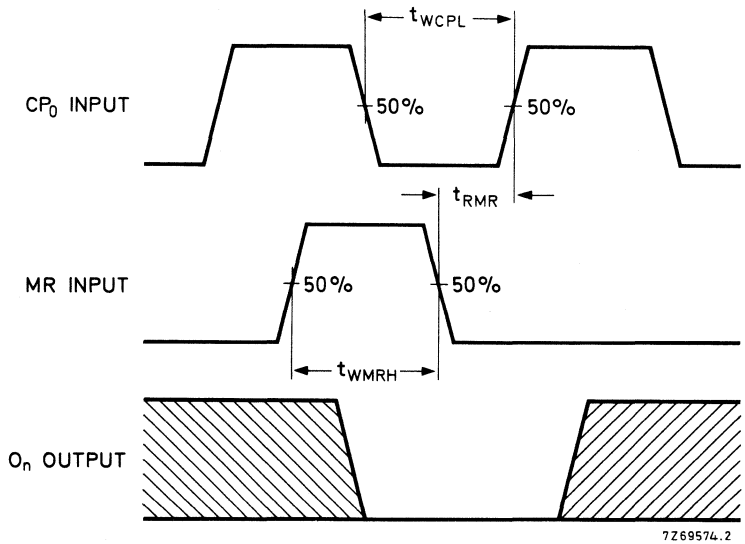


Fig. 5 Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths.

Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition.
t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

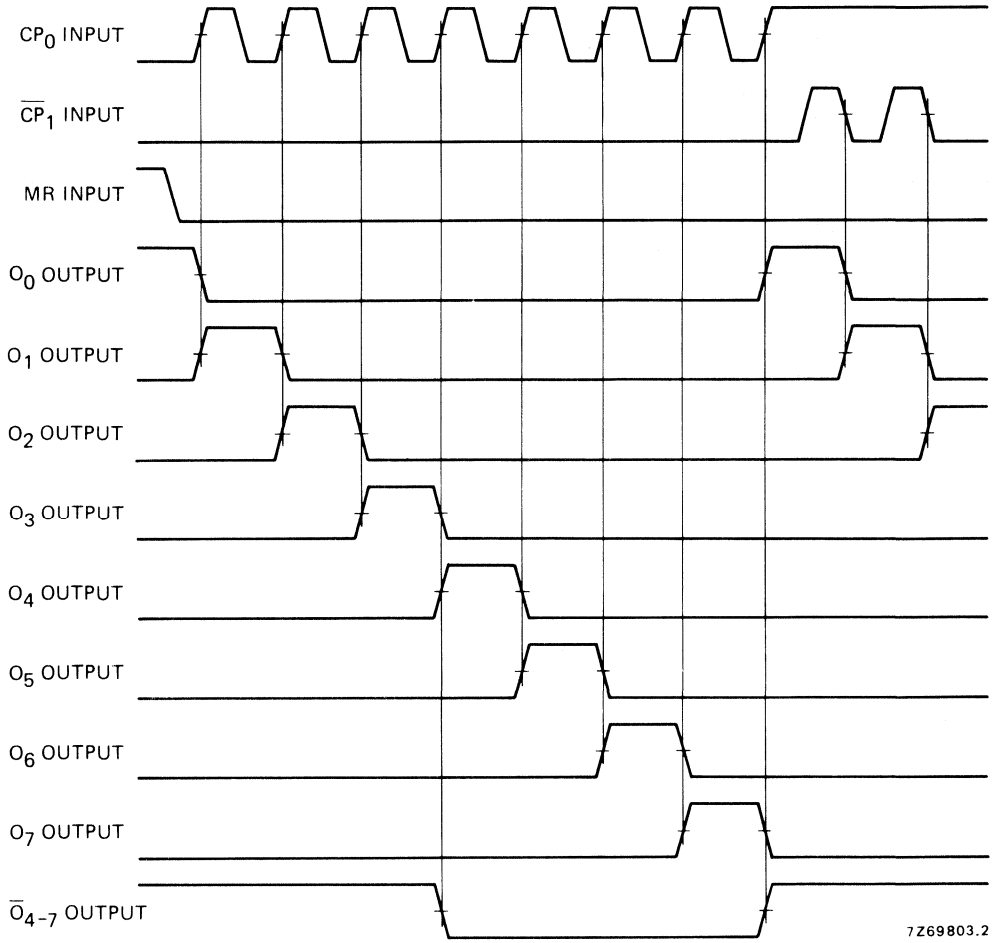


Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some of the features of the HEF4022B are:

- High speed
- Spike-free decoded outputs
- Carry output for cascading

Figure 7 shows a technique for extending the number of decoded output states for the HEF4022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

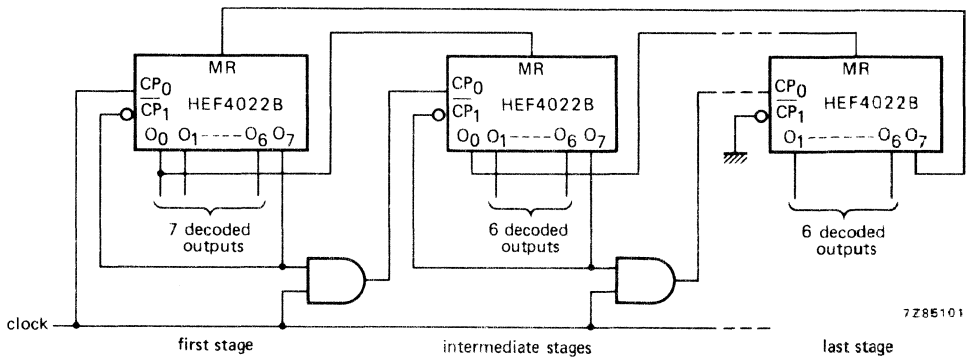


Fig. 7 Counter expansion.

TRIPLE 3-INPUT NAND GATE

The HEF4023B provides the positive triple 3-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

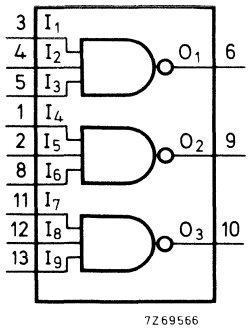


Fig. 1 Functional diagram.

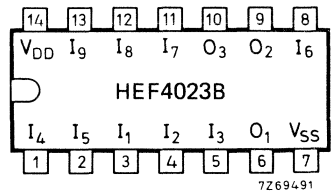


Fig. 2 Pinning diagram.

HEF4023BP : 14-lead DIL; plastic (SOT-27).
HEF4023BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4023BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

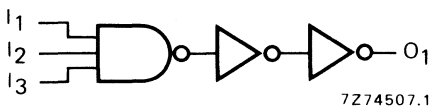


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		65	135	ns	38 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
	5		65	130	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	45	ns	17 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + 1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1200 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5500 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	16 400 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

7-STAGE BINARY COUNTER

The HEF4024B is a 7-stage binary ripple counter with a clock input ($\overline{CP}$), and overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (O_0 to O_6). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of $\overline{CP}$. Each counter stage is a static toggle flip-flop.

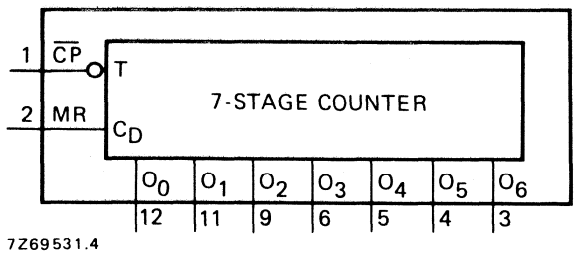


Fig. 1 Functional diagram.

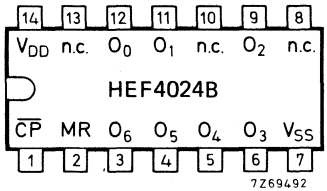


Fig. 2 Pinning diagram.

HEF4024BP : 14-lead DIL; plastic (SOT-27).
HEF4024BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4024BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

PINNING

$\overline{CP}$	clock input (HIGH to LOW triggered)
MR	master reset input
O_0 to O_6	buffered parallel outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4024B are:

- Frequency dividers
- Time delay circuits

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

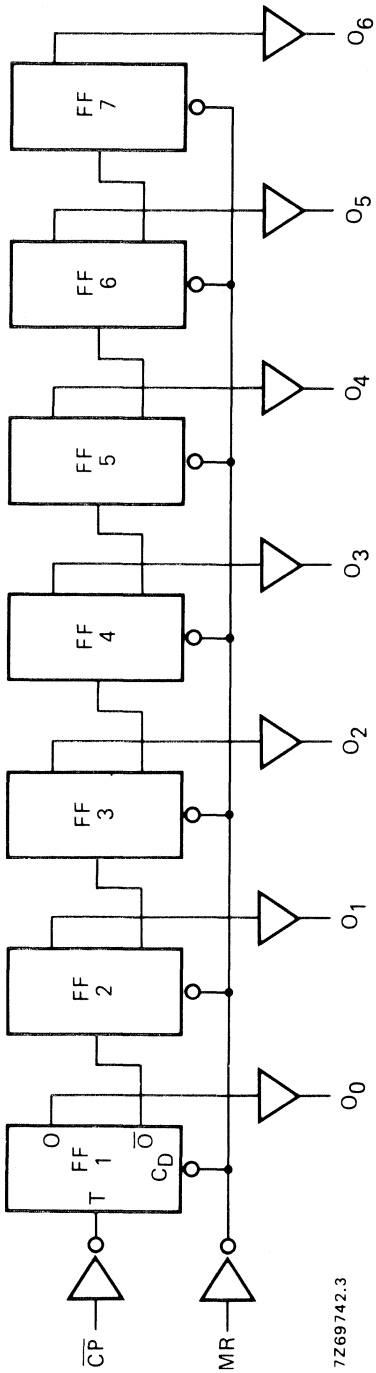


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{CP} \rightarrow O_0$	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	75	ns	29 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	85	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$O_n \rightarrow O_n + 1$	5			60	120	ns	33 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
	5			50	100	ns	23 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		20	40	ns	9 ns + (0,23 ns/pF) C_L
	15			15	30	ns	7 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum clock	5		60	30		ns	
pulse width; HIGH	10	t_{WCPH}	30	15		ns	
	15		20	10		ns	
Minimum MR	5		80	40		ns	
pulse width; HIGH	10	t_{WMRH}	35	20		ns	
	15		25	15		ns	
Recovery time	5		20	10		ns	
for MR	10	t_{RMR}	15	5		ns	
	15		15	5		ns	
Maximum clock	5		5	10		MHz	
pulse frequency	10	f_{max}	13	25		MHz	
	15		18	35		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	500 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2100 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	5200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

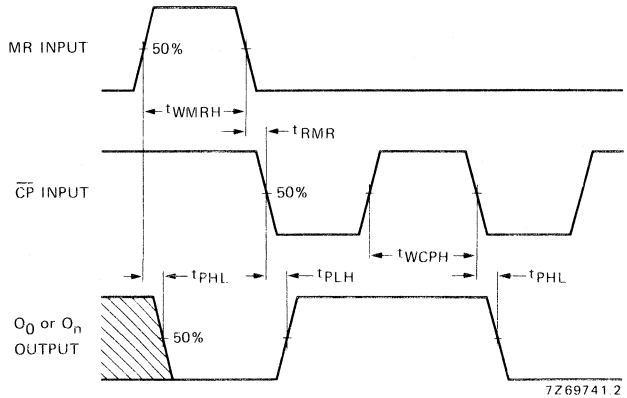


Fig. 4 Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths and recovery time for MR.

TRIPLE 3-INPUT NOR GATE

The HEF4025B provides the positive triple 3-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

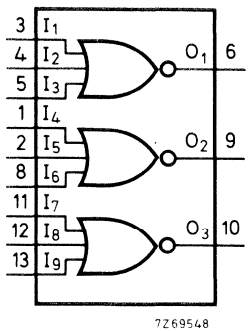


Fig. 1 Functional diagram.

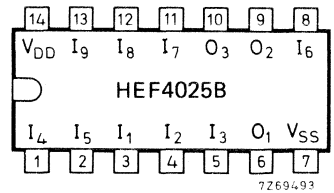


Fig. 2 Pinning diagram.

HEF4025BP : 14-lead DIL; plastic (SOT-27).
HEF4025BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4025BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

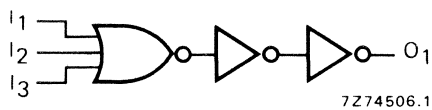


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		70	135	ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	55	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		60	120	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		15	35	ns	7 ns + (0,16 ns/pF) C_L
Output transition times						
HIGH to LOW	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	900 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	10 900 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

DUAL JK FLIP-FLOP

The HEF4027B is a dual JK flip-flop which is edge-triggered and features indepedent set direct (S_D), clear direct (C_D), clock (CP) inputs and outputs (O,$\overline{O}$). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

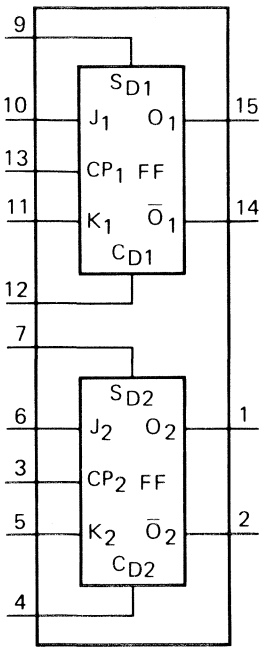


Fig. 1 Functional diagram.

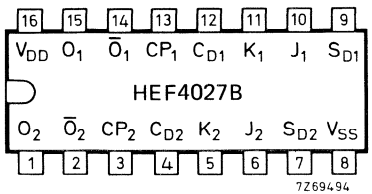


Fig. 2 Pinning diagram.

FUNCTION TABLES

inputs					outputs	
S_D	C_D	CP	J	K	O	$\overline{O}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H

inputs					outputs	
S_D	C_D	CP	J	K	O_{n+1}	$\overline{O}_{n+1}$
L	L	∫	L	L	no change	
L	L	∫	H	L	H	L
L	L	∫	L	H	L	H
L	L	∫	H	H	$\overline{O}_n$	O_n

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
O_{n+1} = state after clock positive transition

PINNING

J,K synchronous inputs
CP clock input (L to H edge-triggered)
S_D asynchronous set-direct input (active HIGH)
C_D asynchronous clear-direct input (active HIGH)
O true output
$\overline{O}$ complement output

HEF4027BP : 16-lead DIL; plastic (SOT-38Z).
HEF4027BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4027BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category FLIP-FLOPS

see Family Specifications

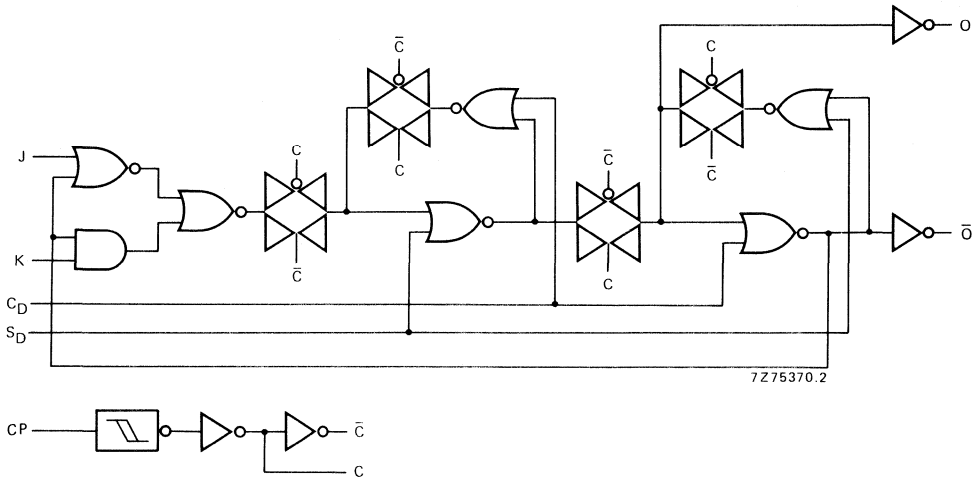


Fig. 3 Logic diagram (one flip-flop).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O, $\overline{O}$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	27 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
S_D → O	5			70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
C_D → O	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	33 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
S_D → $\overline{O}$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
C_D → $\overline{O}$	5			75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		50	25		ns	
J, K → CP	10	t_{su}	30	10		ns	
	15		20	5		ns	
Hold time	5		25	0		ns	
J, K → CP	10	t_{hold}	20	0		ns	
	15		15	5		ns	
Minimum clock	5		80	40		ns	see also waveforms Figs 4 and 5
pulse width; LOW	10	t_{WCPL}	30	15		ns	
	15		24	12		ns	
Minimum S_D, C_D	5		90	45		ns	
pulse width; HIGH	10	t_{WSDH}, t_{WCDH}	40	20		ns	
	15		30	15		ns	
Recovery time	5		20	−15		ns	
for S_D, C_D	10	t_{RSD}, t_{RCD}	15	−10		ns	
	15		10	−5		ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Maximum clock pulse frequency J = K = HIGH	5	f_{max}	4	8	MHz	see also waveforms Fig. 4
	10		12	25	MHz	
	15		15	30	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

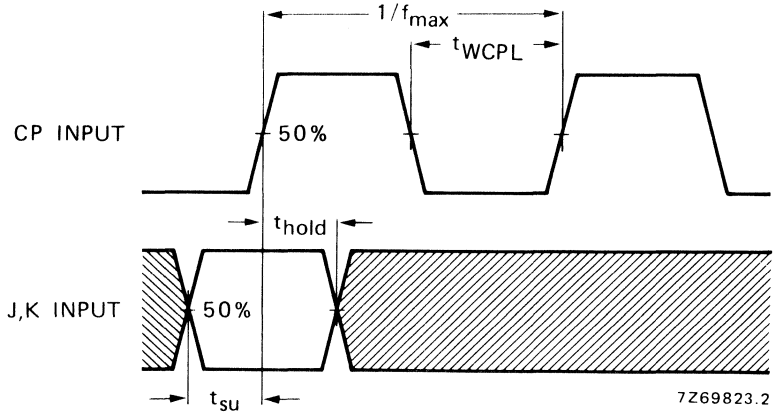


Fig. 4 Waveforms showing set-up times, hold times and minimum clock pulse width.
Set-up and hold times are shown as positive values but may be specified as negative values.

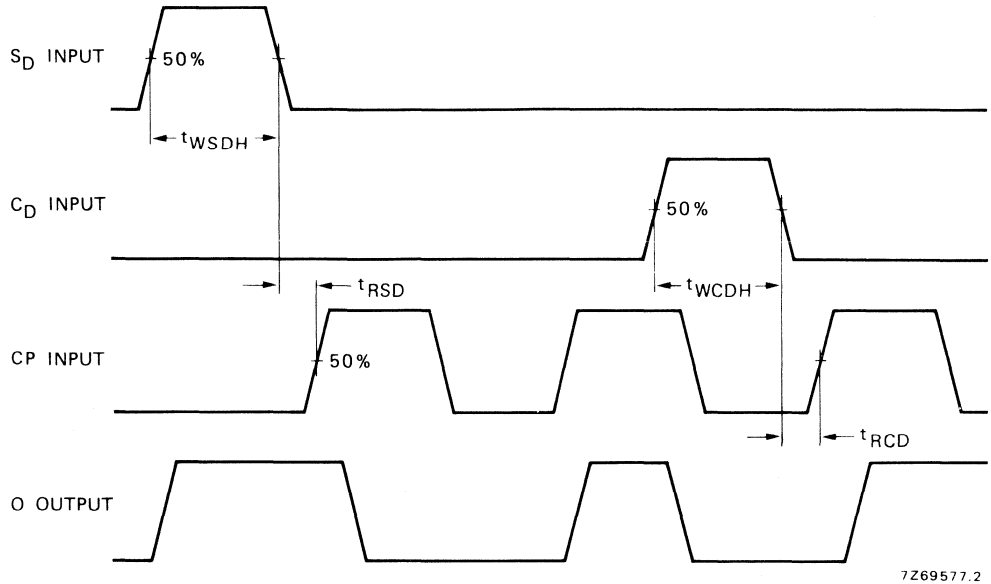


Fig. 5 Waveforms showing recovery times for S_D and C_D; minimum S_D and C_D pulse widths.

APPLICATION INFORMATION

Some examples of applications for the HEF4027B are:

- Registers
- Counters
- Control circuits

1-OF-10 DECODER

The HEF4028B is a 4-bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs A_0 to A_3 causes the selected output to be HIGH, the other nine will be LOW. If desired, the device may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs A_0, A_1 and A_2 selecting an output O_0 to O_7. Input A_3 then becomes an active LOW enable, forcing the selected output LOW when A_3 is HIGH. The HEF4028B may also be used as an 8-output (O_0 to O_7) demultiplexer with A_0 to A_2 as address inputs and A_3 as an active LOW data input. The outputs are fully buffered for best performance.

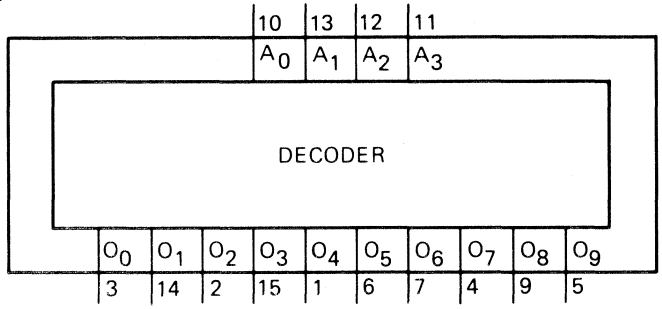


Fig.1 Functional diagram.

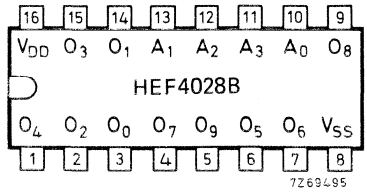


Fig.2 Pinning diagram

HEF4028BP : 16-lead DIL; plastic (SOT-38Z).
HEF4028BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4028BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

A_0 to A_3 address inputs, 1-2-4-8 BCD
O_0 to O_9 outputs (active HIGH)

FAMILY DATA

I_{DD} LIMITS category MSI | see Family Specifications

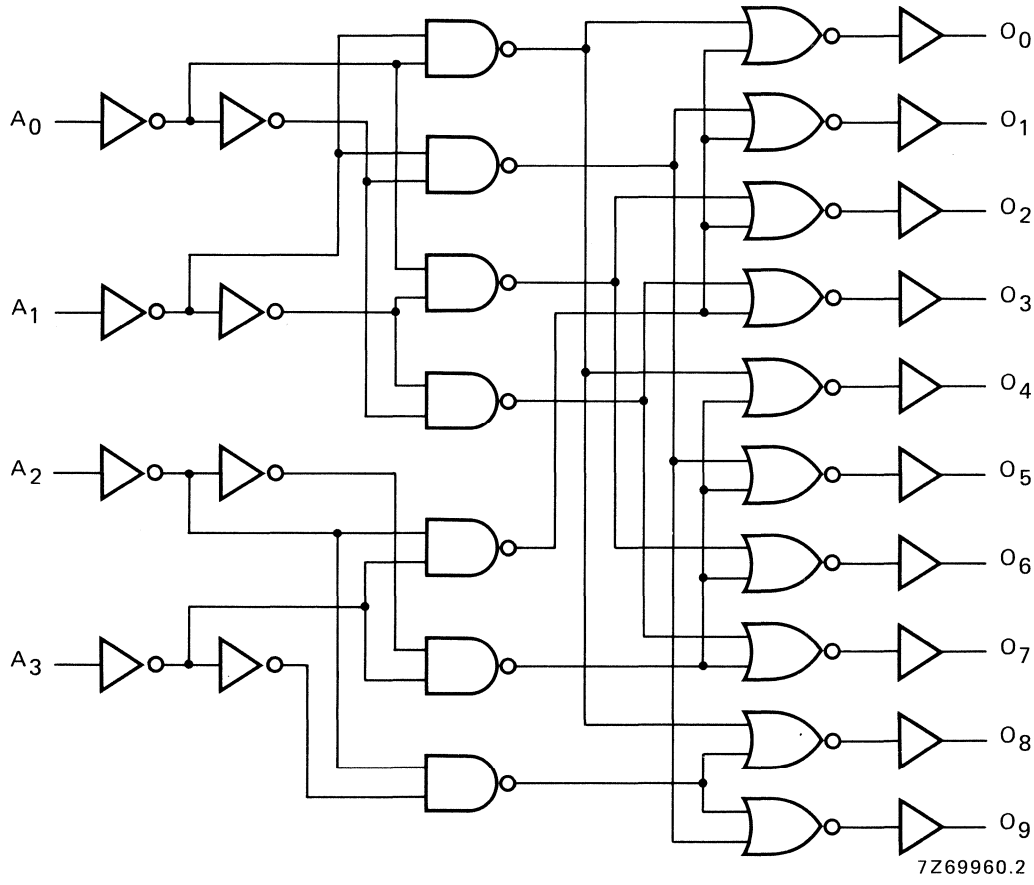


Fig. 3 Logic diagram.

TRUTH TABLE

inputs				outputs										
A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	
L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	H	L	L	L	L	L	L	H	L	L	L	L	L	
L	H	L	H	L	L	L	L	L	H	L	L	L	L	
L	H	H	L	L	L	L	L	L	L	H	L	L	L	
L	H	H	H	L	L	L	L	L	L	L	H	L	L	
H	L	L	L	L	L	L	L	L	L	L	L	H	L	
H	L	L	H	L	L	L	L	L	L	L	L	L	H	
H	L	H	L	L	L	L	L	L	L	L	L	L	L	*
H	L	H	H	L	L	L	L	L	L	L	L	L	L	*
H	H	L	L	L	L	L	L	L	L	L	L	L	L	*
H	H	L	H	L	L	L	L	L	L	L	L	L	L	*
H	H	H	L	L	L	L	L	L	L	L	L	L	L	*
H	H	H	H	L	L	L	L	L	L	L	L	L	L	*

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

* Extraordinary states.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$A_n \rightarrow O_n$	5		100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	350 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2 200 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	7 350 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

SYNCHRONOUS UP/DOWN COUNTER, BINARY/DECADE COUNTER

The HEF4029B is a synchronous edge-triggered up/down 4-bit binary/BCD decade counter with a clock input (CP), an active LOW count enable input ($\overline{CE}$), an up/down control input (UP/$\overline{DN}$), a binary/decade control input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH parallel load input (PL), four parallel data inputs (P_0 to P_3), four parallel buffered outputs (O_0 to O_3) and an active LOW terminal count output ($\overline{TC}$).

Information on P_0 to P_3 is asynchronously loaded into the counter while PL is HIGH, independent of CP.

The counter is advanced one count on the LOW to HIGH transition of CP when $\overline{CE}$ and PL are LOW. The $\overline{TC}$ signal is normally HIGH and goes LOW when the counter reaches its maximum count in the UP mode, or the minimum count in the DOWN mode provided $\overline{CE}$ is LOW.

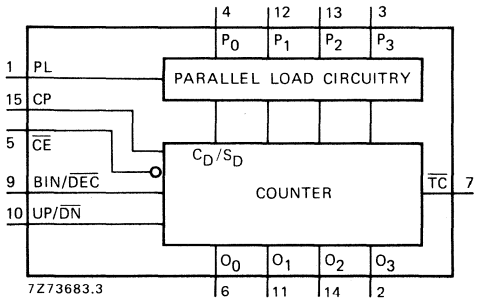


Fig. 1 Functional diagram.

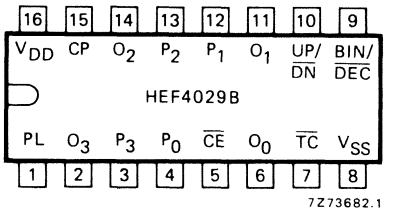


Fig. 2 Pinning diagram.

HEF4029BP : 16-lead DIL; plastic (SOT-38Z).
HEF4029BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4029BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

PL	parallel load input
P_0 to P_3	parallel data inputs
BIN/$\overline{DEC}$	binary/decade control input
UP/$\overline{DN}$	up/down control input
$\overline{CE}$	count enable input (active LOW)
CP	clock input (LOW to HIGH, edge triggered)
O_0 to O_3	buffered parallel outputs
$\overline{TC}$	terminal count output (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

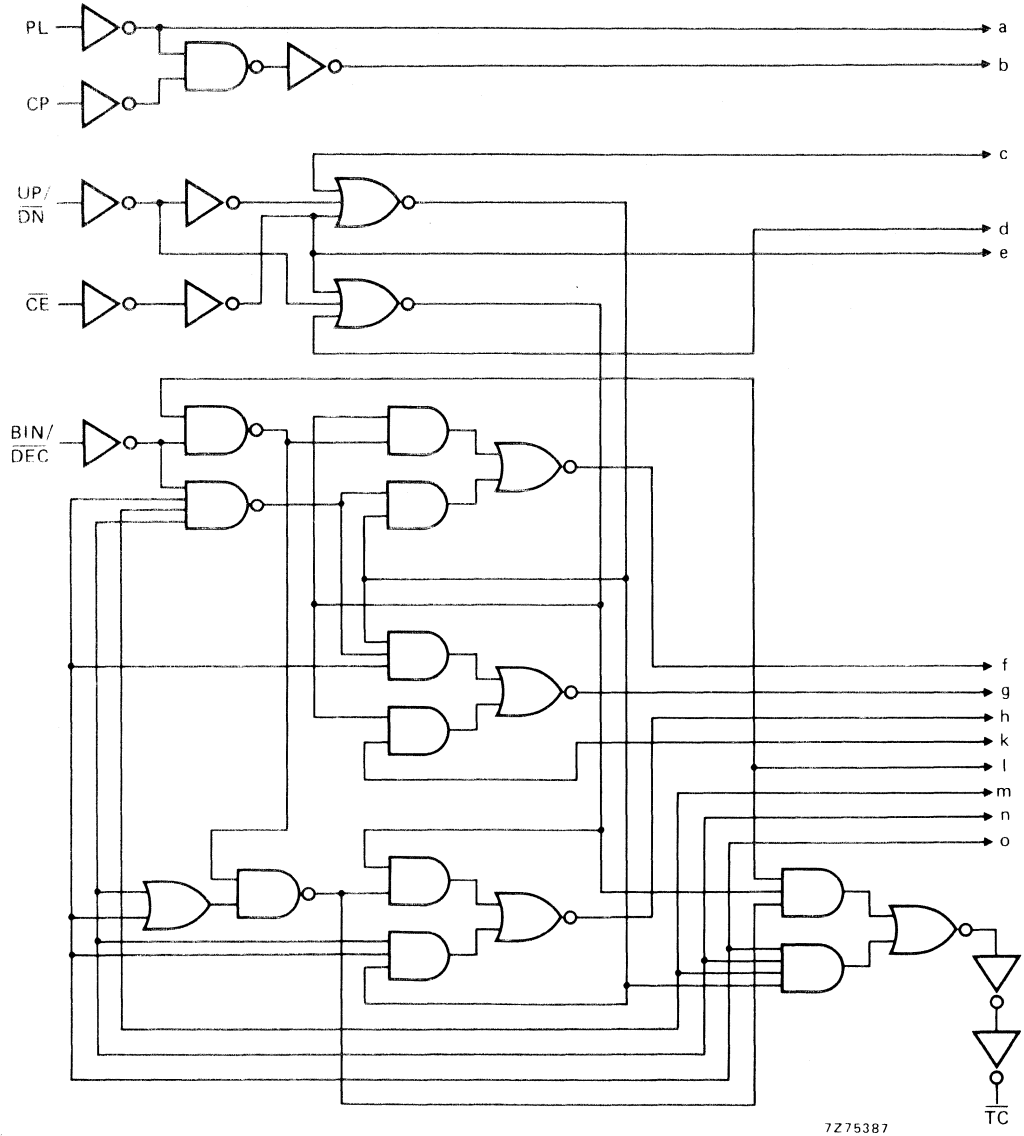


Fig. 3a Logic diagram (continued in Fig. 3b).

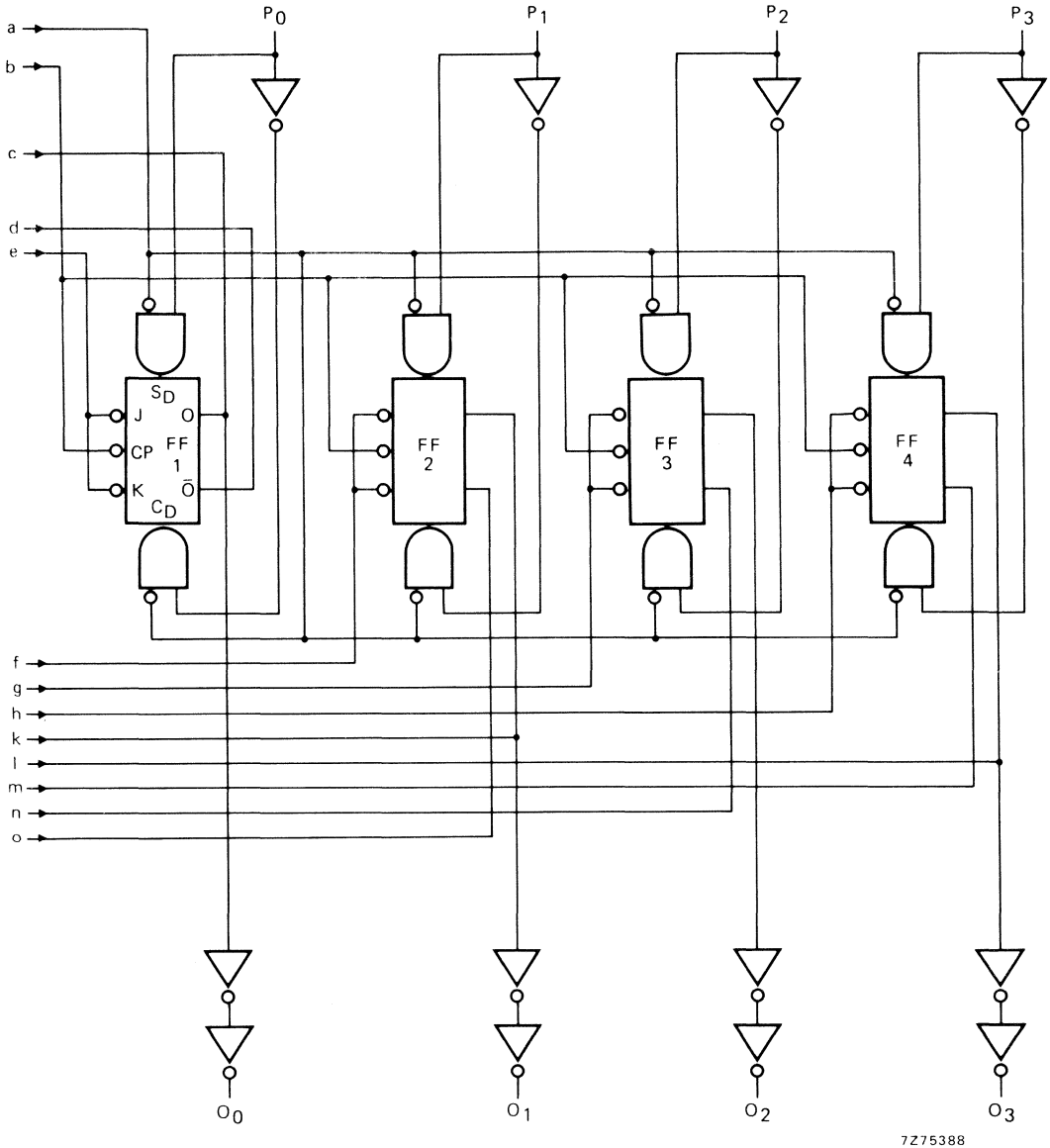


Fig. 3b Logic diagram (continued from Fig. 3a).

FUNCTION TABLE

PL	BIN/$\overline{DEC}$	UP/$\overline{DN}$	$\overline{CE}$	CP	mode
H	X	X	X	X	parallel load ($P_n \longrightarrow O_n$)
L	X	X	H	X	no change
L	L	L	L	∫	count-down, decade
L	L	H	L	∫	count-up, decade
L	H	L	L	∫	count-down, binary
L	H	H	L	∫	count-up, binary

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going clock pulse edge

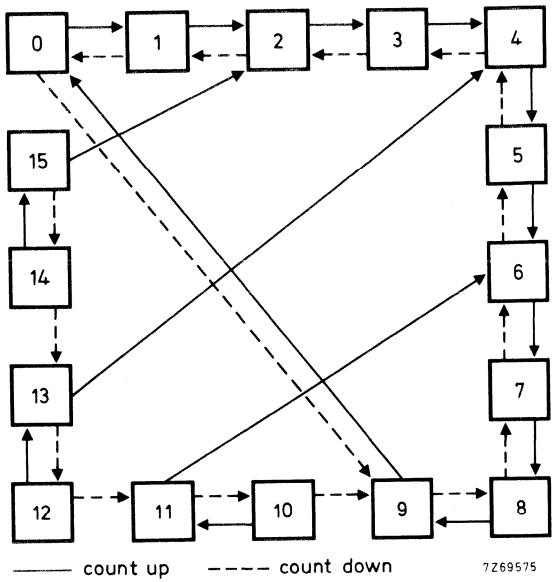


Fig. 4 State diagram; BIN/$\overline{DEC}$ = LOW.

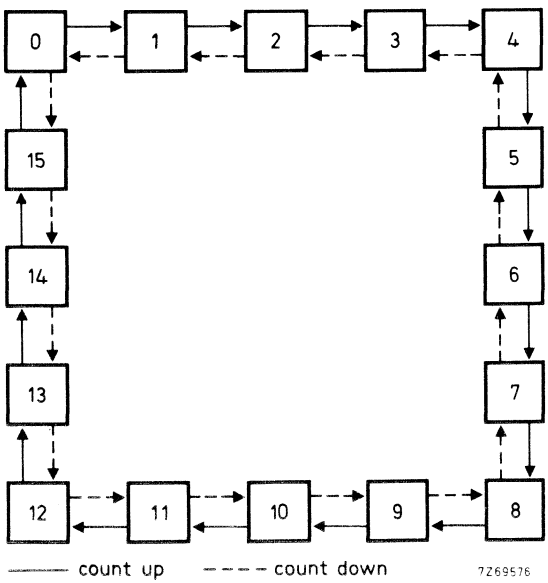


Fig. 5 State diagram; BIN/$\overline{DEC}$ = HIGH.

Logic equation for terminal count:

$$TC = \overline{\overline{CE}\,(BIN/\overline{DEC}\cdot UP/\overline{DN}\cdot O_0\cdot O_1\cdot O_2\cdot O_3 + BIN/\overline{DEC}\cdot \overline{UP/\overline{DN}}\cdot \overline{O}_0\cdot \overline{O}_1\cdot \overline{O}_2\cdot \overline{O}_3 + \overline{BIN/\overline{DEC}}\cdot UP/\overline{DN}\cdot O_0\cdot O_3 + \overline{BIN/\overline{DEC}}\cdot \overline{UP/\overline{DN}}\cdot \overline{O}_0\cdot \overline{O}_1\cdot \overline{O}_2\cdot \overline{O}_3)}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$11\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
	5			160	315	ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CP → $\overline{TC}$	5			280	560	ns	253 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		105	205	ns	94 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			195	385	ns	168 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	105	ns	47 ns + (0,16 ns/pF) C_L
PL → O_n	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			170	335	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
$\overline{CE}$ → $\overline{TC}$	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			170	335	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	135	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	110	55		ns	see also waveforms Figs 6 and 7
	10		35	20		ns	
	15		25	15		ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	160	80		ns	
	10		55	25		ns	
	15		35	15		ns	
Recovery time for PL	5	t_{RPL}	150	75		ns	
	10		50	25		ns	
	15		35	20		ns	
Set-up times BIN/$\overline{DEC}$ → CP	5	t_{su}	270	135		ns	
	10		90	45		ns	
	15		60	30		ns	
UP/$\overline{DN}$ → CP	5	t_{su}	300	150		ns	
	10		105	55		ns	
	15		75	35		ns	
$\overline{CE}$ → CP	5	t_{su}	120	60		ns	
	10		45	25		ns	
	15		35	20		ns	
P_n → PL	5	t_{su}	70	35		ns	
	10		20	10		ns	
	15		10	5		ns	
Hold times BIN/$\overline{DEC}$ → CP	5	t_{hold}	45	−90		ns	
	10		15	−30		ns	
	15		10	−20		ns	
UP/$\overline{DN}$ → CP	5	t_{hold}	15	−135		ns	
	10		0	−50		ns	
	15		−5	−35		ns	
$\overline{CE}$ → CP	5	t_{hold}	30	−30		ns	
	10		10	−10		ns	
	15		5	−10		ns	
P_n → PL	5	t_{hold}	15	−20		ns	
	10		0	−10		ns	
	15		0	−5		ns	
Maximum clock pulse frequency	5	f_{max}	4	8		MHz	
	10		12	25		MHz	
	15		18	35		MHz	

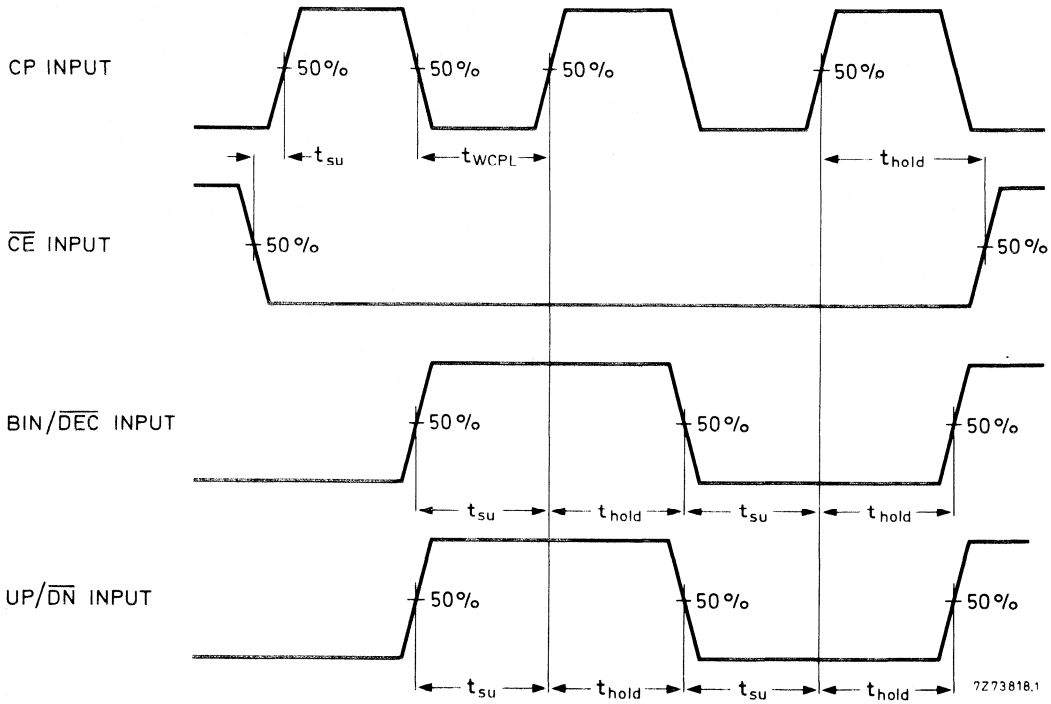


Fig. 6 Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP, BIN/$\overline{DEC}$ to CP and UP/$\overline{DN}$ to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

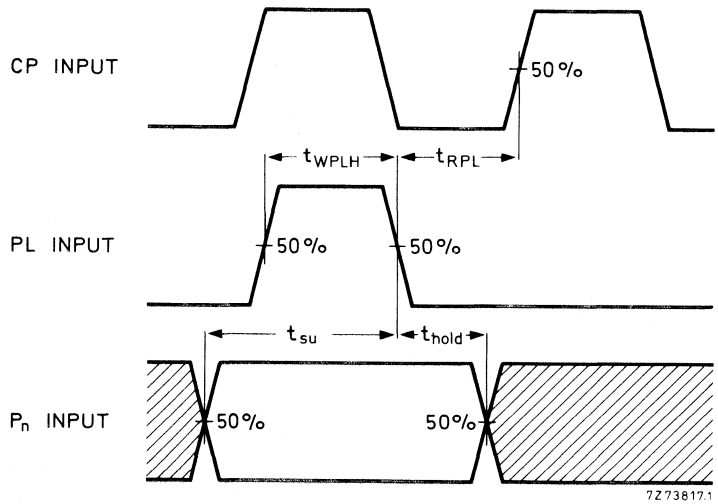


Fig. 7 Waveforms showing minimum pulse width for PL, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

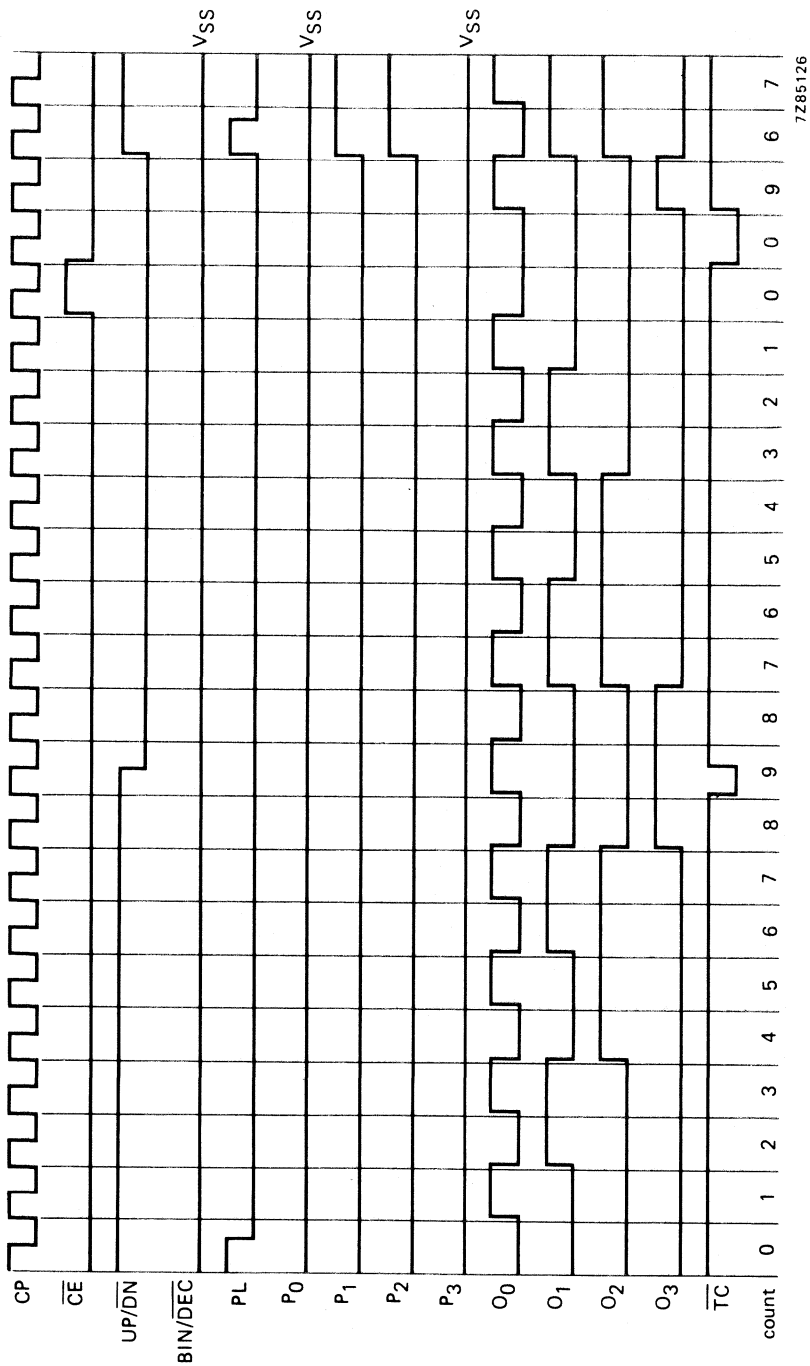


Fig. 8 Timing diagram; decade mode; P_0 = LOW; P_3 = LOW; BIN/$\overline{DEC}$ = LOW.

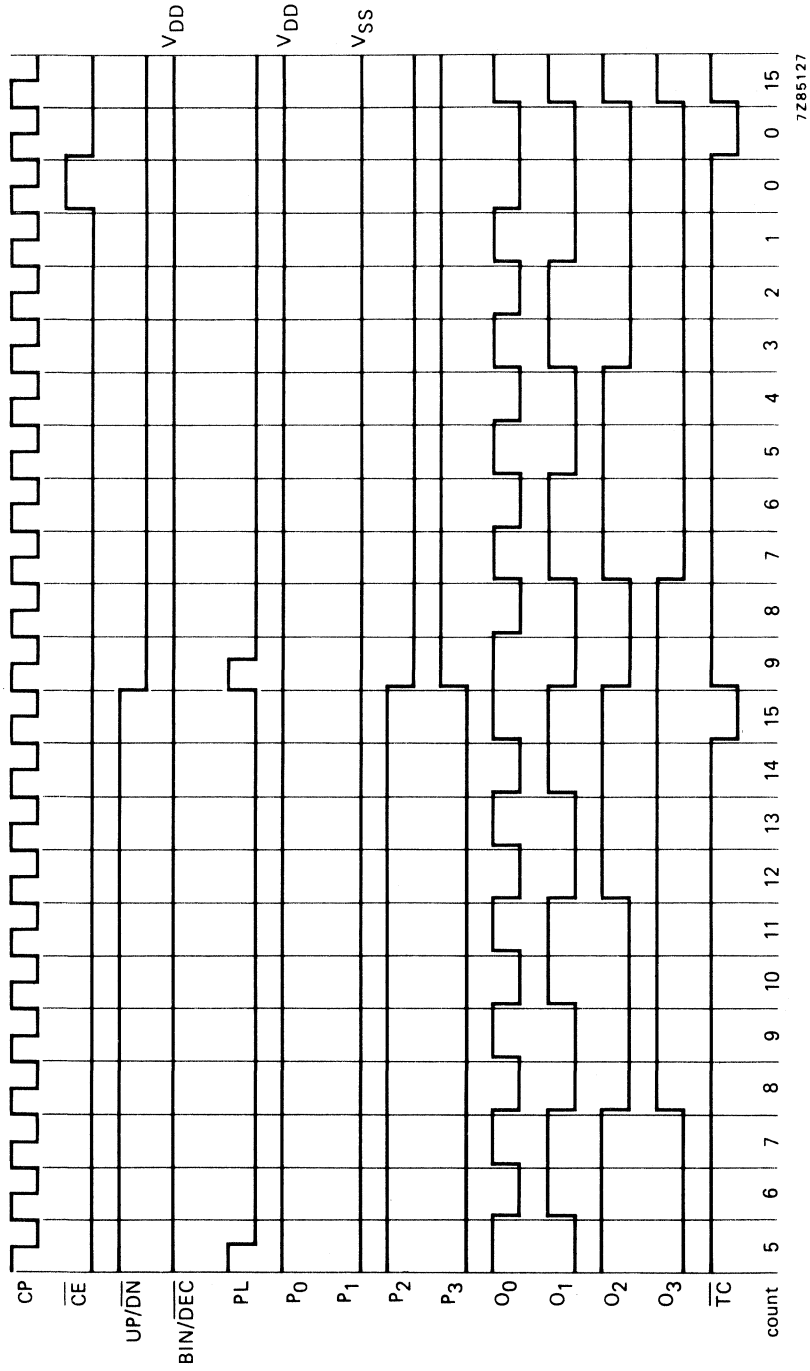


Fig. 9 Timing diagram; binary mode; P_0 = HIGH; P_1 = LOW; BIN/$\overline{DEC}$ = HIGH.

APPLICATION INFORMATION

Some examples of applications for the HEF4029B are:

- Programmable binary and decade counting/frequency synthesizers - BCD output.
- Analogue-to-digital and digital-to-analogue conversion.
- Up/down binary counting.
- Magnitude and sign generation.
- Up/down decade counting.
- Difference counting.

APPLICATION INFORMATION (continued)

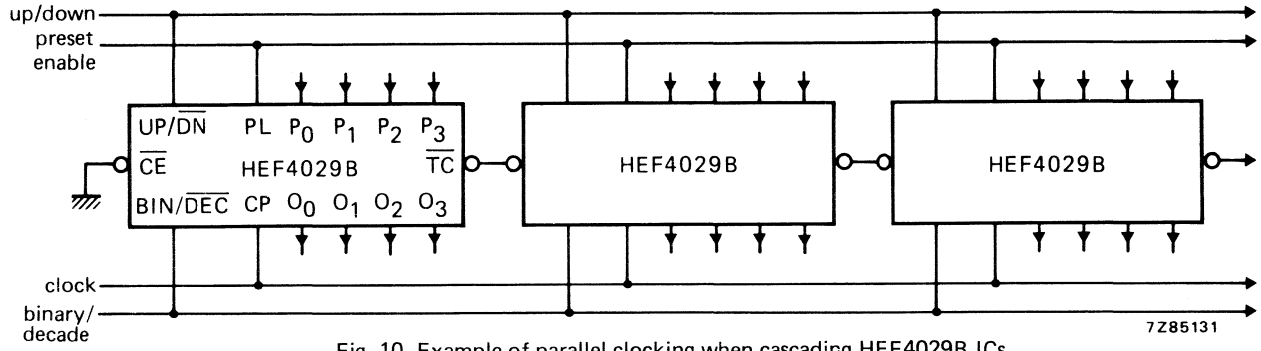


Fig. 10 Example of parallel clocking when cascading HEF4029B ICs.

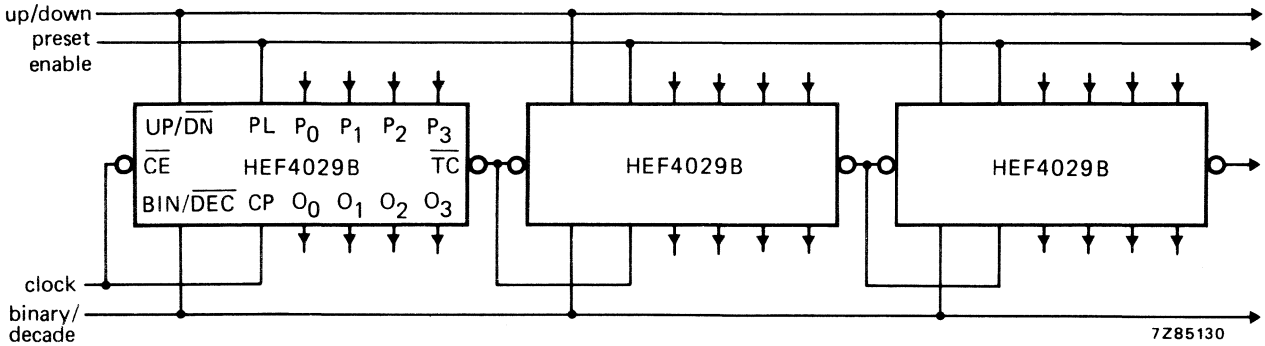


Fig. 11 Example of ripple clocking when cascading HEF4029B ICs. Ripple clocking mode: the up/down control can be changed at any count; the only restriction on changing the up/down control is that the clock input to the first counting stage must be HIGH.

Note

$\overline{TC}$ lines at all stages after the first may have a negative-going glitch pulse resulting from differential delays of different HEF4029B ICs. These negative-going glitches do not affect proper HEF4029B operation; however if the $\overline{TC}$ signals are used to trigger other edge-sensitive logic devices, such as flip-flops or counters, the $\overline{TC}$ signals should be gated with the clock signal using a 2-input OR gate such as HEF4071B.

QUADRUPLE EXCLUSIVE-OR GATE

The HEF4030B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

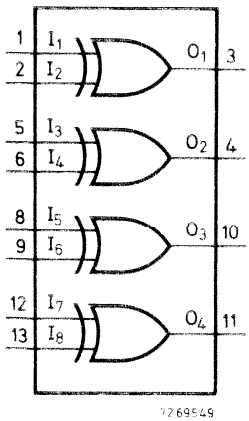


Fig. 1 Functional diagram.

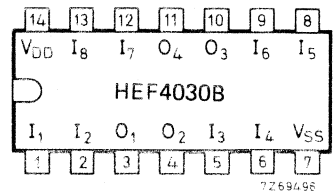


Fig. 2 Pinning diagram.

HEF4030BP : 14-lead DIL; plastic (SOT-27).
HEF4030BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4030BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

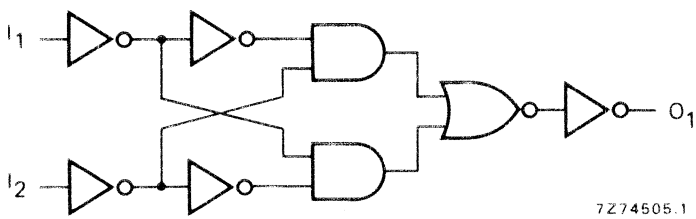


Fig. 3 Logic diagram (one gate).

TRUTH TABLE

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \longrightarrow O_n$	5		85	175	ns	57 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	75	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5		75	150	ns	47 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	65	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 100 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4 900 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	
	15	14 400 f_i + $\Sigma(f_oCL) \times V_{DD}^2$	

64-STAGE STATIC SHIFT REGISTER

The HEF4031B is an edge-triggered 64-stage static shift register with two serial data inputs (D_A, D_B), a data select input $\overline{A}/B$, a clock input (CP), a buffered clock output (CO), and buffered outputs from the 64th bit position (O_{63}, $\overline{O}_{63}$). The output O_{63} is capable of driving one TTL load.

Data from D_A or D_B, as determined by the state of $\overline{A}/B$, is shifted into the first shift register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D_A is selected by a LOW, and D_B by a HIGH on $\overline{A}/B$. Registers can be cascaded either by connecting all CP inputs together or by driving CP of the most right-hand register with the system clock and connecting CO to CP of the preceding register. When the second technique is used in the recirculating mode, a flip-flop must be used to store O_{63} of the most right-hand register until the most left-hand register is clocked.

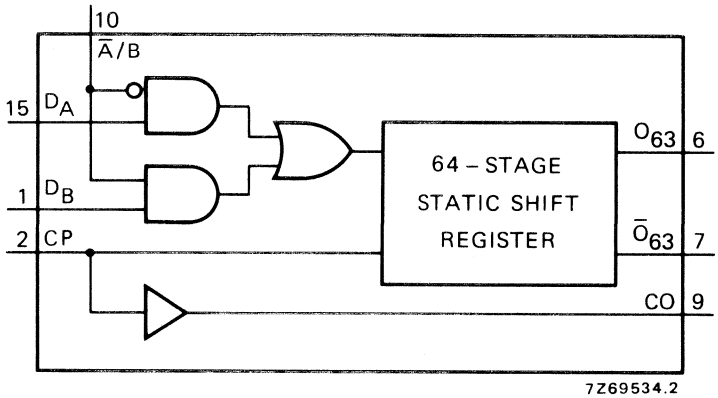


Fig. 1 Functional diagram.

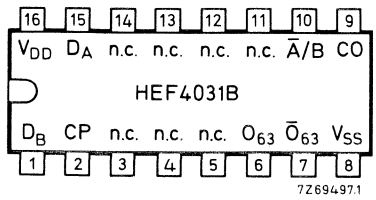


Fig. 2 Pinning diagram.

PINNING

D_A, D_B	data inputs
$\overline{A}/B$	data select input
CP	clock input (LOW to HIGH edge-triggered)
CO	buffered clock output
O_{63}	buffered output from the 64th stage
$\overline{O}_{63}$	complementary buffered output from the 64th stage

HEF4031BP : 16-lead DIL; plastic (SOT-38Z).
HEF4031BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4031BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications.

Products approved to CECC 90 104-028.

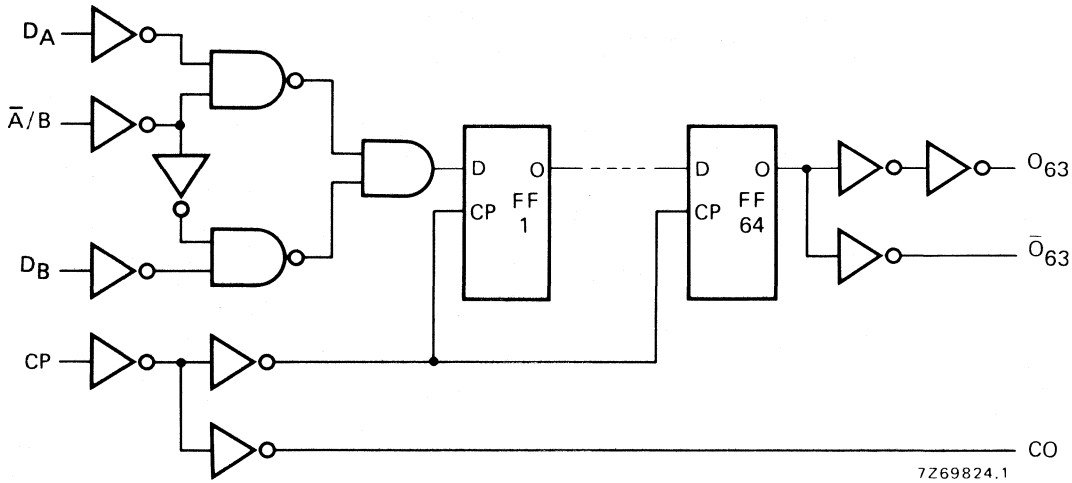


Fig. 3 Logic diagram.

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+ 25 min.	+ 25 max.	+ 85 min.	+ 85 max.	
Output (source)	5	4,6			1,0		0,85		0,65		mA
current	10	9,5		$-I_{OH}$	3,0		2,5		2,0		mA
HIGH; O_{63}	15	13,5			10,0		8,5		6,5		mA
HIGH; O_{63}	5	2,5		$-I_{OH}$	3,0		2,5		2,0		mA
Output (sink)	4,75		0,4		2,7		2,3		1,8		mA
current	10		0,5	I_{OL}	9,5		8,0		6,3		mA
LOW; O_{63}	15		1,5		24,0		20,0		16,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP → O_{63}	5			180	360 ns	167 ns + (0,26 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130 ns	57 ns + (0,16 ns/pF) C_L
	15			45	90 ns	40 ns + (0,11 ns/pF) C_L
	5			170	340 ns	148 ns + (0,45 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	56 ns + (0,19 ns/pF) C_L
	15			45	90 ns	39 ns + (0,13 ns/pF) C_L
CP → $\overline{O}_{63}$	5			190	380 ns	163 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
	5			190	380 ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
CP → CO	5			70	140 ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70 ns	24 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
	5			55	110 ns	28 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60 ns	19 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
Output transition	5			25	50 ns	5 ns + (0,40 ns/pF) C_L
times; O_{63}	10	t_{THL}		12	24 ns	3 ns + (0,18 ns/pF) C_L
HIGH to LOW	15			8	16 ns	2 ns + (0,13 ns/pF) C_L
	5			40	80 ns	8 ns + (0,65 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		20	40 ns	5 ns + (0,30 ns/pF) C_L
	15			13	26 ns	3 ns + (0,20 ns/pF) C_L
Output transition						
times; $\overline{O}_{63}$, CO	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Set-up times	5		25	0	ns	see also waveforms Fig. 4
D_A, D_B → CP	10	t_{su}	25	−5	ns	
	15		10	−10	ns	
	5		30	10	ns	
$\overline{A}/B$ → CP	10	t_{su}	15	0	ns	
	15		10	−5	ns	
Hold times	5		40	10	ns	
D_A, D_B → CP	10	t_{hold}	40	10	ns	
	15		40	10	ns	
	5		40	10	ns	
$\overline{A}/B$ → CP	10	t_{hold}	40	10	ns	
	15		40	10	ns	
Minimum clock pulse width; LOW	5		180	90	ns	
	10	t_{WCPL}	70	35	ns	
	15		50	25	ns	
Maximum clock pulse frequency	5		2,5	5	MHz	
	10	f_{max}	7	14	MHz	
	15		10	20	MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$4000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$19\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$54\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

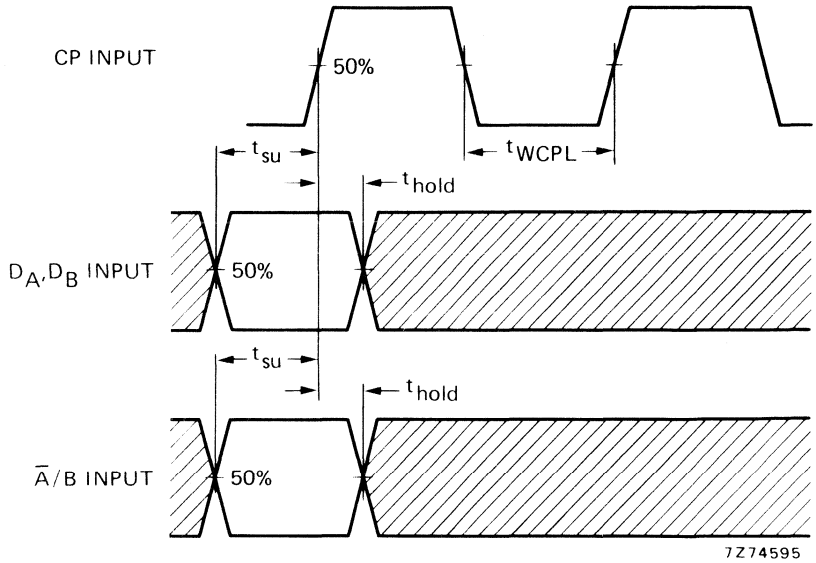


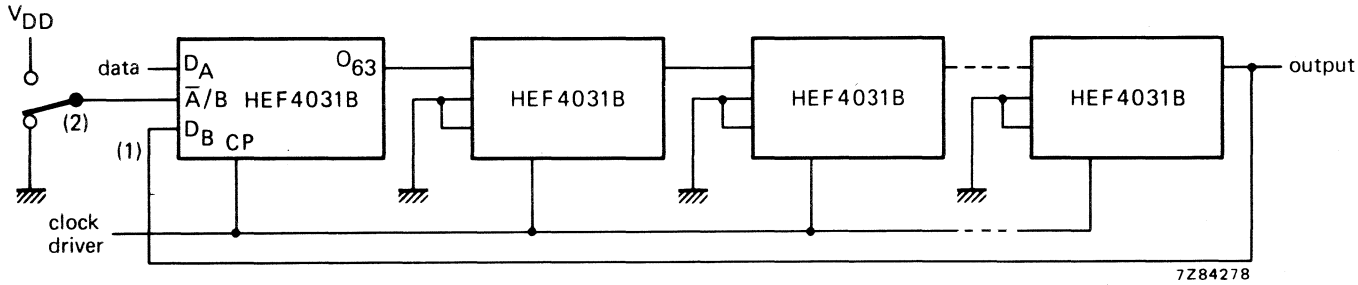
Fig. 4 Waveforms showing minimum clock pulse width, set-up and hold times for D_A, D_B to CP and $\overline{A}$/B to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

An example of an application for the HEF4031B is:

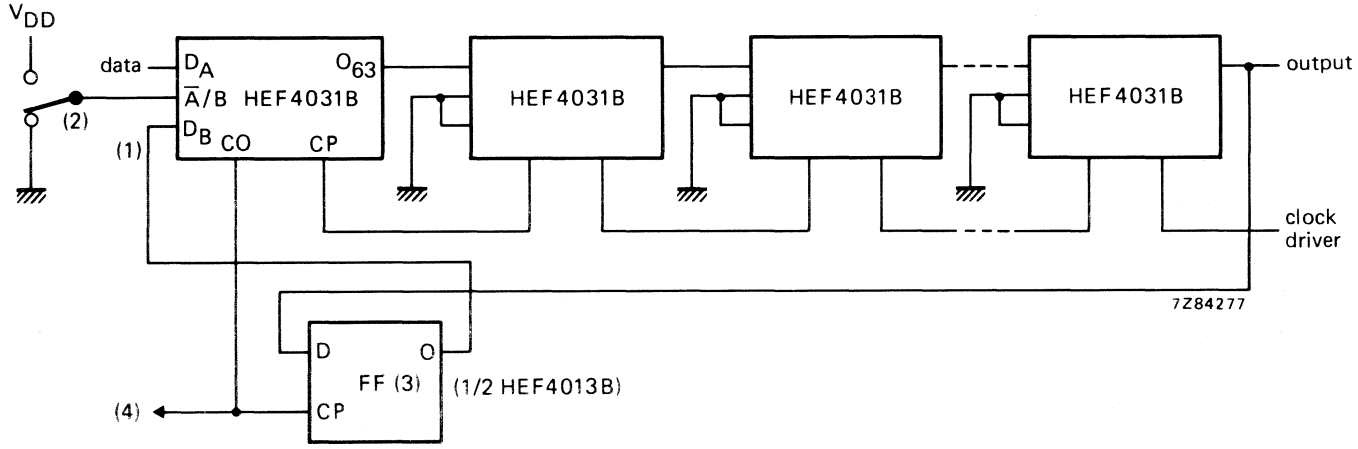
- Serial shift register.

APPLICATION INFORMATION



(1) Recirculating input.
(2) Mode control: V_{DD} = recirculation; ground (V_{SS}) = new data.

Fig. 5 Cascading using direct clocking for high speed operation (see clock rise and fall time requirements).



(1) Recirculating input.
(2) Mode control: V_{DD} = recirculation; ground (V_{SS}) = new data.
(3) For recirculation mode only, FF to delay data until first register delayed clocking has occurred.
(4) Delayed clock-to-clock; new data into first register.

Fig. 6 Cascading using delayed clocking for reduced clock drive requirements.

4-BIT UNIVERSAL SHIFT REGISTER

The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J, $\overline{K}$), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a true/complement input ($T/\overline{C}$) and an overriding asynchronous master reset input (MR).
Each register is of a D-type master-slave flip-flop.

Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP.

When PE is LOW, data is shifted into the first register position from J and $\overline{K}$ and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and $\overline{K}$. When J = HIGH and $\overline{K}$ = LOW the first stage is in the toggle mode. When J = LOW and $\overline{K}$ = HIGH the first stage is in the hold mode.

The outputs (O_0 to O_3) are either inverting or non-inverting, depending on $T/\overline{C}$ state. With $T/\overline{C}$ HIGH, O_0 to O_3 are non-inverting (active HIGH) and when $T/\overline{C}$ is LOW, O_0 to O_3 are inverting (active LOW).

A HIGH on MR resets all four bit positions (O_0 to O_3 = LOW if $T/\overline{C}$ = HIGH, O_0 to O_3 = HIGH if $T/\overline{C}$ = LOW) independent of all other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

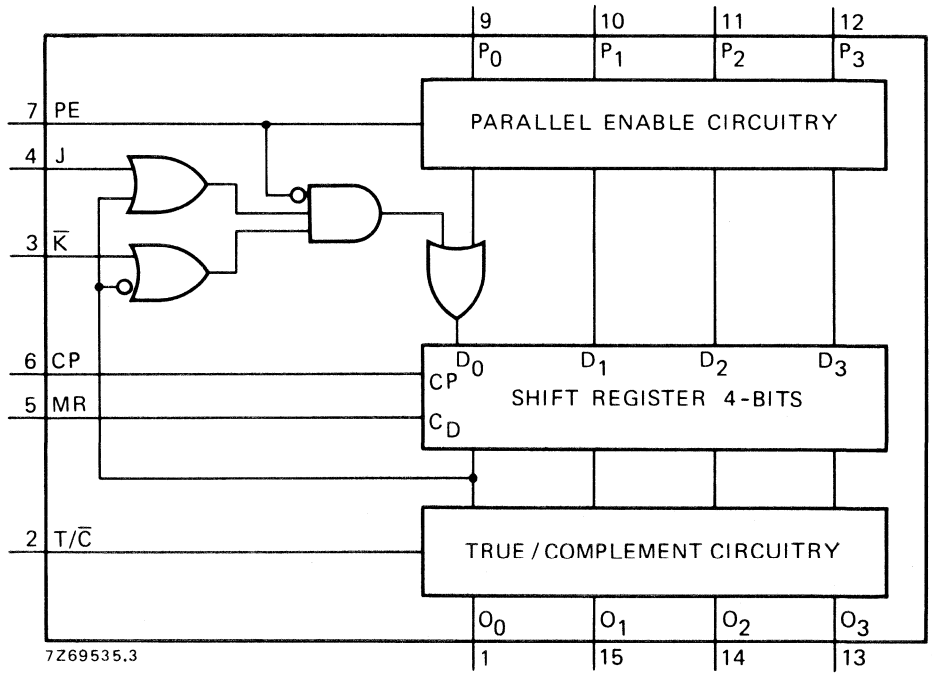


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

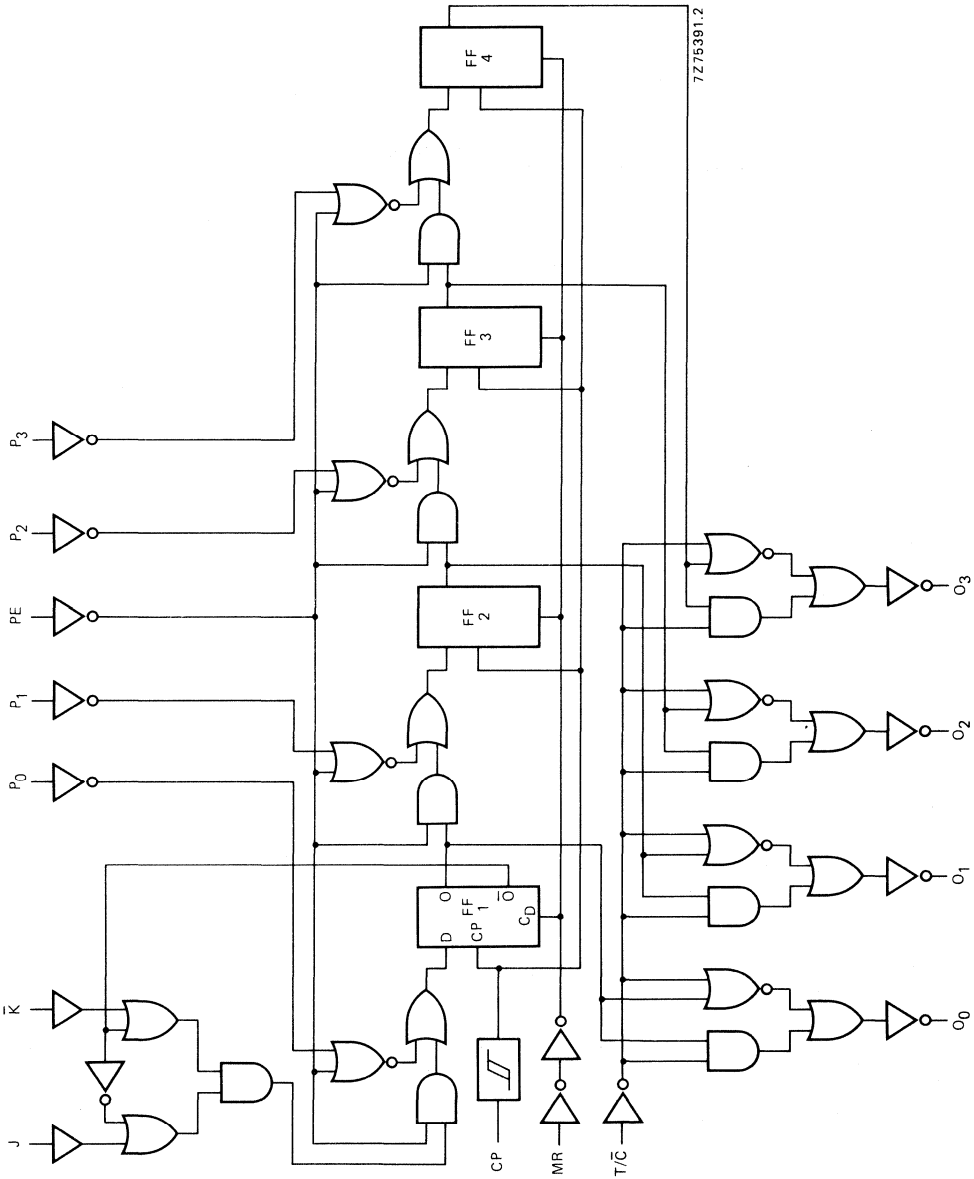


Fig. 2 Logic diagram.

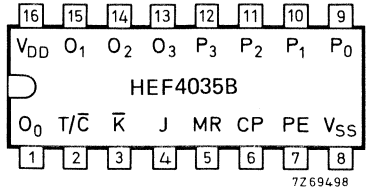


Fig. 3 Pinning diagram.

HEF4035BP : 16-lead DIL; plastic (SOT-38Z).
HEF4035BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4035BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

PE	parallel enable input	CP	clock input (LOW to HIGH edge-triggered)
P_0 to P_3	parallel data inputs		
J	first stage J-input (active HIGH)	$T/\overline{C}$	true/complement input
$\overline{K}$	first stage K-input (active LOW)	MR	master reset input
		O_0 to O_3	buffered parallel outputs

FUNCTION TABLES

Serial operation first stage

inputs				output	mode of operation
CP	J	$\overline{K}$	MR	O_{0+1}	
⎍	H	H	L	H	D flip-flop
⎍	L	L	L	L	D flip-flop
⎍	H	L	L	$\overline{O}_0$	toggle
⎍	L	H	L	O_0	no change
X	X	X	H	L	reset

$T/\overline{C}$ = HIGH; PE = LOW

Parallel operation

CP	inputs				outputs			
	P_0	P_1	P_2	P_3	O_0	O_1	O_2	O_3
⎍	H	H	H	H	H	H	H	H
⎍	L	L	L	L	L	L	L	L

$T/\overline{C}$ = HIGH; PE = HIGH; MR = LOW

⎍ = positive-going transition
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP → O_n	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
	5			150	300 ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
MR → O_n	5			115	230 ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			115	230 ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
$T/\overline{C}$ → O_n	5			105	210 ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
	5			85	170 ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90 ns	34 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; LOW	5	t_{WCPL}	80	40		ns	see also waveforms Figs 4 and 5
	10		40	20		ns	
	15		30	15		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	50	25		ns	
	10		30	15		ns	
	15		20	10		ns	
Recovery time for MR	5	t_{RMR}	50	20		ns	
	10		40	15		ns	
	15		25	10		ns	
Set-up times $P_n \longrightarrow CP$	5	t_{su}	40	5		ns	
	10		25	0		ns	
	15		15	0		ns	
$PE \longrightarrow CP$	5	t_{su}	50	25		ns	
	10		35	15		ns	
	15		30	10		ns	
$J, \overline{K} \longrightarrow CP$	5	t_{su}	55	40		ns	
	10		35	15		ns	
	15		25	10		ns	
Hold times $P_n \longrightarrow CP$	5	t_{hold}	25	10		ns	
	10		20	10		ns	
	15		20	10		ns	
$PE \longrightarrow CP$	5	t_{hold}	15	−5		ns	
	10		10	−5		ns	
	15		5	−5		ns	
$J, \overline{K} \longrightarrow CP$	5	t_{hold}	10	−5		ns	
	10		10	0		ns	
	15		10	0		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	25		MHz	
	15		15	30		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$20\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

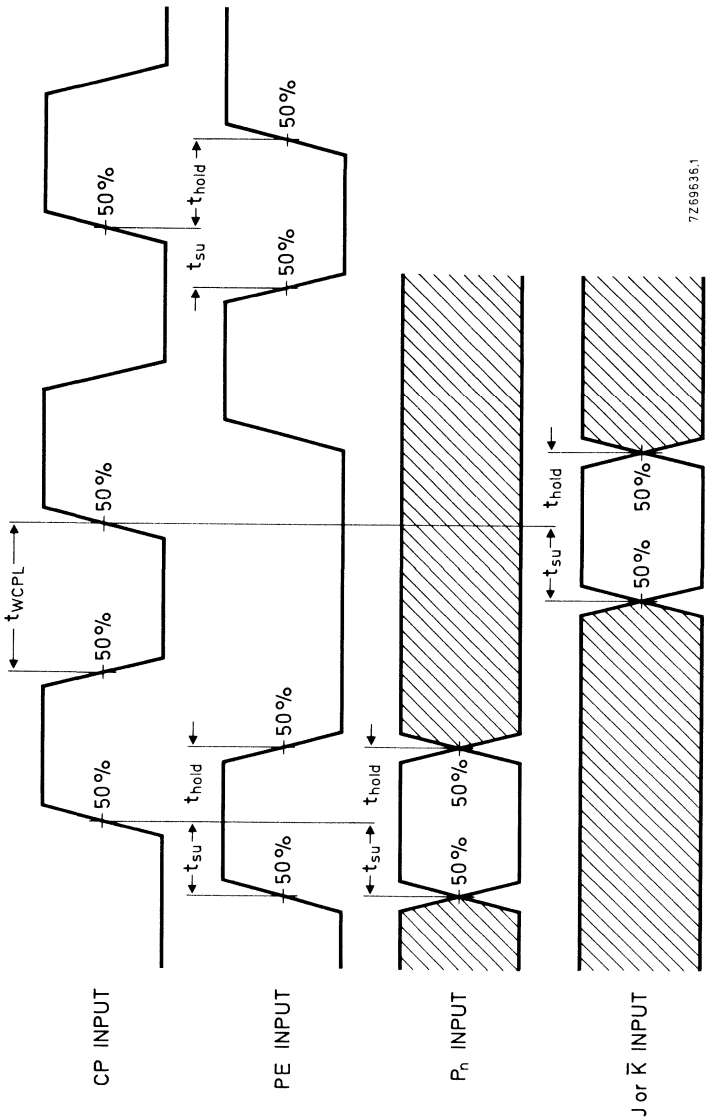


Fig. 4 Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.

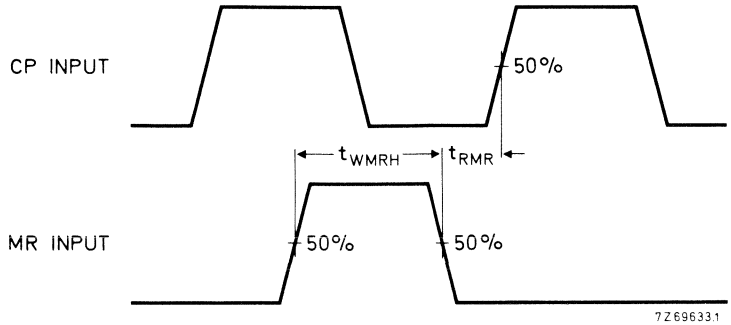


Fig. 5 Waveforms showing minimum MR pulse width and MR recovery time.

APPLICATION INFORMATION

Some examples of applications for the HEF4035B are:

- Counters, registers, arithmetic-unit registers, shift-left/shift-right registers.
- Serial-to-parallel/parallel-to-serial conversions.
- Sequence generation.
- Control circuits.
- Code conversion.

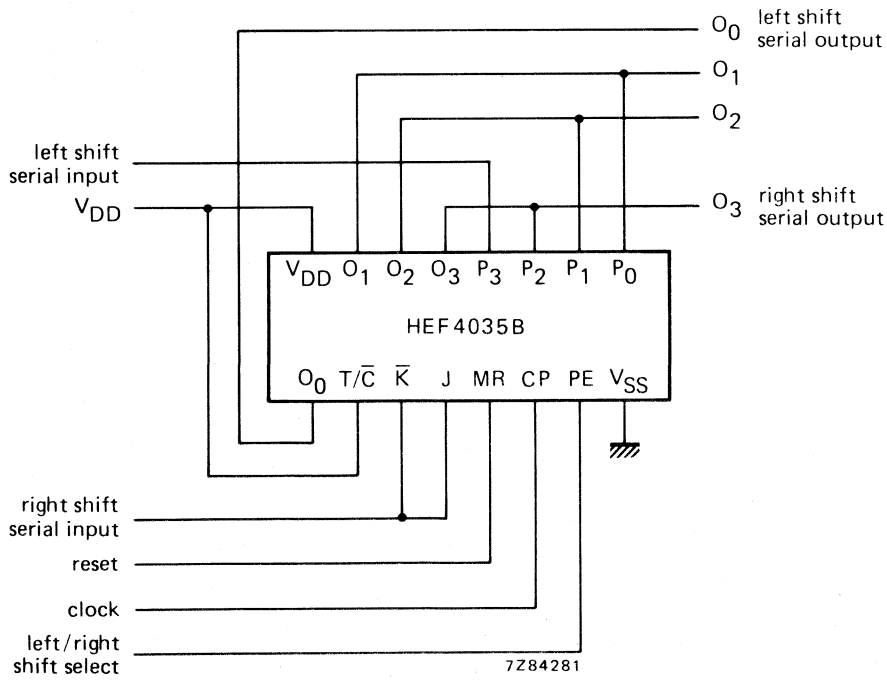


Fig. 6 Shift-left/shift-right register.

12-STAGE BINARY COUNTER

The HEF4040B is a 12-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0 to O_{11}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of $\overline{CP}$. Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

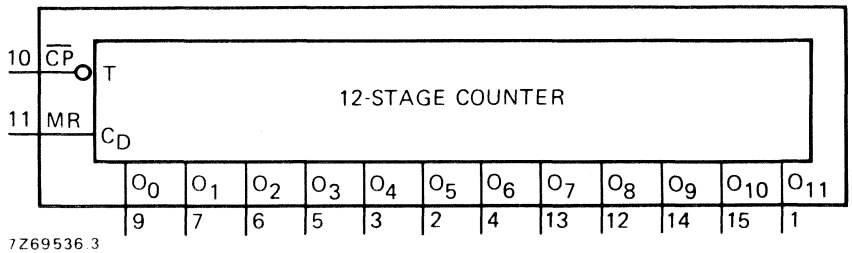


Fig. 1 Functional diagram.

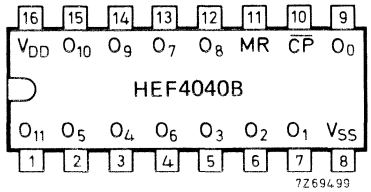


Fig. 2 Pinning diagram.

HEF4040BP : 16-lead DIL; plastic (SOT-38Z);
HEF4040BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4040BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{CP}$	clock input (HIGH to LOW edge-triggered)
MR	master reset input (active HIGH)
O_0 to O_{11}	parallel outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4040B are:

- Frequency dividing circuits
- Time delay circuits
- Control counters

FAMILY DATA, I_{DD} LIMITS category MSI — see Family Specifications

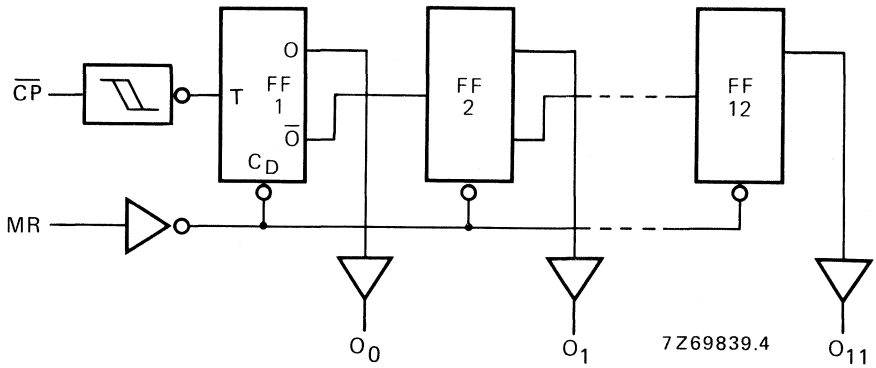


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{CP} \rightarrow O_0$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$O_n \rightarrow O_{n+1}$	5			35	70	ns	note (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		15	30	ns	note (0,23 ns/pF) C_L
	15			10	20	ns	note (0,16 ns/pF) C_L
	5			35	70	ns	note (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		15	30	ns	note (0,23 ns/pF) C_L
	15			10	20	ns	note (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

Note

For other loads than 50 pF at the n^{th} output, use the slope given.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; HIGH	5	t_{WCPH}	50	25		ns	see also waveforms Fig. 4
	10		30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	40	20		ns	
	10		30	15		ns	
	15		20	10		ns	
Recovery time for MR	5	t_{RMR}	40	20		ns	
	10		30	15		ns	
	15		20	10		ns	
Maximum clock pulse frequency	5	f_{max}	10	20		MHz	
	10		15	30		MHz	
	15		25	50		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$5\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

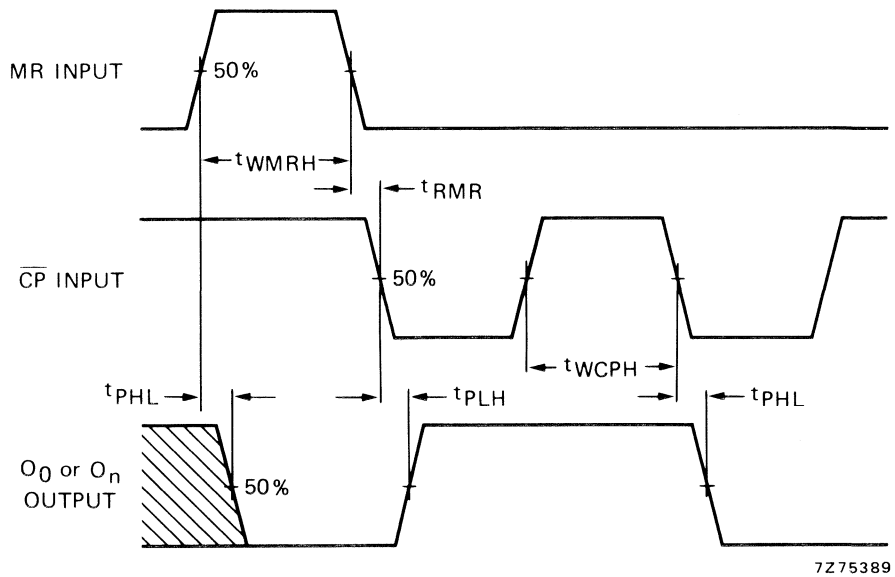


Fig. 4 Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths.

QUADRUPLE TRUE/COMPLEMENT BUFFER

The HEF4041B is a quadruple true/complement buffer which provides both an inverted active LOW output ($\overline{O}$) and a non-inverted active HIGH output (O) for each input (I).
The buffers exhibit high current output capability suitable for driving TTL or high capacitive loads.

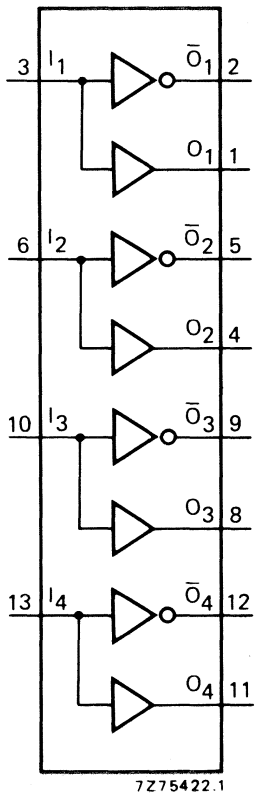


Fig. 1 Functional diagram.

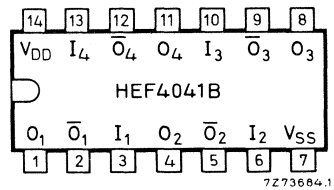


Fig. 2 Pinning diagram.

HEF4041BP : 14-lead DIL; plastic (SOT-27).
HEF4041BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4041BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

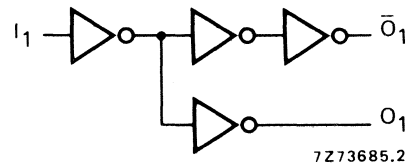


Fig. 3 Logic diagram (one buffer).

APPLICATION INFORMATION

Some examples of applications for the HEF4041B are:

- LOCMOS to DTL/TTL converter
- High current sink and source driver

FAMILY DATA

I_{DD} LIMITS category BUFFERS } see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 typ.	+85 min.	+85 max.	
Output (source) current	5	4,6			1,6		1,3	2,6	1,0		mA
HIGH	10	9,5		$-I_{OH}$	4,5		3,6	7,0	2,7		mA
	15	13,5			16,0		14,0	30,0	10,0		mA
HIGH	5	2,5		$-I_{OH}$	5,0		4,0	8,0	3,0		mA
Output (sink) current	4,75		0,4		2,0		1,7	4,0	1,35		mA
LOW	10		0,5	I_{OL}	7,5		6,0	12,0	4,5		mA
	15		1,5		23,0		20,0	35,0	15,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$I_n \rightarrow O_n$	5			30	65	ns	17 ns + (0,27 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		20	40	ns	14 ns + (0,11 ns/pF) C_L
	15			15	30	ns	12 ns + (0,08 ns/pF) C_L
	5			30	55	ns	17 ns + (0,27 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		15	30	ns	9 ns + (0,11 ns/pF) C_L
	15			10	20	ns	7 ns + (0,08 ns/pF) C_L
$I_n \rightarrow \overline{O}_n$	5			35	75	ns	22 ns + (0,27 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		20	40	ns	14 ns + (0,11 ns/pF) C_L
	15			15	30	ns	12 ns + (0,08 ns/pF) C_L
	5			35	75	ns	22 ns + (0,27 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		20	40	ns	14 ns + (0,11 ns/pF) C_L
	15			15	30	ns	12 ns + (0,08 ns/pF) C_L
Output transition times							
	5			25	50	ns	5 ns + (0,40 ns/pF) C_L
$O_n \rightarrow \overline{O}_n$	10	t_{THL}		12	25	ns	2 ns + (0,21 ns/pF) C_L
HIGH to LOW	15			8	20	ns	1 ns + (0,14 ns/pF) C_L
	5			25	45	ns	5 ns + (0,40 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		12	25	ns	2 ns + (0,21 ns/pF) C_L
	15			8	20	ns	1 ns + (0,14 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	3100 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	12 700 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	33 800 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

QUADRUPLE D-LATCH

The HEF4042B is a 4-bit latch with four data inputs (D_0 to D_3), four buffered latch outputs (O_0 to O_3), four buffered complementary latch outputs ($\overline{O}_0$ to $\overline{O}_3$) and two common enable inputs (E_0 and E_1). Information on D_0 to D_3 is transferred to O_0 to O_3 while both E_0 and E_1 are in the same state, either HIGH or LOW. O_0 to O_3 follow D_0 to D_3 as long as both E_0 and E_1 remain in the same state. When E_0 and E_1 are different, D_0 to D_3 do not affect O_0 to O_3 and the information in the latch is stored.

$\overline{O}_0$ to $\overline{O}_3$ are always the complement of O_0 to O_3. The exclusive-OR input structure allows the choice of either polarity for E_0 and E_1. With one enable input HIGH, the other enable input is active HIGH; with one enable input LOW, the other enable input is active LOW.

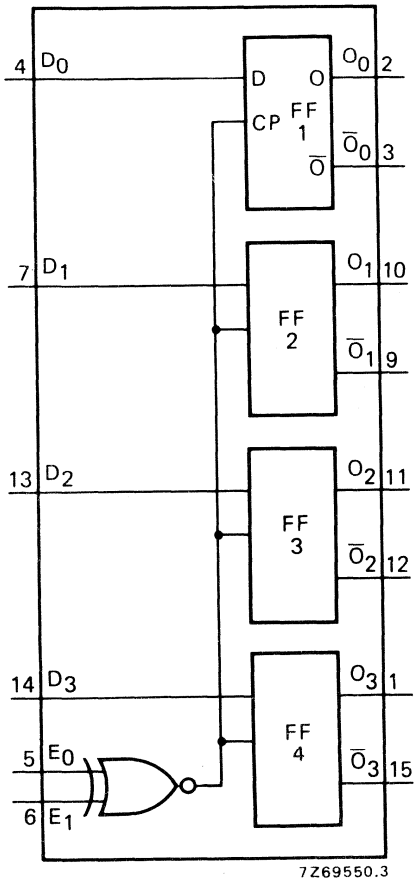


Fig. 1 Functional diagram.

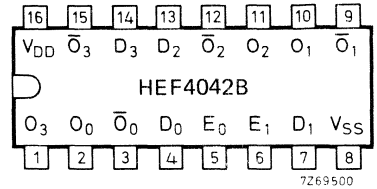


Fig. 2 Pinning diagram.

HEF4042BP : 16-lead DIL; plastic (SOT-38Z).
HEF4042BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4042BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_0 to D_3	data inputs
E_0 and E_1	enable inputs
O_0 to O_3	parallel latch outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary parallel latch outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4042B are:

- Buffer storage
- Holding register

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

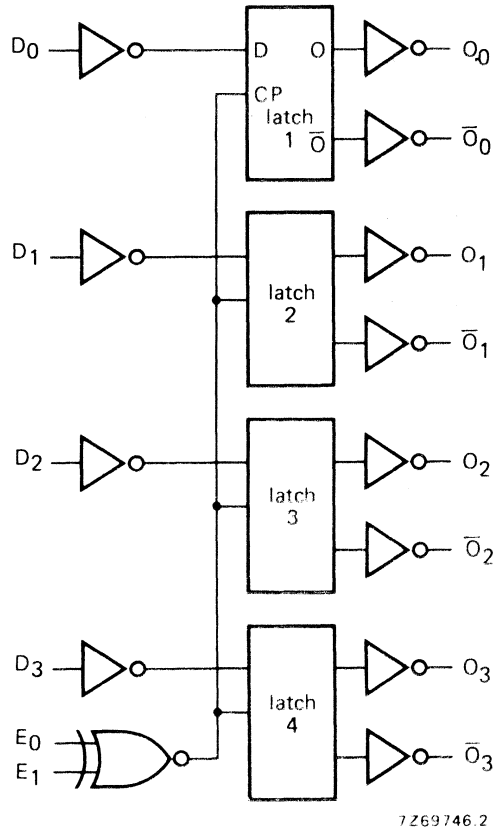


Fig. 3 Logic diagram.

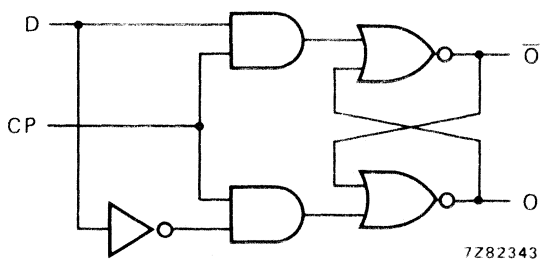


Fig. 4 Logic diagram (one latch).

FUNCTION TABLE

E_0	E_1	output O_n
L	L	D_n
L	H	latched
H	L	latched
H	H	D_n

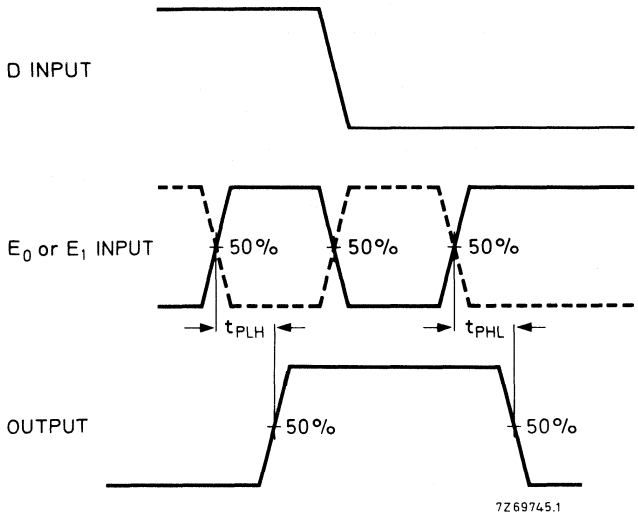
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
D ⟶ O, $\overline{O}$	5			95	190	ns	67 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	28 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
	5			85	175	ns	57 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	75	ns	28 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
E ⟶ O, $\overline{O}$	5			130	260	ns	102 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	105	ns	38 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			120	245	ns	92 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	105	ns	38 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		30	10		ns	
D ⟶ E	10	t_{su}	20	5		ns	
	15		20	5		ns	
Hold time	5		15	−5		ns	see also waveforms Figs 5 and 6
D ⟶ E	10	t_{hold}	15	0		ns	
	15		15	0		ns	
Minimum enable pulse width	5		90	45		ns	
	10	t_{WE}	40	20		ns	
	15		30	15		ns	

	V_{DD} V	typical formula for P (W)	where
Dynamic power dissipation per package (P)	5	$3800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$15\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$41\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



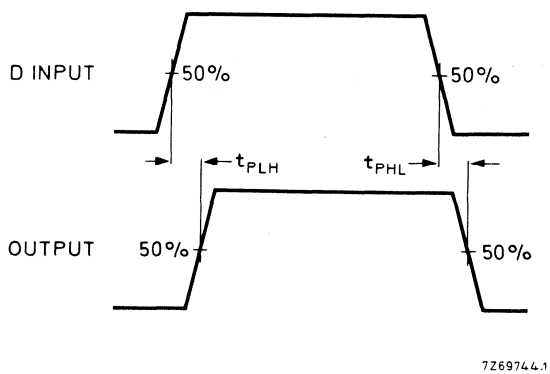


Fig. 5 Waveforms showing propagation delays for D to O, with latch enabled.

Note

Either E_0 or E_1 is held HIGH or LOW while the other enable input is pulsed as the function table shows.

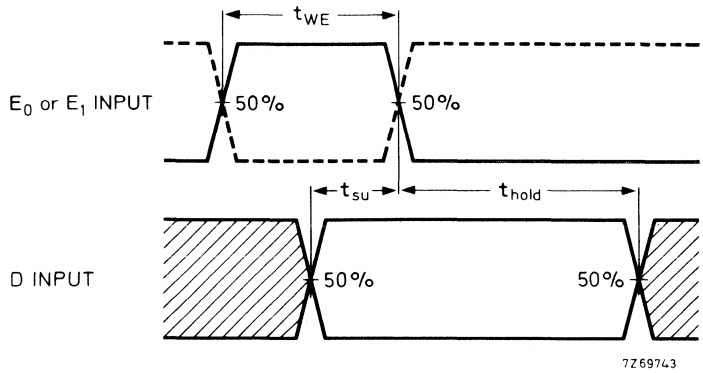


Fig. 6 Waveforms showing minimum enable pulse width, set-up time and hold time for E and D. Set-up and hold-times are shown as positive values but may be specified as negative values.

QUADRUPLE R/S LATCH WITH 3-STATE OUTPUTS

The HEF4043B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active HIGH set input (S_0 to S_3), an active HIGH reset input (R_0 to R_3) and an active HIGH 3-state output (O_0 to O_3).

When EO is HIGH, the state of the latch output (O_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common busing of the outputs.

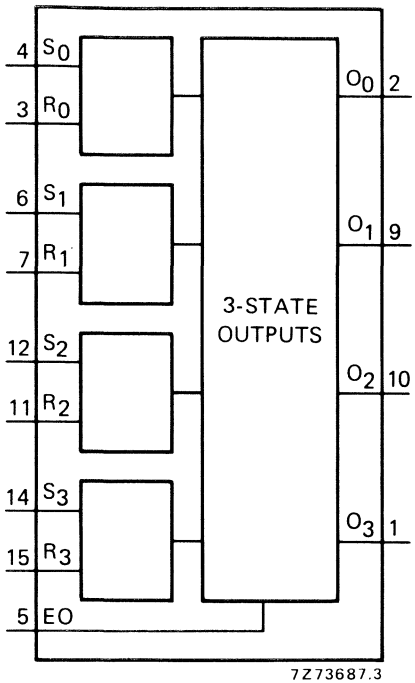


Fig. 1 Functional diagram.

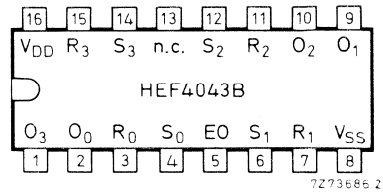


Fig. 2 Pinning diagram.

HEF4043BP : 16-lead DIL; plastic (SOT-38Z).
HEF4043BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4043BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

EO	common output enable input
S_0 to S_3	set inputs (active HIGH)
R_0 to R_3	reset inputs (active HIGH)
O_0 to O_3	3-state buffered latch outputs

FUNCTION TABLE

inputs			output
EO	S_n	R_n	O_n
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state immaterial
Z = high impedance state

FAMILY DATA } see Family Specifications

I_{DD} LIMITS category MSI }

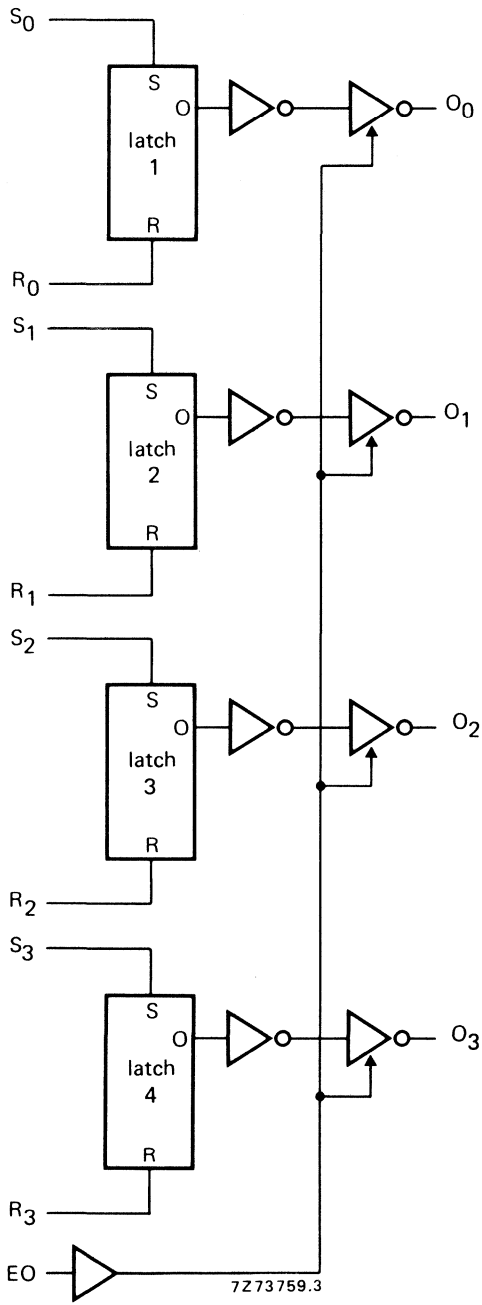


Fig. 3 Logic diagram.

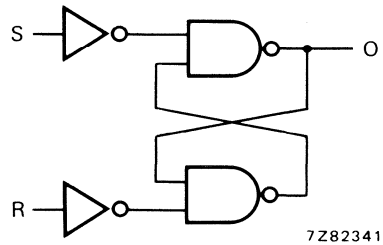


Fig. 4 Logic diagram (one latch).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$R_n \longrightarrow O_n$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$S_n \longrightarrow O_n$	5			65	135	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15			15	35	ns	7 ns + (0,16 ns/pG) C_L
Output transition	5			60	120	ns	10 ns + (1,0 ns /pF) C_L
times	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays							
Output disable times							
EO $\longrightarrow$ O_n	5			45	90	ns	
HIGH	10	t_{PHZ}		20	35	ns	
	15			10	25	ns	
	5			50	100	ns	
LOW	10	t_{PLZ}		20	40	ns	
	15			10	25	ns	
Output enable times							
EO $\longrightarrow$ O_n	5			25	50	ns	
HIGH	10	t_{PZH}		15	30	ns	
	15			10	25	ns	
	5			40	80	ns	
LOW	10	t_{PZL}		20	45	ns	
	15			15	35	ns	
Minimum S_n	5		30	15		ns	see also waveforms Fig. 5
pulse width; HIGH	10	t_{WSH}	20	10		ns	
	15		16	8		ns	
Minimum R_n	5		30	15		ns	
pulse width; HIGH	10	t_{WRH}	20	10		ns	
	15		16	8		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4400 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	11 400 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

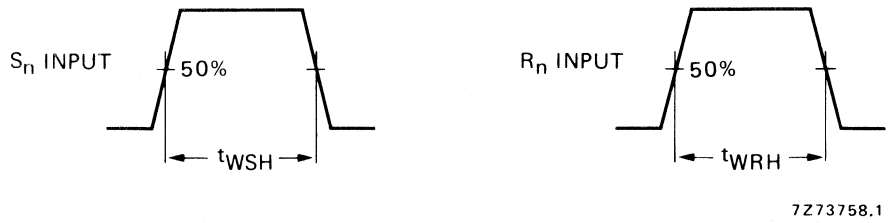


Fig. 5 Waveforms showing minimum S_n and R_n pulse widths.

APPLICATION INFORMATION

An example of application for the HEF4043B is:

- Four-bit storage with output enable

QUADRUPLE R/S LATCH WITH 3-STATE OUTPUTS

The HEF4044B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active LOW set input ($\overline{S}_0$ to $\overline{S}_3$), an active LOW reset input ($\overline{R}_0$ to $\overline{R}_3$) and an active HIGH 3-state output (O_0 to O_3).

When EO is HIGH, the state of the latch output (O_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common busing of the outputs.

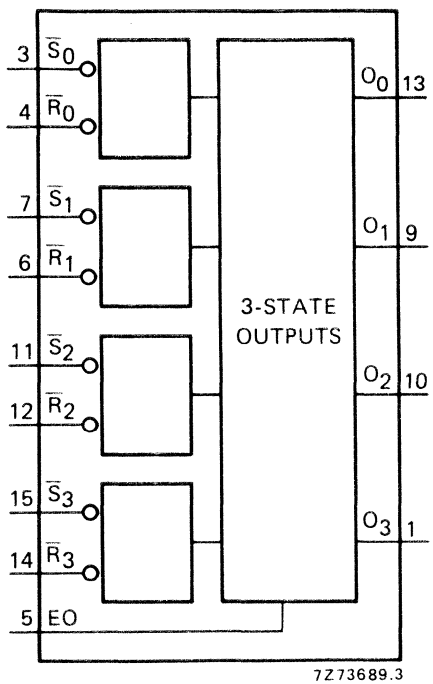


Fig. 1 Functional diagram.

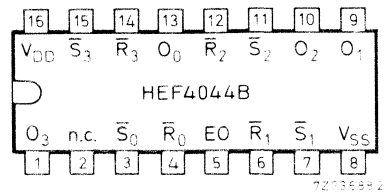


Fig. 2 Pinning diagram.

HEF4044BP : 16-lead DIL; plastic (SOT-38Z).
HEF4044BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4044BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

EO	common output enable input
$\overline{S}_0$ to $\overline{S}_3$	set inputs (active LOW)
$\overline{R}_0$ to $\overline{R}_3$	reset inputs (active LOW)
O_0 to O_3	3-state buffered latch outputs

FUNCTION TABLE

inputs			output
EO	$\overline{S}_n$	$\overline{R}_n$	O_n
L	X	X	Z
H	L	H	H
H	X	L	L
H	H	H	latched

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state immaterial
Z = high impedance OFF-state

FAMILY DATA
I_{DD} LIMITS category MSI
} see Family Specifications

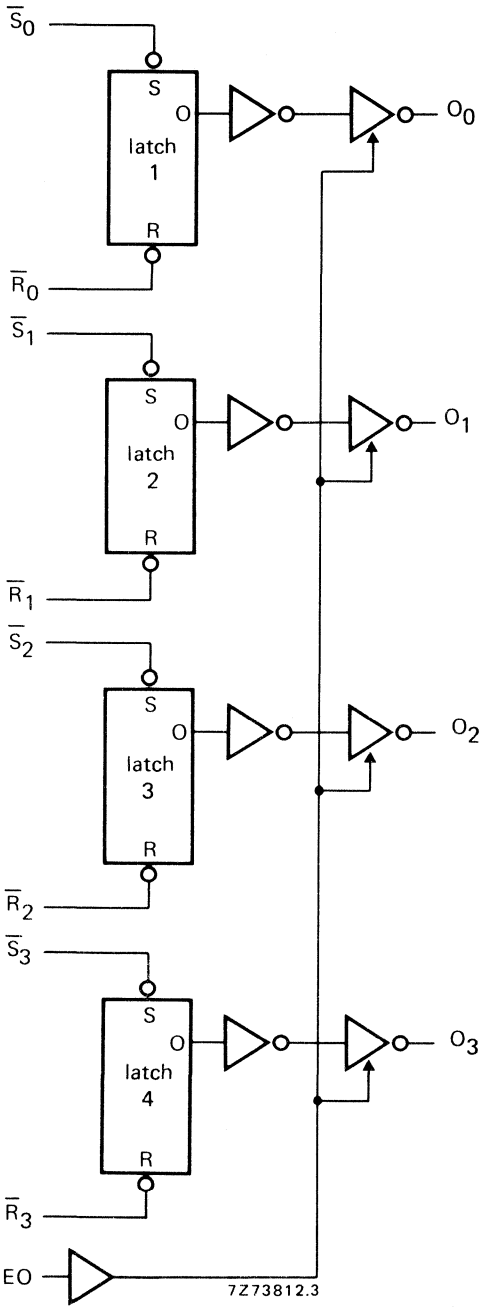


Fig. 3 Logic diagram.

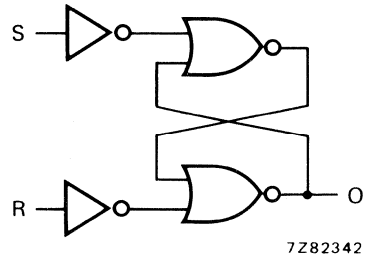


Fig. 4 Logic diagram (one latch).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{R}_n \rightarrow O_n$	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{S}_n \rightarrow O_n$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
times	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays							
Output disable times							
EO $\rightarrow O_n$	5			50	100	ns	
HIGH	10	t_{PHZ}		30	60	ns	
	15			25	50	ns	
	5			30	60	ns	
LOW	10	t_{PLZ}		25	45	ns	
	15			20	40	ns	
Output enable times							
EO $\rightarrow O_n$	5			50	100	ns	
HIGH	10	t_{PZH}		25	50	ns	
	15			20	40	ns	
	5			50	95	ns	
LOW	10	t_{PZL}		25	45	ns	
	15			20	35	ns	
Minimum $\overline{S}_n$	5		30	15		ns	see also waveforms Fig. 5
pulse width; LOW	10	t_{WSL}	20	10		ns	
	15		16	8		ns	
Minimum $\overline{R}_n$	5		30	15		ns	
pulse width; LOW	10	t_{WRL}	20	10		ns	
	15		16	8		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1300 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	12 900 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

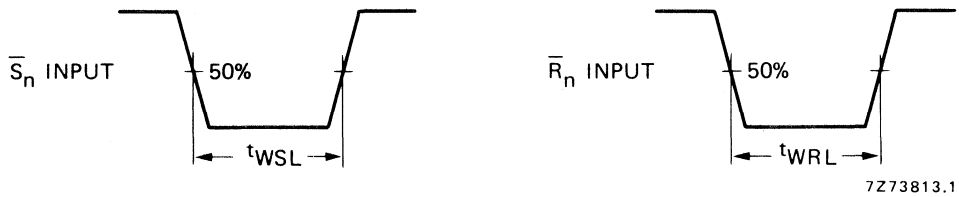


Fig. 5 Waveforms showing minimum $\overline{S}_n$ and $\overline{R}_n$ pulse widths.

APPLICATION INFORMATION

An example of application for the HEF4044B is:

- Four-bit storage with output enable

PHASE-LOCKED LOOP

The HEF4046B is a phase-locked loop circuit that consists of a linear voltage controlled oscillator (VCO) and two different phase comparators with a common signal input amplifier and a common comparator input. A 7 V regulator (zener) diode is provided for supply voltage regulation if necessary. For functional description see further on in this data.

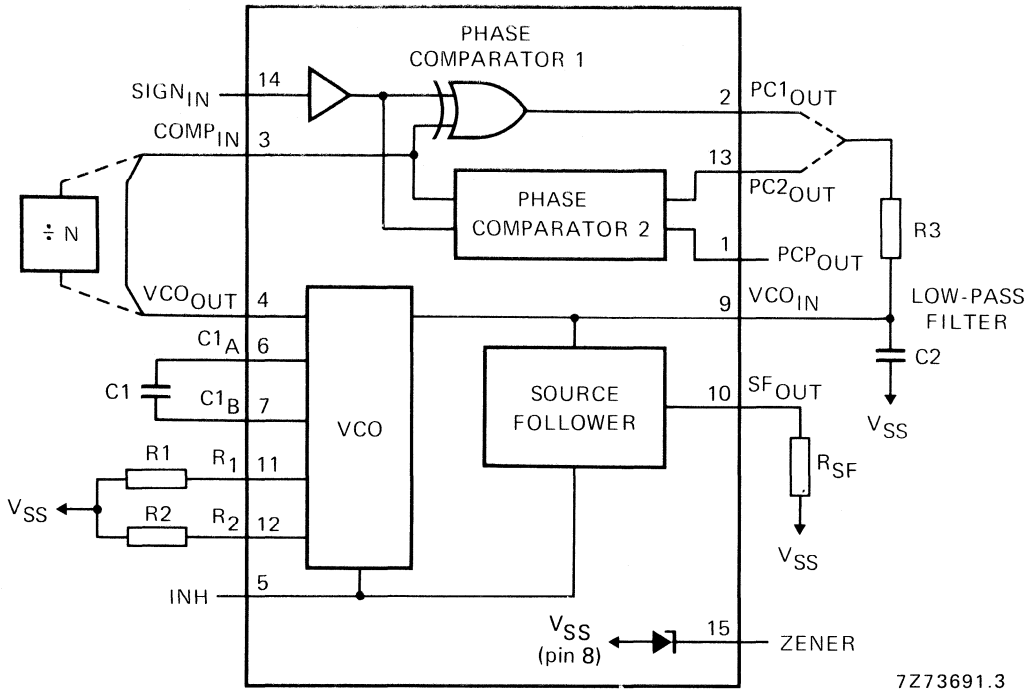


Fig. 1 Functional diagram.

HEF4046BP : 16-lead DIL; plastic (SOT-38Z).
HEF4046BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4046BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA: see Family Specifications

I_{DD} LIMITS category MSI: see further on in this data.

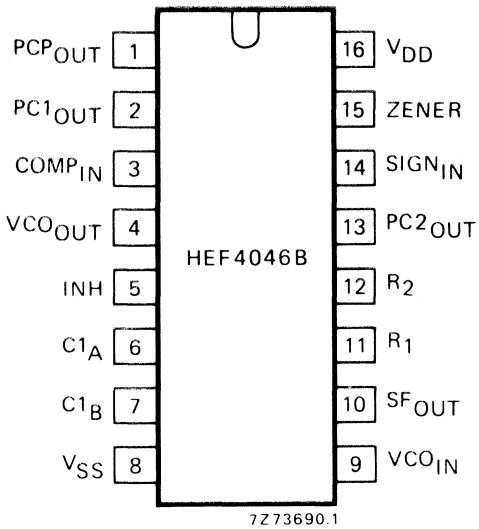


Fig. 2 Pinning diagram.

PINNING

1. Phase comparator pulse output
2. Phase comparator 1 output
3. Comparator input
4. VCO output
5. Inhibit input
6. Capacitor C1 connection A
7. Capacitor C1 connection B
8. V_{SS}
9. VCO input
10. Source-follower output
11. Resistor R1 connection
12. Resistor R2 connection
13. Phase comparator 2 output
14. Signal input
15. Zener diode input for regulated supply.

FUNCTIONAL DESCRIPTION

VCO part

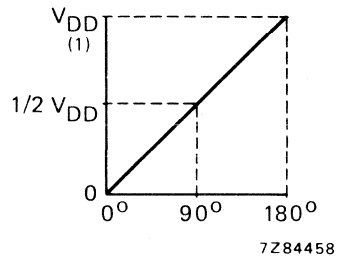
The VCO requires one external capacitor (C1) and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency off-set if required. The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at pin 10. If this pin (SF_{OUT}) is used, a load resistor (R_{SF}) should be connected from this pin to V_{SS}; if unused, this pin should be left open. The VCO output (pin 4) can either be connected directly to the comparator input (pin 3) or via a frequency divider. A LOW level at the inhibit input (pin 5) enables the VCO and the source follower, while a HIGH level turns off both to minimize stand-by power consumption.

Phase comparators

The phase-comparator signal input (pin 14) can be direct-coupled, provided the signal swing is between the standard HE4000B family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at the signal input in case of smaller swings. Phase comparator 1 is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50% duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to ½ V_{DD} when there is no signal or noise at the signal input. The average voltage to the VCO input is supplied by the low-pass filter connected to the output of phase comparator 1. This also causes the VCO to oscillate at the centre frequency (f_o). The frequency capture range (2 f_c) is defined as the frequency range of input signals on which the PLL will lock if it was inititally out of lock. The frequency lock range (2 f_L) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With phase comparator 1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. Phase comparator 1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal. A typical behaviour of this type of phase comparator is that it may lock onto input

frequencies that are close to harmonics of the VCO centre frequency. Another typical behaviour is, that the phase angle between the signal and comparator input varies between 0° and 180° and is 90° at the centre frequency. Figure 3 shows the typical phase-to-output response characteristic.



(1) Average output voltage.

Fig. 3 Signal-to-comparator inputs phase difference for comparator 1.

Figure 4 shows the typical waveforms for a PLL employing phase comparator 1 in locked condition of f_o.

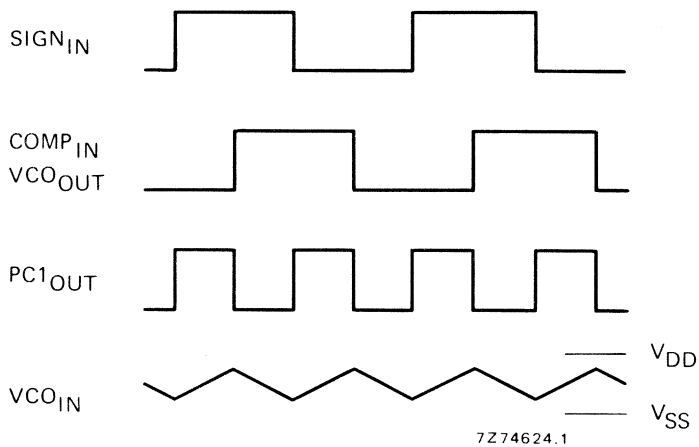


Fig. 4 Typical waveforms for phase-locked loop employing phase comparator 1 in locked condition of f_o.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers having a common output node. When the p-type or n-type drivers are ON, they pull the output up to V_{DD} or down to V_{SS} respectively. This type of phase comparator only acts on the positive-going edges of the signals at $SIGN_{IN}$ and $COMP_{IN}$. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain OFF and thus the phase comparator output becomes an open circuit and keeps the voltage at the capacitor of the low-pass filter constant.

Moreover, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level which can be used for indicating a locked condition. Thus, for phase comparator 2 no phase difference exists between the signal and comparator inputs over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both p and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator 2. Figure 5 shows typical waveforms for a PLL employing this type of phase comparator in locked condition.

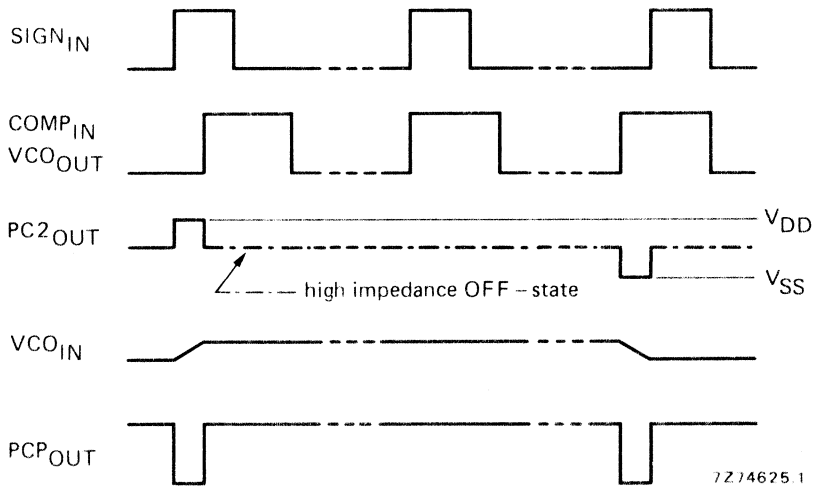
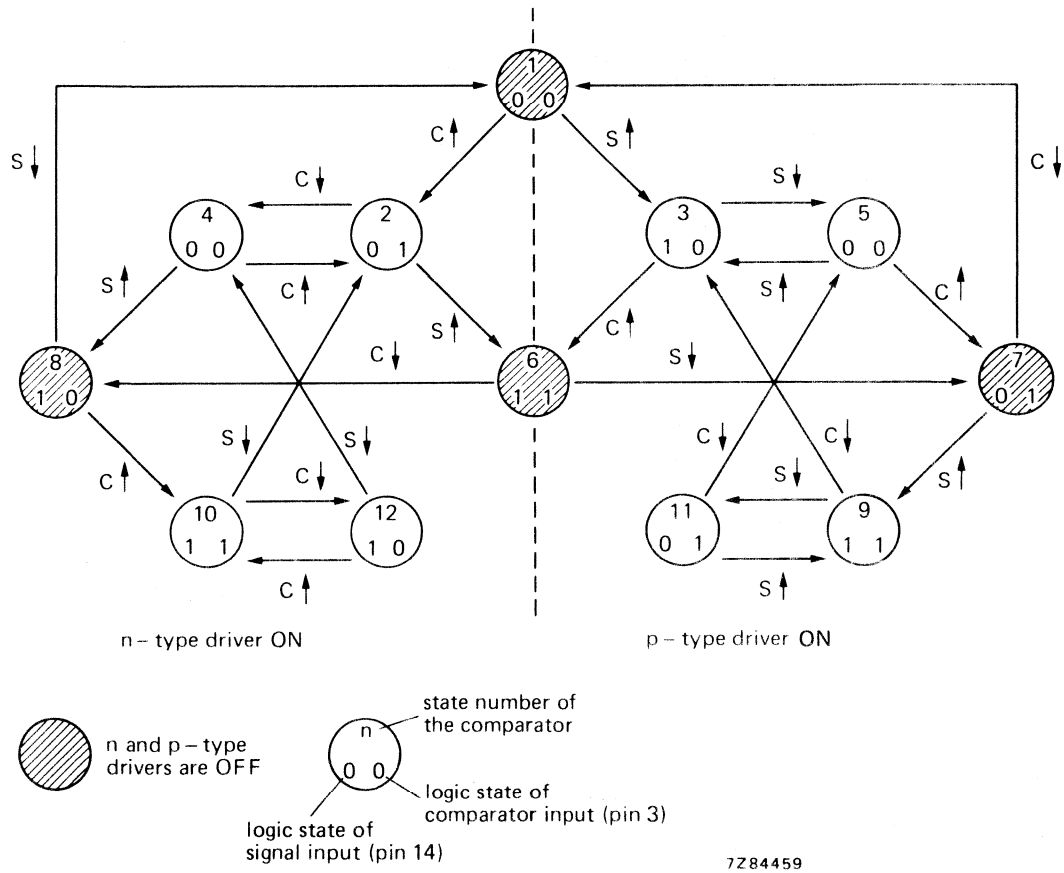


Fig. 5 Typical waveforms for phase-locked loop employing phase comparator 2 in locked condition.

Figure 6 shows the state diagram for phase comparator 2. Each circle represents a state of the comparator. The number at the top, inside each circle, represents the state of the comparator, while the logic state of the signal and comparator inputs are represented by a '0' for a logic LOW or a '1' for a logic HIGH, and they are shown in the left and right bottom of each circle.

The transitions from one to another result from either a logic change at the signal input (S) or the comparator input (C). A positive-going and a negative-going transition are shown by an arrow pointing up or down respectively.

The state diagram assumes, that only one transition on either the signal input or comparator input occurs at any instant. States 3, 5, 9 and 11 represent the condition at the output when the p-type driver is ON, while states 2, 4, 10 and 12 determine the condition when the n-type driver is ON. States 1, 6, 7 and 8 represent the condition when the output is in its high impedance OFF state; i.e. both p and n-type drivers are OFF, and the PCP_{OUT} output is HIGH. The condition at output PCP_{OUT} for all other states is LOW.



S ↑ : 0 to 1 transition at the signal input.
C ↓ : 1 to 0 transition at the comparator input.

Fig. 6 State diagram for comparator 2.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 typ.	−40 max.	+25 typ.	+25 max.	+85 typ.	+85 max.	
Supply current (note 1)	5	I_D	–	–	20	–	–	–	μA
	10		–	–	300	–	–	–	μA
	15		–	–	750	–	–	–	μA
Quiescent device current (note 2)	5	I_{DD}	–	20	–	20	–	150	μA
	10		–	40	–	40	–	300	μA
	15		–	80	–	80	–	600	μA

Notes

1. Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 open.
2. Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 at V_{DD}; input current pin 14 not included.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Phase comparators							
Operating supply voltage		V_{DD}	3		15	V	
Input resistance at $SIGN_{IN}$	5	R_{IN}		750		kΩ	at self-bias operating point
	10			220		kΩ	
	15			140		kΩ	
A.C. coupled input sensitivity at $SIGN_{IN}$	5	V_{IN}		150		mV	peak-to-peak values; R1 = 10 kΩ; R2 = ∞; C1 = 100 pF; independent of the lock range
	10			150		mV	
	15			200		mV	
D.C. coupled input sensitivity at $SIGN_{IN}$; $COMP_{IN}$ LOW level	5	V_{IL}			1,5	V	full temperature range
	10				3,0	V	
	15				4,0	V	
HIGH level	5	V_{IH}	3,5			V	
	10		7,0			V	
	15		11,0			V	
Input current at $SIGN_{IN}$	5	$+I_{IN}$		7		μA	$SIGN_{IN}$ at V_{DD}
	10			30		μA	
	15			70		μA	
	5	$-I_{IN}$		3		μA	$SIGN_{IN}$ at V_{SS}
	10			18		μA	
	15			45		μA	

A.C. CHARACTERISTICS $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
VCO							
Operating supply voltage		V_{DD}	3		15	V	as fixed oscillator only
			5		15	V	phase-locked loop operation
Power dissipation	5			150		μW	f_o = 10 kHz; R1 = 1 MΩ; R2 = ∞; VCO_{IN} at ½ V_{DD}; see also Figs 10 and 11
	10	P		2500		μW	
	15			9000		μW	
Maximum operating frequency	5		0,5	1,0		MHz	VCO_{IN} at V_{DD}; R1 = 10 kΩ; R2 = ∞; C1 = 50 pF
	10	f_{max}	1,0	2,0		MHz	
	15		1,3	2,7		MHz	
Temperature/ frequency stability	5			0,22–0,30		%/°C	no frequency offset (f_{min} = 0); see also note 1
	10			0,04–0,05		%/°C	
	15			0,01–0,05		%/°C	
	5			0–0,22		%/°C	with frequency offset ($f_{min} > 0$); see also note 1
	10			0–0,04		%/°C	
	15			0–0,01		%/°C	
Linearity	5			0,50		%	R1 > 10 kΩ; R1 > 400 kΩ; R1 = 1 MΩ; see Fig. 13 and Figs 14 15 and 16
	10			0,25		%	
	15			0,25		%	
Duty factor at VCO_{OUT}	5			50		%	
	10	δ		50		%	
	15			50		%	
Input resistance at VCO_{IN}	5			10^6		MΩ	
	10	R_{IN}		10^6		MΩ	
	15			10^6		MΩ	
Source follower							
Offset voltage VCO_{IN} minus SF_{OUT}	5			1,7		V	R_{SF} = 10 kΩ; VCO_{IN} at ½ V_{DD}
	10			2,0		V	
	15			2,1		V	
	5			1,5		V	R_{SF} = 50 kΩ; VCO_{IN} at ½ V_{DD}
	10			1,7		V	
	15			1,8		V	
Linearity	5			0,3		%	R_{SF} > 50 kΩ; see Fig. 13
	10			1,0		%	
	15			1,3		%	
Zener diode							
Zener voltage		V_Z		7,3		V	I_Z = 50 μA
Dynamic resistance		R_Z		25		Ω	I_Z = 1 mA

Notes
1. Over the recommended component range.

DESIGN INFORMATION

characteristic	using phase comparator 1	using phase comparator 2
No signal on $SIGN_{IN}$	VCO in PLL system adjusts to centre frequency (f_o)	VCO in PLL system adjusts to min. frequency (f_{min})
Phase angle between $SIGN_{IN}$ and $COMP_{IN}$	90° at centre frequency (f_o), approaching 0° and 180° at ends of lock range (2 f_L)	always 0° in lock (positive-going edges)
Locks on harmonics of centre frequency	yes	no
Signal input noise rejection	high	low
Lock frequency range (2 f_L)	the frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2 f_L = full VCO frequency range = $f_{max} - f_{min}$	
Capture frequency range (2 f_C)	the frequency range of the input signal on which the loop will lock if it was initially out of lock	
	depends on low-pass filter characteristics; $f_C < f_L$	$f_C = f_L$
Centre frequency (f_o)	the frequency of the VCO when VCO_{IN} at $\frac{1}{2}V_{DD}$	

VCO component selection

Recommended range for R1 and R2: 10 kΩ to 1 MΩ; for C1: 50 pF to any practical value.

1. VCO without frequency offset (R2 = ∞).
   a. Given f_o: use f_o with Fig. 7 to determine R1 and C1.
   b. Given f_{max}: calculate f_o from $f_o = \frac{1}{2} f_{max}$; use f_o with Fig. 7 to determine R1 and C1.
2. VCO with frequency offset.
   a. Given f_o and f_L: calculate f_{min} from the equation $f_{min} = f_o - f_L$; use f_{min} with Fig. 8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$; use $\frac{f_{max}}{f_{min}}$ with Fig. 9 to determine the ratio R2/R1 to obtain R1.
   b. Given f_{min} and f_{max}: use f_{min} with Fig. 8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$; use $\frac{f_{max}}{f_{min}}$ with Fig. 9 to determine R2/R1 to obtain R1.

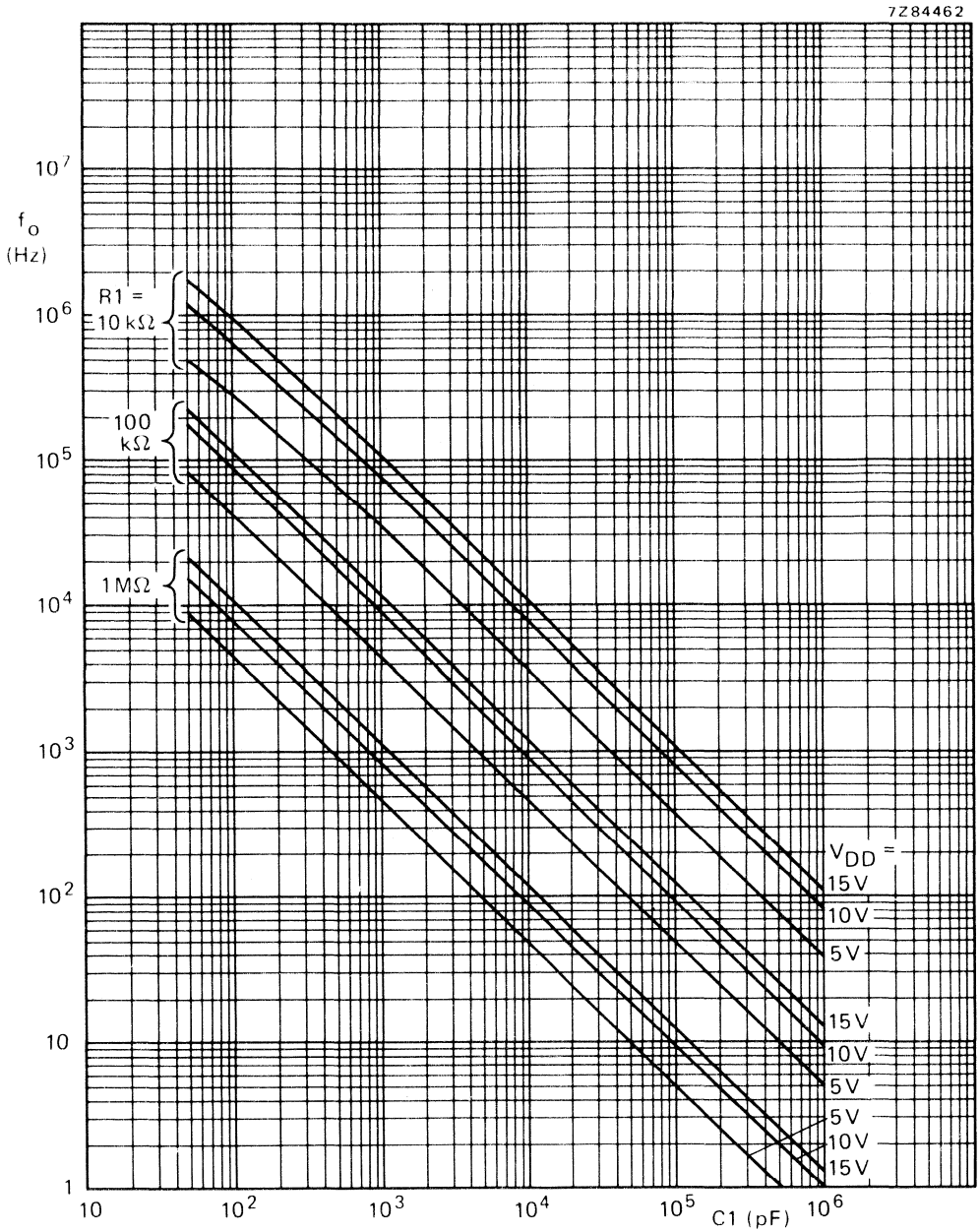


Fig. 7 Typical centre frequency as a function of capacitor C1; T_{amb} = 25 °C; VCO_{IN} at ½ V_{DD}; INH at V_{SS}; R2 = ∞.

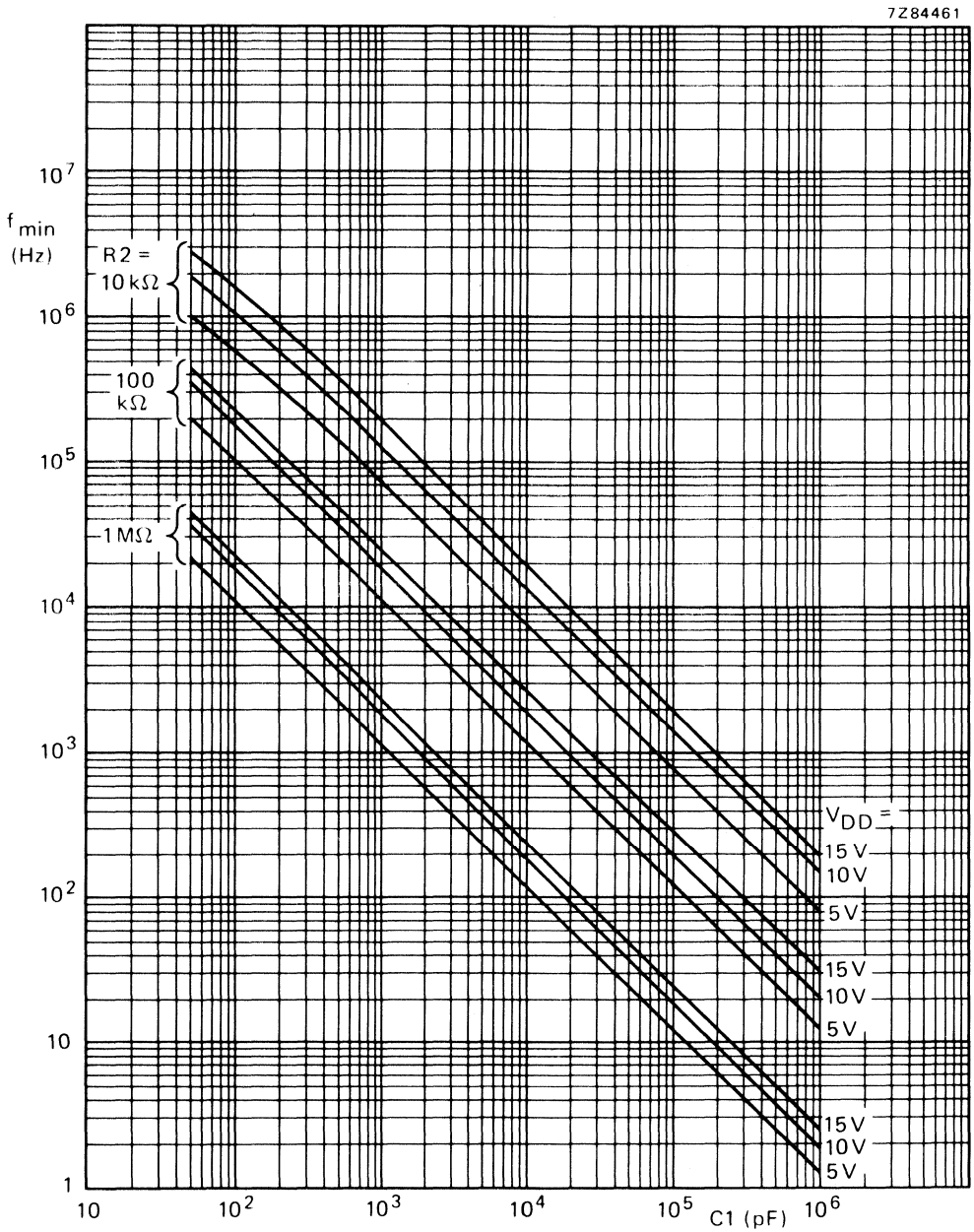


Fig. 8 Typical frequency offset as a function of capacitor C1; T_{amb} = 25 °C; VCO_{IN} at V_{SS}; INH at V_{SS}; R1 = ∞.

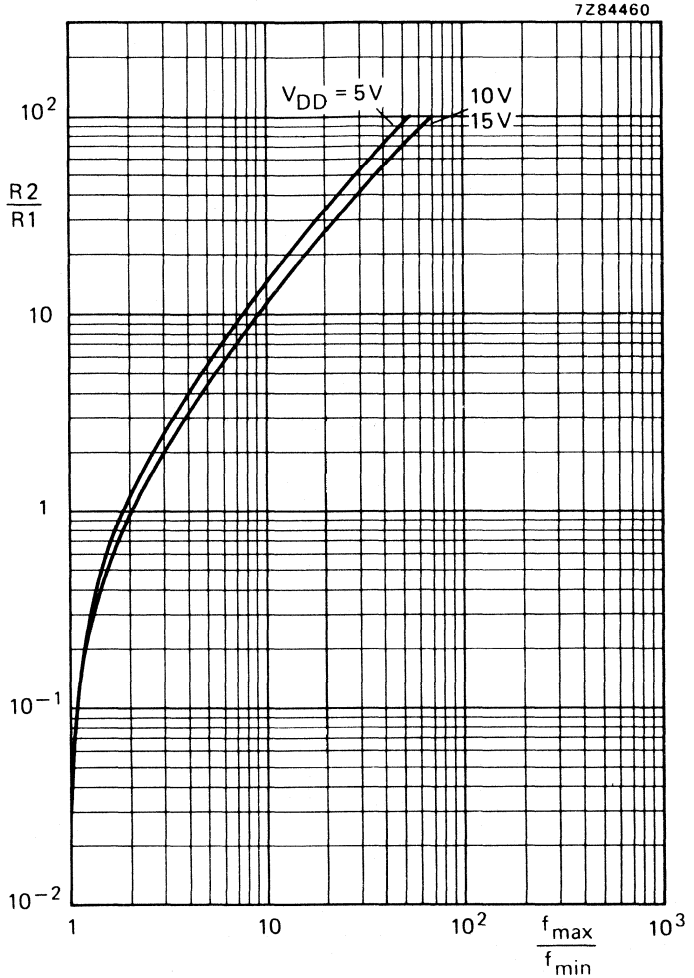


Fig. 9 Typical ratio of R2/R1 as a function of the ratio f_{max}/f_{min}.

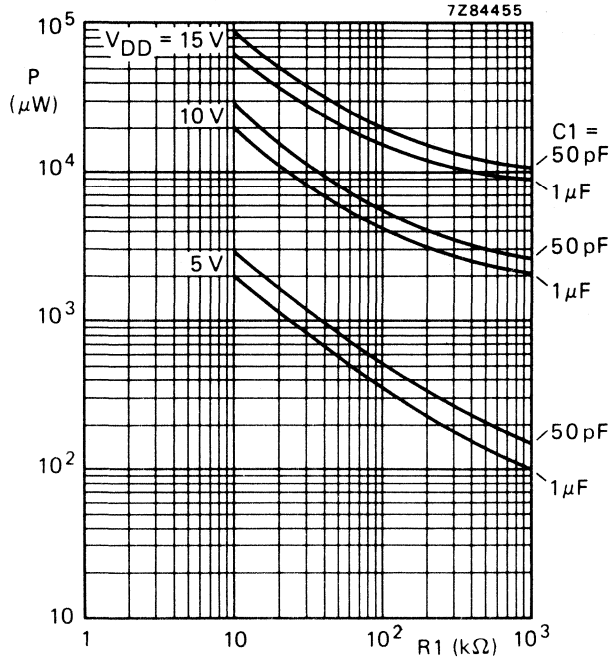


Fig. 10 Power dissipation as a function of R1; R2 = ∞; VCO_{IN} at ½ V_{DD}; C_L = 50 pF.

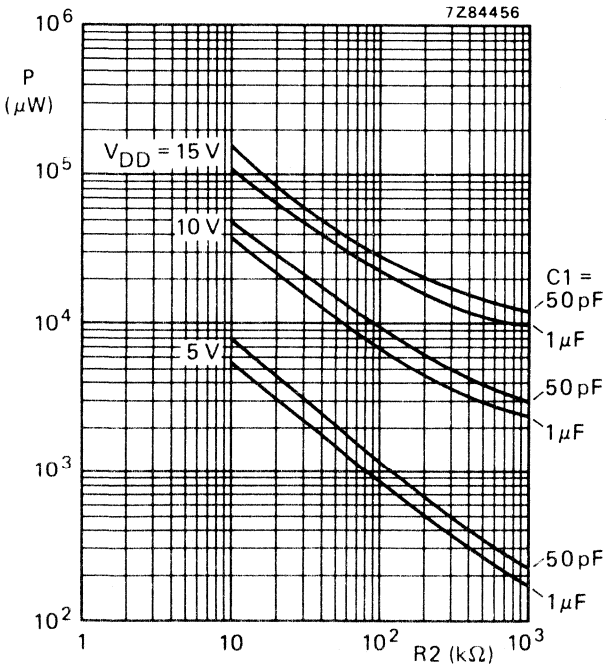


Fig. 11 Power dissipation as a function of R2; R1 = ∞; VCO_{IN} at V_{SS} (0 V); C_L = 50 pF.

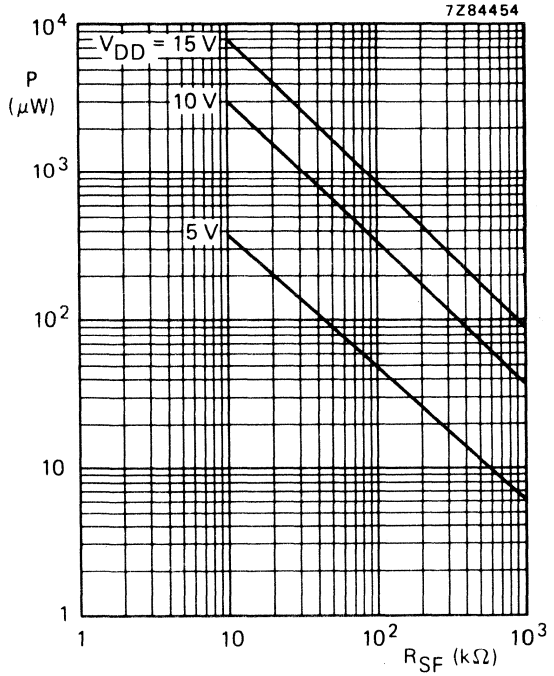


Fig. 12 Power dissipation of source follower as a function of R_{SF}; VCO_{IN} at ½ V_{DD}; R1 = ∞; R2 = ∞.

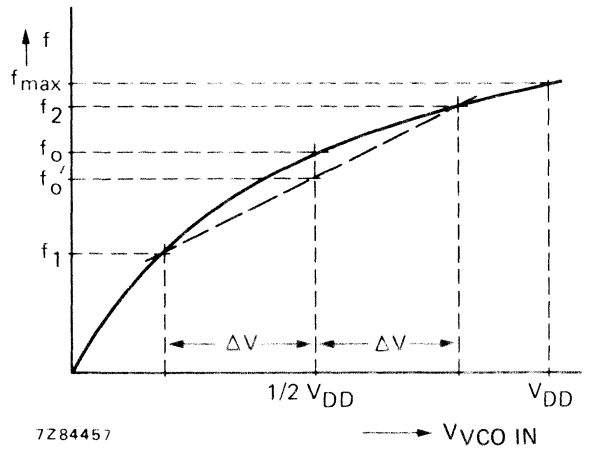


Fig. 13 Definition of linearity (see a.c. characteristics).

For VCO linearity:

$$f'_o = \frac{f_1 + f_2}{2}$$

$$\text{lin.} = \frac{f'_o - f_o}{f'_o} \times 100\%$$

Figure 13 and the above formula also apply to source follower linearity: substitute $V_{SF\ OUT}$ for f.

ΔV = 0,3 V at V_{DD} = 5 V
ΔV = 2,5 V at V_{DD} = 10 V
ΔV = 5 V at V_{DD} = 15 V

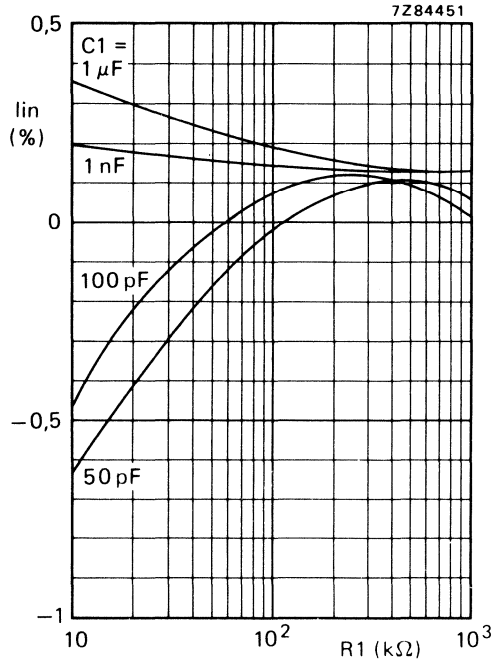


Fig. 14 VCO frequency linearity as a function of R1; R2 = ∞; V_{DD} = 5 V.

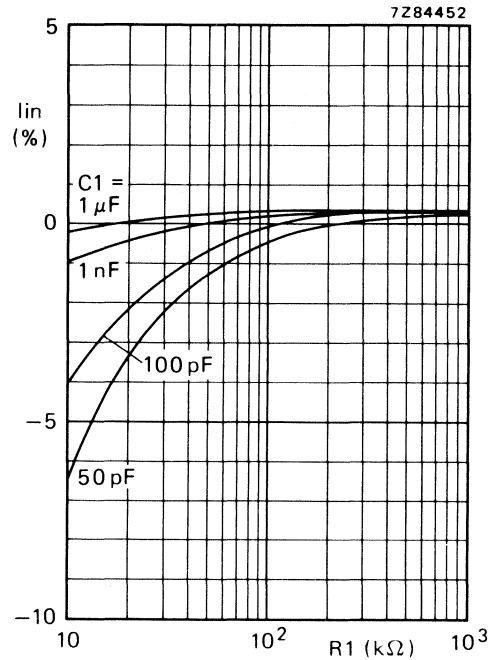


Fig. 15 VCO frequency linearity as a function of R1; R2 = ∞; V_{DD} = 10 V.

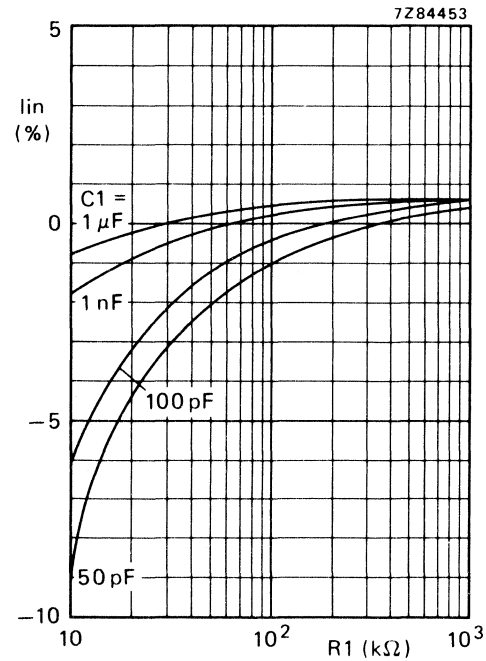


Fig. 16 VCO frequency linearity as a function of R1; R2 = ∞; V_{DD} = 15 V.

MONOSTABLE/ASTABLE MULTIVIBRATOR

The HEF4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include + TRIGGER, – TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and MR (Master Reset). Buffered outputs are O, $\overline{\text{O}}$ and OSCILLATOR OUTPUT. In all modes of operation an external capacitor (C_t) must be connected between C_{TC} and RC_{TC}, and an external resistor (R_t) must be connected between R_{TC} and RC_{TC} (continued on next page).

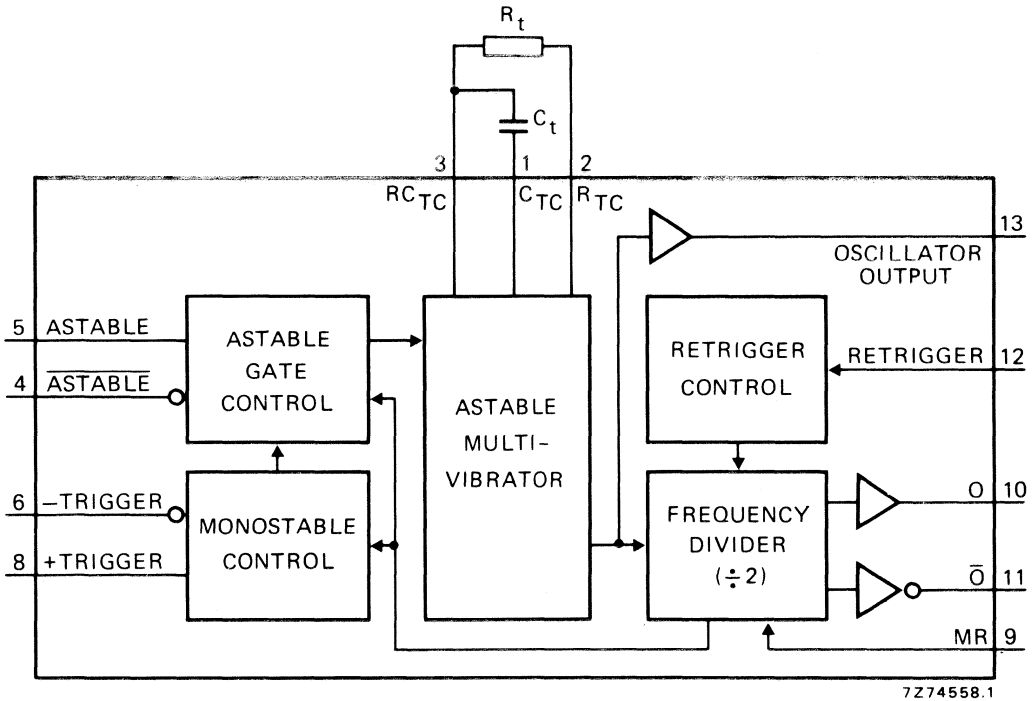


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

Astable operation is enabled by a HIGH level on the ASTABLE input. The period of the square wave at O and $\overline{O}$ outputs is a function of the external components employed. 'True' input pulses on the ASTABLE or 'complement' pulses on the $\overline{ASTABLE}$ input, allow the circuit to be used as a gatable multivibrator. The OSCILLATOR OUTPUT period will be half of the O output in the astable mode. However, a 50% duty factor is not guaranteed at this output.

In the monostable mode, positive edge-triggering is accomplished by applying a leading-edge pulse to the + TRIGGER input and a LOW level to the – TRIGGER input. For negative edge-triggering, a trailing-edge pulse is applied to the – TRIGGER and a HIGH level to the + TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading-edge only) by applying a common pulse to both the RETRIGGER and + TRIGGER inputs. In this mode the output pulse remains HIGH as long as the input pulse period is shorter than the period determined by the RC components.

An external count down option can be implemented by coupling O to an external 'N' counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{ASTABLE}$ input and has a duration equal to N times the period of the multivibrator. A HIGH level on the MR input assures no output pulse during an ON-power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a HIGH level or power-ON reset pulse must be applied to MR, whenever V_{DD} is applied.

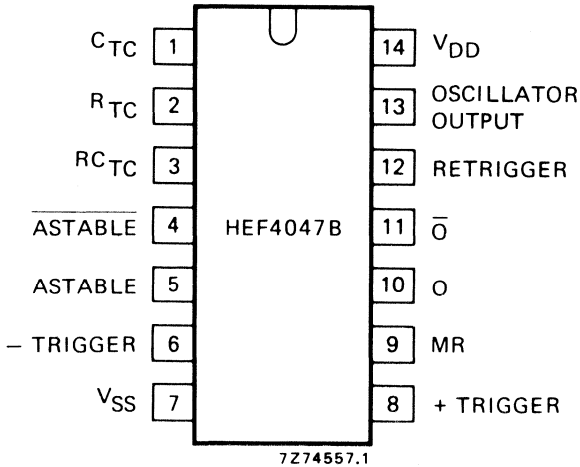
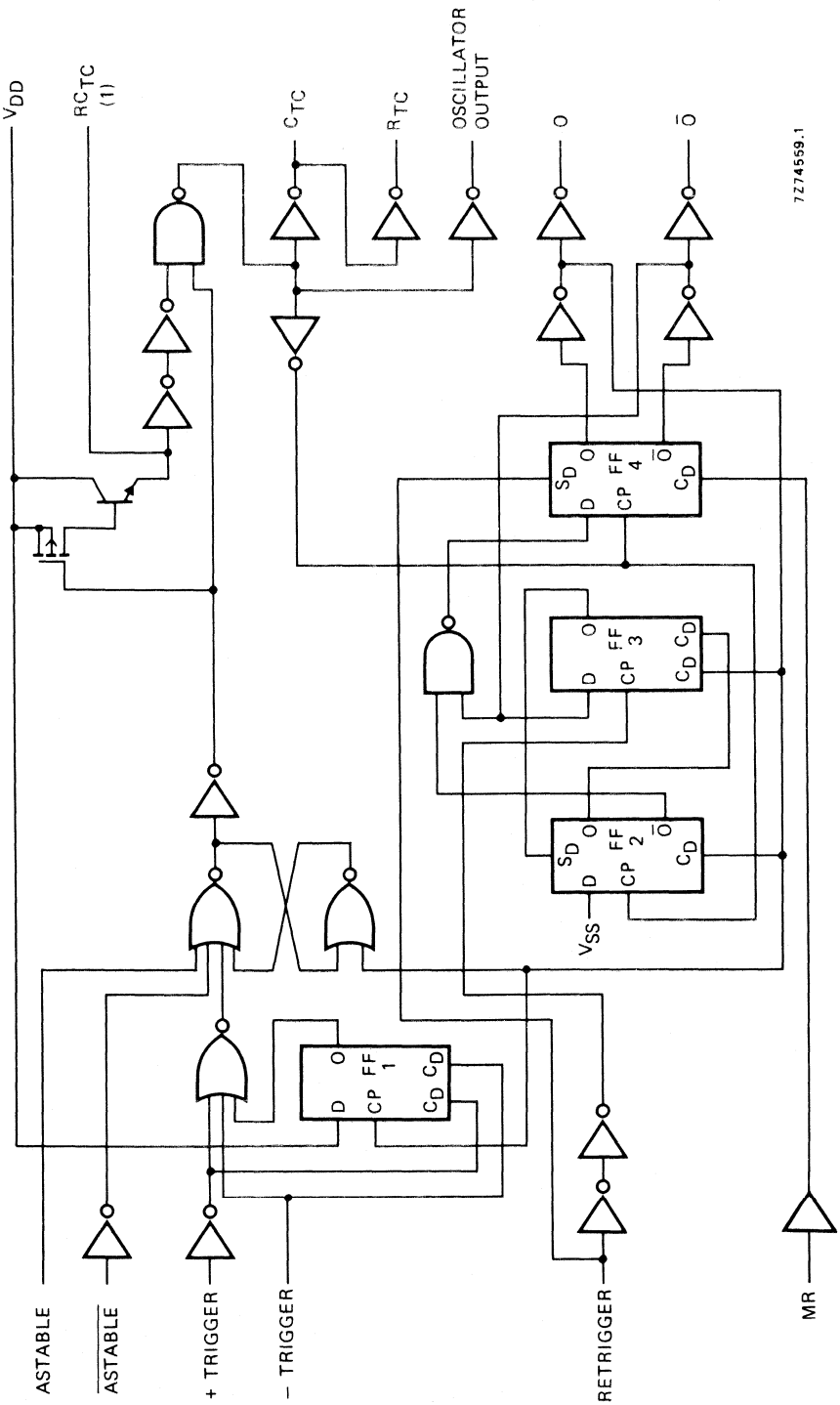


Fig. 2 Pinning diagram.

HEF4047BP : 14-lead DIL; plastic (SOT-27).
HEF4047BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4047BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).



(1) Special input protection that allows operating input voltages outside the supply voltage lines. Compared to the standard input protection pin 3 is more sensitive to static discharge; extra handling precautions are recommended.

Fig. 3 Logic diagram.

FUNCTIONAL CONNECTIONS

function	pins connected to			output pulse from pins	output period or pulse width
	V_{DD}	V_{SS}	input pulse		
astable multivibrator					
free running	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	at pins 10, 11: $t_A = 4{,}40\ R_tC_t$
true gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	
complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	at pin 13: $t_A = 2{,}20\ R_tC_t$
monostable multivibrator					
pos. edge-triggering	4, 14	5, 6, 7, 9, 12	8	10, 11	
neg. edge-triggering	4, 8, 14	5, 7, 9, 12	6	10, 11	at pins 10, 11: $t_M = 2{,}48\ R_tC_t$
retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
external count down*	14	5, 6, 7, 8, 9, 12	–	10, 11	

* Input pulse to RESET of external counting chip; external counting chip output to pin 4.

Note

In all cases, external resistor between pins 2 and 3, external capacitor between pins 1 and 3.

D.C. CHARACTERISTICS

V_{SS} = 0 V; inputs at V_{SS} or V_{DD}

	V_{DD} V	symbol	T_{amb} (°C) −40 max.	+ 25 min.	+ 25 max.	+ 85 max.		
Leakage current pin 3; output transistor OFF	15	I_3	0,3	–	0,3	1	μA	pin 3 at V_{DD} or V_{SS}

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
ASTABLE, $\overline{\text{ASTABLE}}$						
→ OSC. OUTPUT	5			95	190	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	43 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
	5			85	170	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	29 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
ASTABLE, $\overline{\text{ASTABLE}}$						
→ O, $\overline{\text{O}}$	5			150	300	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
	5			130	260	103 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	49 ns + (0,23 ns/pF) C_L
	15			45	90	37 ns + (0,16 ns/pF) C_L
+/– TRIGGER						
→ O, $\overline{\text{O}}$	5			160	320	133 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
	5			155	310	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
+ TRIGGER,						
RETRIGGER → $\overline{\text{O}}$	5			65	130	38 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60	19 ns + (0,23 ns/pF) C_L
	15			25	50	17 ns + (0,16 ns/pF) C_L
+ TRIGGER,						
RETRIGGER → O	5			95	190	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	29 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
MR → O	5			100	200	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	34 ns + (0,23 ns/pF) C_L
	15			35	70	27 ns + (0,16 ns/pF) C_L
MR → $\overline{\text{O}}$	5			100	200	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90	34 ns + (0,23 ns/pF) C_L
	15			35	70	27 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times							
HIGH to LOW	5	t_{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum MR pulse width; HIGH	5	t_{WMRH}	60	30		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum input pulse width; any input exept MR	5	t_W	220	110		ns	
	10		100	50		ns	
	15		70	35		ns	

APPLICATION INFORMATION

General features:

- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

Monostable multivibrator features:

- Positive- or negative-edge triggering
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse-width expansion
- Long pulse width possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

Astable multivibrator features:

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available

1. Astable mode design information

a. Unit-to-unit transfer-voltage variations

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift for free running (astable) operation.

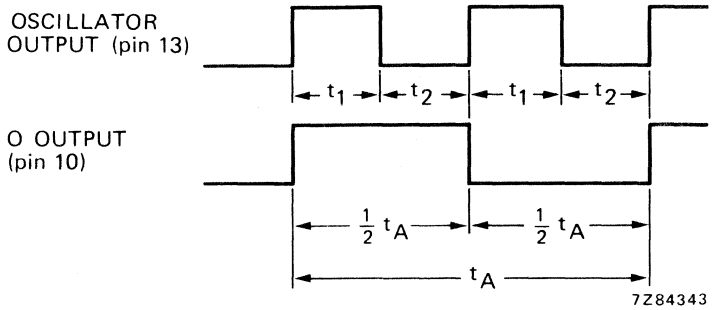


Fig. 4 Astable mode waveforms.

$$t_1 = -R_t C_t \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -R_t C_t \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2\,(t_1 + t_2) = -2R_t C_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$, where t_A = Astable mode pulse width.

Values for t_A are:

V_{DD} = 5 or 10 V	typ. : $V_{TR} = 0{,}5\ V_{DD}$;	$t_A = 4{,}40\ R_t C_t$
	min. : $V_{TR} = 0{,}3\ V_{DD}$;	$t_A = 4{,}71\ R_t C_t$
	max.: $V_{TR} = 0{,}7\ V_{DD}$;	$t_A = 4{,}71\ R_t C_t$
V_{DD} = 15 V	min. : V_{TR} = 4 V;	$t_A = 4{,}84\ R_t C_t$
	max.: V_{TR} = 11 V;	$t_A = 4{,}84\ R_t C_t$

thus if $\mathbf{t_A = 4{,}40\ R_t C_t}$ is used, the maximum variation will be (+ 7,0%; −0,0%) at 10 V.

APPLICATION INFORMATION (continued)

b. Variations due to changes in V_{DD}

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD}.
Typical variations are presented graphically in Figs 5 and 6 with 10 V as a reference.

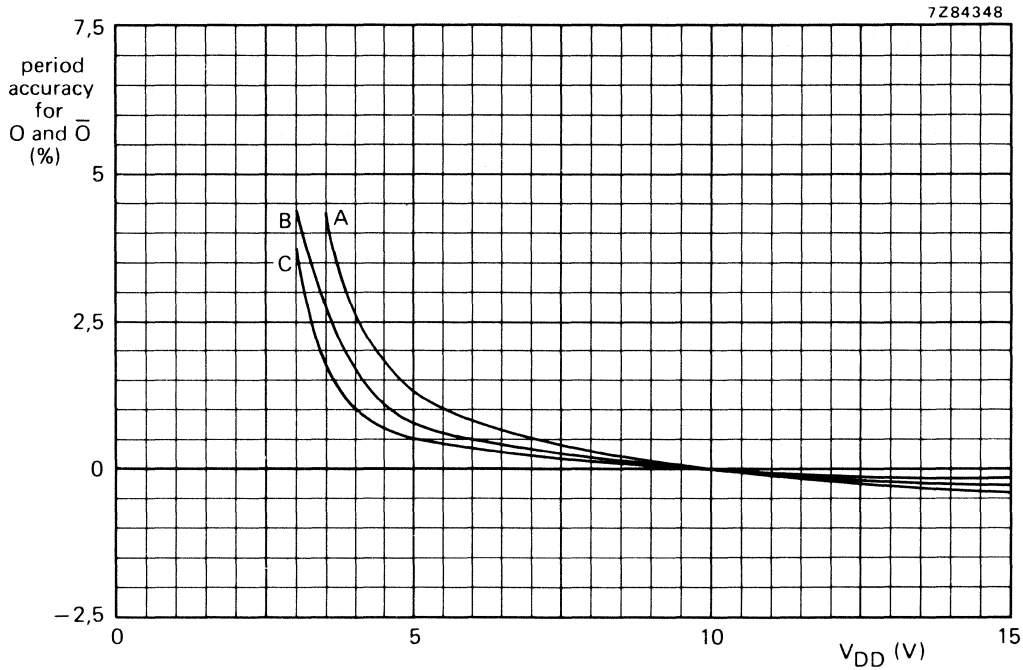


Fig. 5 Typical O and $\overline{O}$ period accuracy as a function of supply voltage; astable mode; T_{amb} = 25 °C.

curve	f_o kHz	C_t pF	R_t kΩ
A	10	100	220
B	5	100	470
C	1	1000	220

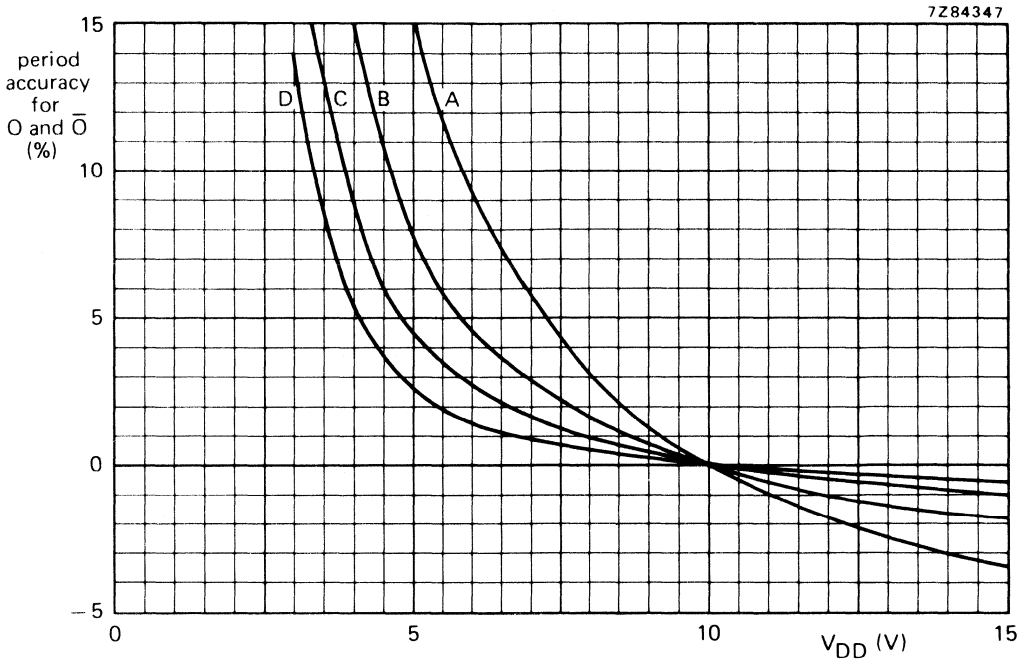


Fig. 6 Typical O and $\overline{O}$ period accuracy as a function of supply voltage; astable mode; T_{amb} = 25 °C.

curve	f_o kHz	C_t pF	R_t kΩ
A	500	10	47
B	225	100	10
C	100	100	22
D	50	100	47

APPLICATION INFORMATION (continued)

2. Monostable mode design information

The following analysis presents worst case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift for one-shot (monostalbe) operation.

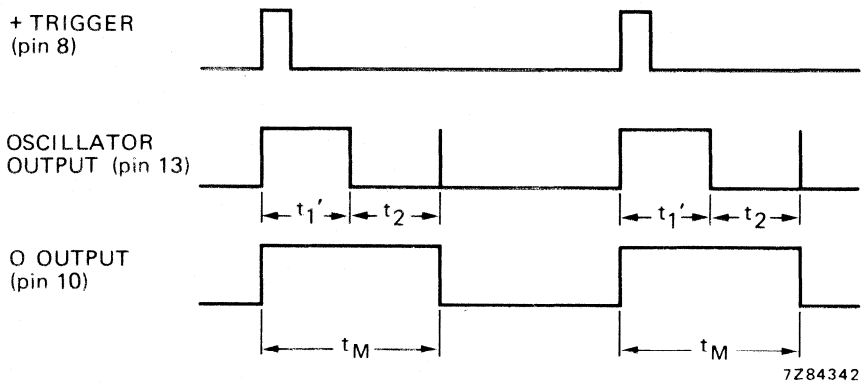


Fig. 7 Monostable waveforms.

$$t_1' = -R_tC_t \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -R_tC_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$, where t_M = Monostable mode pulse width.

Values for t_M are:

	typ. : $V_{TR} = 0{,}5\ V_{DD}$;	$t_M = 2{,}48\ R_tC_t$
V_{DD} = 5 to 10 V	min. : $V_{TR} = 0{,}3\ V_{DD}$;	$t_M = 2{,}78\ R_tC_t$
	max.: $V_{TR} = 0{,}7\ V_{DD}$;	$t_M = 2{,}52\ R_tC_t$
V_{DD} = 15 V	min. : V_{TR} = 4 V;	$t_M = 2{,}88\ R_tC_t$
	max.: V_{TR} = 11 V;	$t_M = 2{,}56\ R_tC_t$

thus if $t_M = 2{,}48\ R_tC_t$ is used, the maximum variation will be (+ 12%; −0,0%) at 10 V.

Note
In the astable mode, the first positive half cycle has a duration of t_M; succeeding durations are ½ t_A.

3. Retrigger mode operation

The HEF4047B can be used in the retrigger mode to extend the output pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to pins 8 and 12, and the output is taken from pin 10 or 11. Normal monostable action is obtained when one retrigger pulse is applied (Fig. 8).
Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$.
For more than two pulses, t_{RE} (output O), terminates at some variable time, t_D, after the termination of the last retrigger pulse; t_D is variable because t_{RE} (output O) terminates after the second positive edge of the oscillator output appears at flip-flop 4.

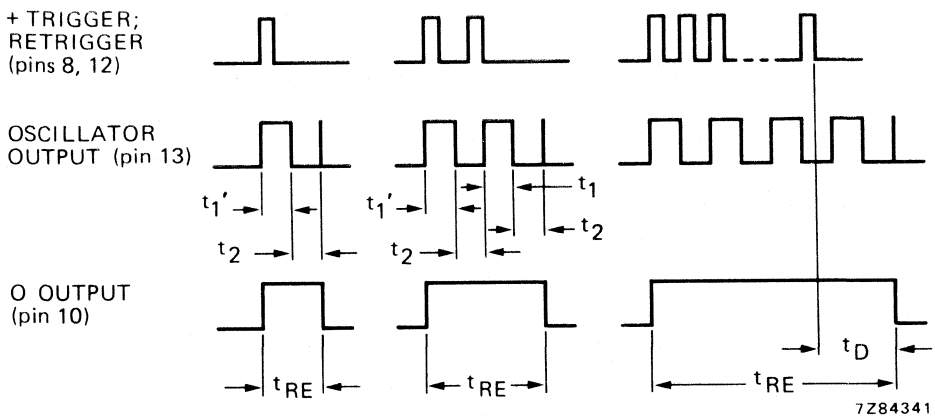


Fig. 8 Retrigger mode waveforms.

4. External counter option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 9.
The pulse duration at the output is:

$$t_{ext} = (N - 1)(t_A) + (t_M + \tfrac{1}{2}\, t_A)$$

Where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

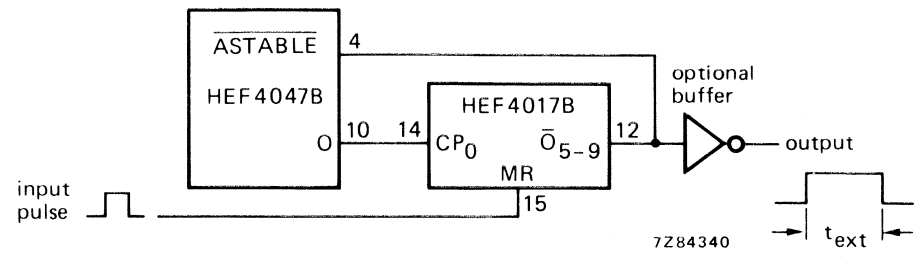


Fig. 9 Implementation of external counter option.

APPLICATION INFORMATION (continued)

5. Timing component limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used).
There is no upper or lower limit for either R_t or C_t value to maintain oscillation.
However, in consideration of accuracy, C_t must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account).
R_t must be much larger than the LOCMOS 'ON' resistance in series with it, which typically is hundreds of ohms.

The recommended values for R_t and C_t to maintain agreement with previously calculated formulae without trimming should be:

$C_t \geqslant 100$ pF, up to any practical value,

$10\ k\Omega \leqslant R_t \leqslant 1\ M\Omega$.

6. Power consumption

In the standby mode (monostable or astable), power dissipation will be a function of leakage current in the circuit.
For dynamic operation, the power needed to charge the external timing capacitor C_t is given by the following formulae:

Astable mode: $P = 2\ C_t\ V^2\ f$ (f at output pin 13)

$P = 4\ C_t\ V^2\ f$ (f at output pins 10 and 11)

Monostable mode: $P = \dfrac{(2{,}9\ C_t\ V^2)(\text{duty cycle})}{T}$ (f at output pins 10 and 11)

Because the power dissipation does not depend on R_t, a design for minimum power dissipation would be a small value of C_t. The value of R would depend on the desired period (within the limitations discussed previously).
Typical power consumption in astable mode is shown in Figs 10, 11 and 12.

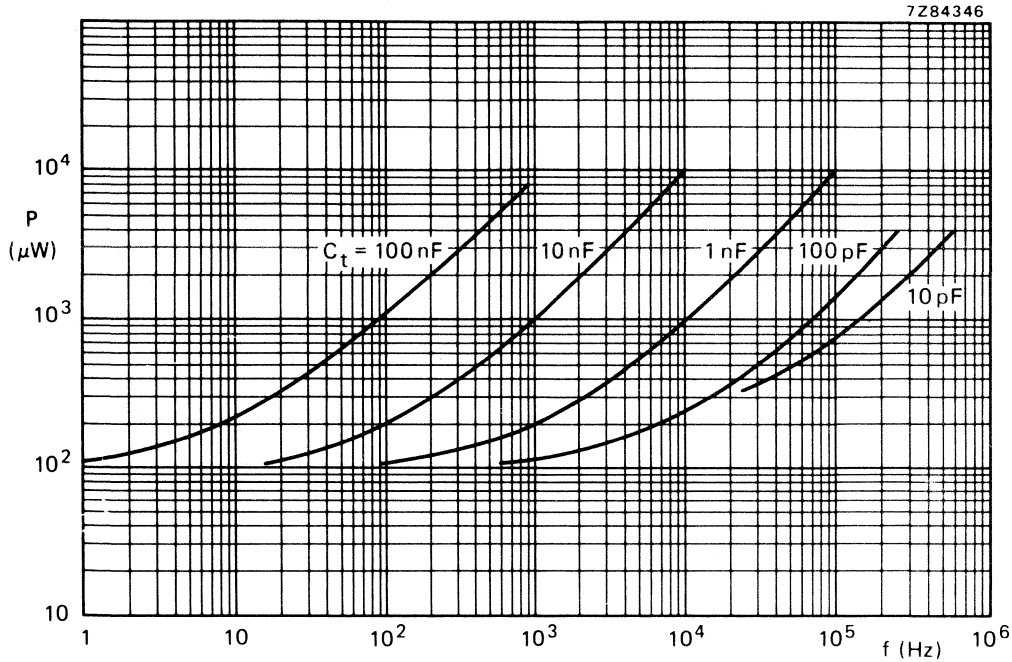


Fig. 10 Power consumption as a function of the output frequency at O or $\overline{O}$; V_{DD} = 5 V; astable mode.

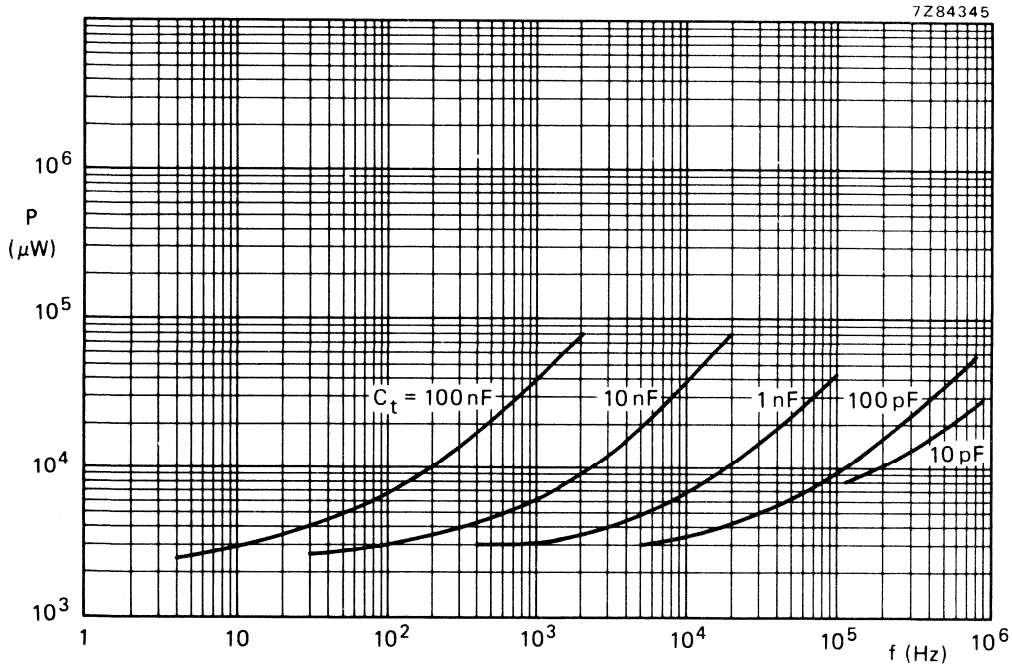


Fig. 11 Power consumption as a function of the output frequency at O or $\overline{O}$; V_{DD} = 10 V; astable mode.

APPLICATION INFORMATION (continued)

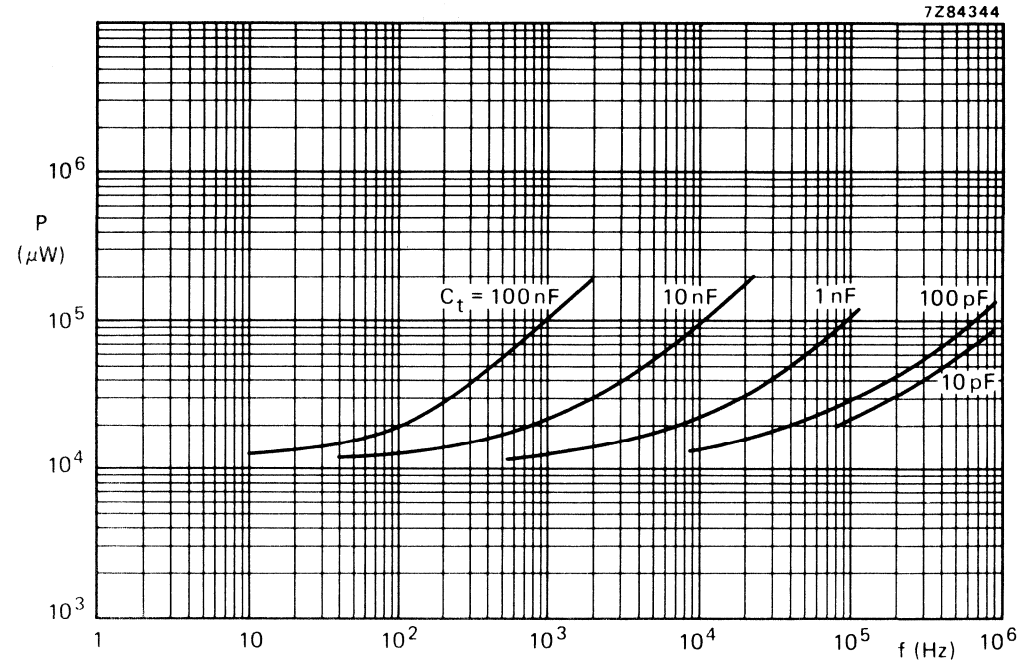


Fig. 12 Power consumption as a function of the output frequency at O or $\overline{O}$; V_{DD} = 15 V; astable mode.

HEX INVERTING BUFFERS

The HEF4049B provides six inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table below.

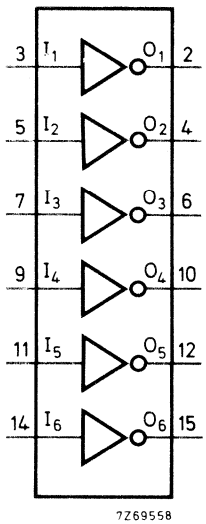


Fig. 1 Functional diagram.

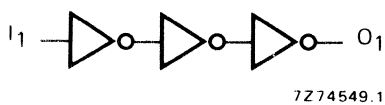


Fig. 3 Logic diagram (one gate).

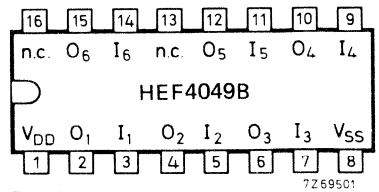


Fig. 2 Pinning diagram.

HEF4049BP : 16-lead DIL; plastic (SOT-38Z).
HEF4049BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4049BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Guaranteed fan-out in common logic families

driven element	guaranteed fan-out
standard TTL	2
74LS	9
74L	16

Input protection

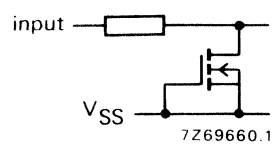


Fig. 4 Input protection circuit that allows input voltages in excess of V_{DD}.

APPLICATION INFORMATION

Some examples of applications for the HEF4049B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

FAMILY DATA

I_{DD} LIMITS category BUFFERS } see Family Specifications

D.C. CHARACTERISTICS V_{SS} = 0 V; V_I = V_{SS} or V_{DD}

HEF	V_{DD} V	V_O V	symbol	T_{amb}(°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,5	–	2,9	–	2,3	–	mA
	10	0,5		12,0	–	10,0	–	8,0	–	mA
	15	1,5		24,0	–	20,0	–	16,0	–	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA
	10	9,5		1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA
Output (source) current HIGH	5	2,5	$-I_{OH}$	1,7	–	1,4	–	1,1	–	mA

HEC	V_{DD} V	V_O V	symbol	T_{amb}(°C) −55 min.	−55 max.	+25 min.	+25 max.	+125 min.	+125 max.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,6	–	2,9	–	1,9	–	mA
	10	0,5		12,5	–	10,0	–	6,7	–	mA
	15	1,5		25,0	–	20,0	–	13,0	–	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA
	10	9,5		1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	35	70	ns	26 ns + (0,18 ns/pF) C_L
	10		15	30	ns	11 ns + (0,08 ns/pF) C_L
	15		12	25	ns	9 ns + (0,05 ns/pF) C_L
LOW to HIGH	5	t_{PLH}	50	100	ns	23 ns + (0,55 ns/pF) C_L
	10		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5	t_{THL}	20	40	ns	3 ns + (0,35 ns/pF) C_L
	10		10	20	ns	3 ns + (0,14 ns/pF) C_L
	15		7	14	ns	2 ns + (0,09 ns/pF) C_L
LOW to HIGH	5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2 500 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	f_i = input freq. (MHz)
	10	11 000 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	f_o = output freq. (MHz)
	15	35 000 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

HEX NON-INVERTING BUFFERS

The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table below.

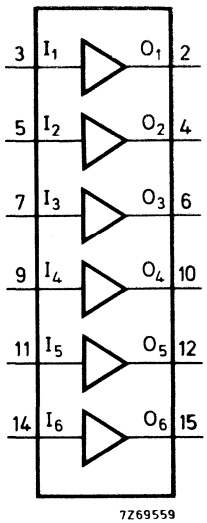


Fig. 1 Functional diagram.

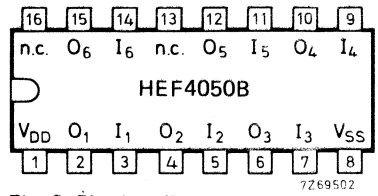


Fig. 2 Pinning diagram.

HEF4050BP : 16-lead DIL; plastic (SOT-38Z).
HEF4050BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4050BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Guaranteed fan-out in common logic families

driven element	guaranteed fan-out
standard TTL	2
74LS	9
74L	16

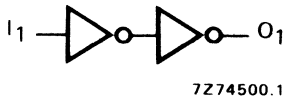


Fig. 3 Logic diagram (one gate).

Input protection

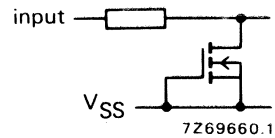


Fig.4 Input protection circuit that allows input voltages in excess of V_{DD}.

APPLICATION INFORMATION

Some examples of applications for the HEF4050B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

FAMILY DATA
I_{DD} LIMITS category BUFFERS } see Family Specifications

D.C. CHARACTERISTICS $V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD}

HEF	V_{DD} V	V_O V	symbol	T_{amb}(°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,5	–	2,9	–	2,3	–	mA
	10	0,5		12,0	–	10,0	–	8,0	–	mA
	15	1,5		24,0	–	20,0	–	16,0	–	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA
	10	9,5		1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA
Output (source) current HIGH	5	2,5	$-I_{OH}$	1,7	–	1,4	–	1,1	–	mA

HEC	V_{DD} V	V_O V	symbol	T_{amb}(°C) −55 min.	−55 max.	+25 min.	+25 max.	+125 min.	+125 max.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,6	–	2,9	–	1,9	–	mA
	10	0,5		12,5	–	10,0	–	6,7	–	mA
	15	1,5		25,0	–	20,0	–	13,0	–	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA
	10	9,5		1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA

A.C. CHARACTERISTICS $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays I_n → O_n HIGH to LOW	5	t_{PHL}	35	70	ns	26 ns + (0,18 ns/pF)C_L
	10		20	35	ns	16 ns + (0,08 ns/pF)C_L
	15		15	30	ns	12 ns + (0,05 ns/pF)C_L
LOW to HIGH	5	t_{PLH}	55	110	ns	28 ns + (0,55 ns/pF)C_L
	10		25	55	ns	14 ns + (0,23 ns/pF)C_L
	15		20	40	ns	12 ns + (0,16 ns/pF)C_L
Output transition times HIGH to LOW	5	t_{THL}	25	50	ns	7 ns + (0,35 ns/pF)C_L
	10		10	20	ns	3 ns + (0,14 ns/pF)C_L
	15		7	14	ns	2 ns + (0,09 ns/pF)C_L
LOW to HIGH	5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF)C_L
	10		30	60	ns	9 ns + (0,42 ns/pF)C_L
	15		20	40	ns	6 ns + (0,28 ns/pF)C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	3 800 f_i + Σ ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz)
	10	11 600 f_i + Σ ($f_o C_L$) × V_{DD}^2	f_o = output freq. (MHz)
	15	65 900 f_i + Σ ($f_o C_L$) × V_{DD}^2	C_L = load capacitance (pF)
			Σ($f_o C_L$) = sum of outputs
			V_{DD} = supply voltage (V)

8-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4051B is an 8-channel analogue multiplexer/demultiplexer with three address inputs (A_0 to A_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The device contains eight bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by A_0 to A_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 to A_2.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 to A_2, and $\overline{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

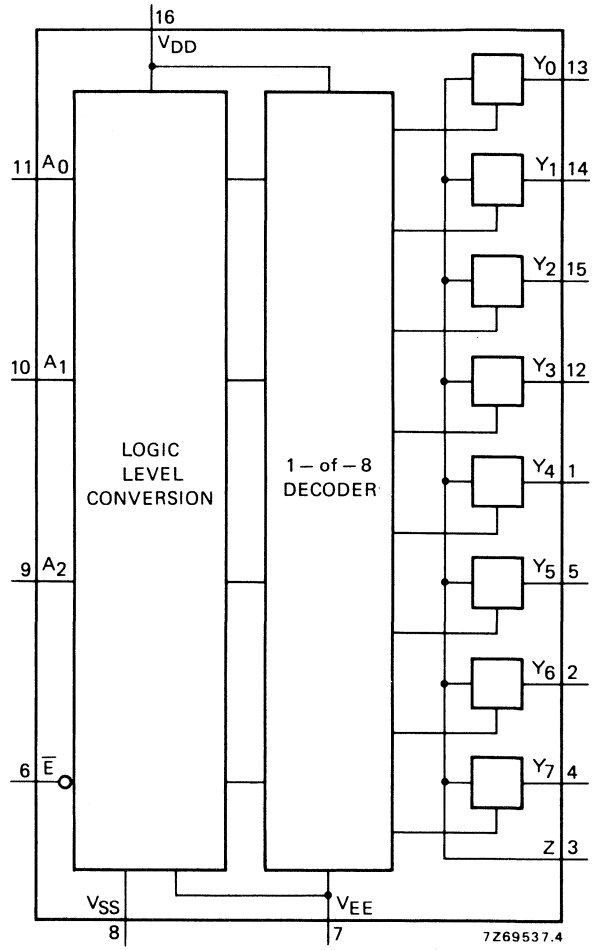


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

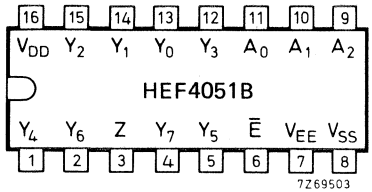


Fig. 2 Pinning diagram.

PINNING

Y_0 to Y_7	independent inputs/outputs
A_0 to A_2	address inputs
$\bar{E}$	enable input (active LOW)
Z	common input/output

HEF4051BP : 16-lead DIL; plastic (SOT-38Z).
HEF4051BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4051BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

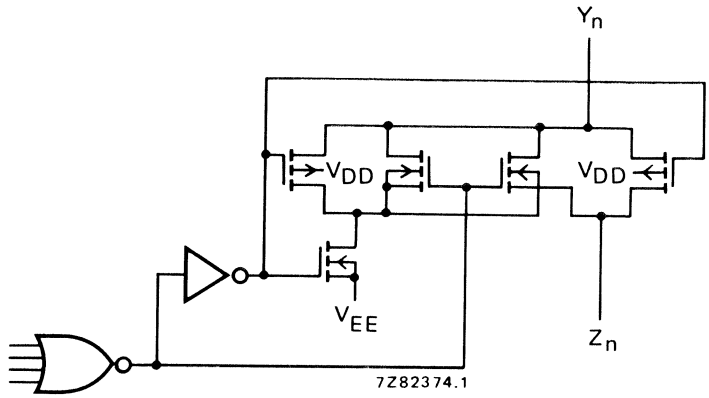


Fig. 3 Schematic diagram (one switch).

FUNCTION TABLE

inputs				channel ON
$\bar{E}$	A_2	A_1	A_0	
L	L	L	L	Y_0–Z
L	L	L	H	Y_1–Z
L	L	H	L	Y_2–Z
L	L	H	H	Y_3–Z
L	H	L	L	Y_4–Z
L	H	L	H	Y_5–Z
L	H	H	L	Y_6–Z
L	H	H	H	Y_7–Z
H	X	X	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

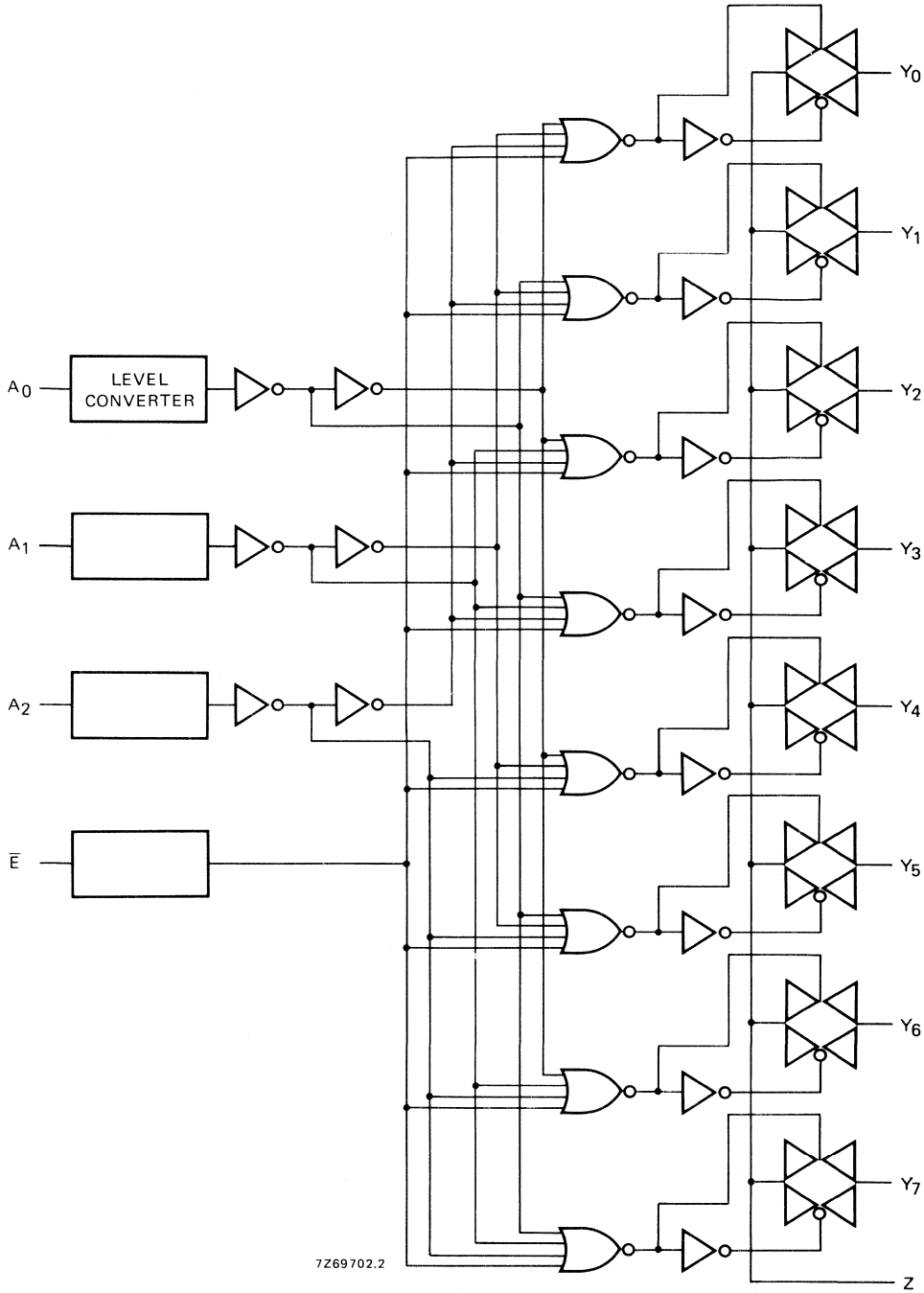


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.		conditions
ON resistance	5	R_{ON}	350	2500	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_{is} = 0 see Fig. 6
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_{is} = $V_{DD}-V_{EE}$ see Fig. 6
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	25	–	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD} V_{SS} = V_{EE}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS} V_{SS} = V_{EE}
	10		–	–	nA	
	15		–	200	nA	

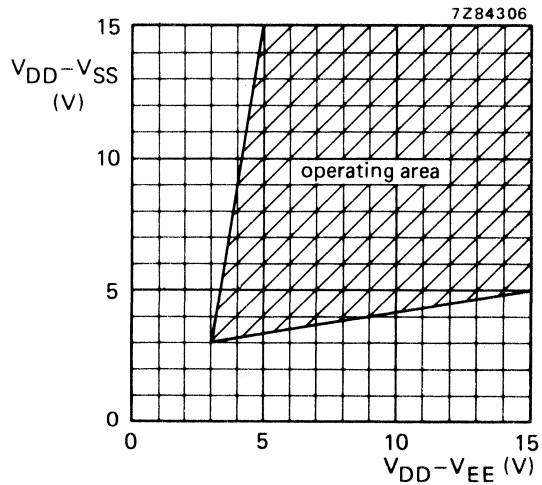


Fig. 5 Operating area as a function of the supply voltages.

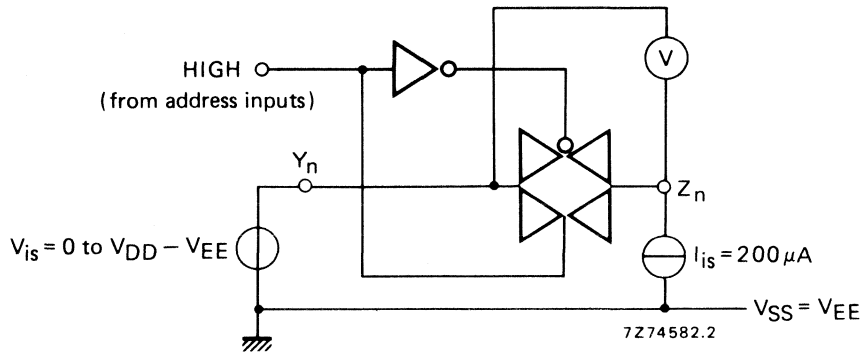


Fig. 6 Test set-up for measuring R_{ON}.

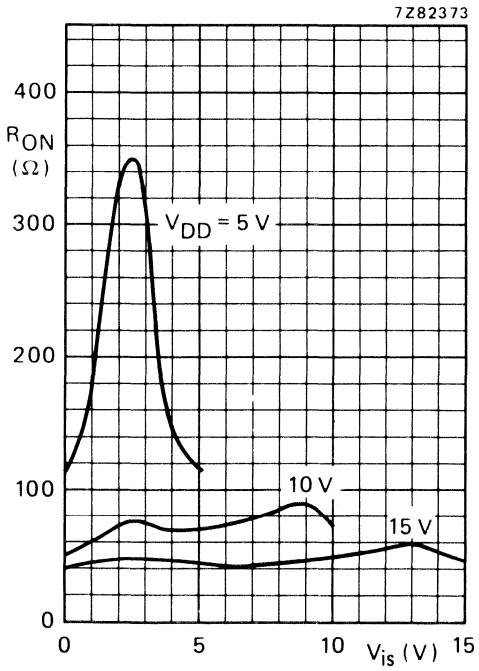


Fig. 7 Typical R_{ON} as a function of input voltage.

I_{is} = 200 μA
$V_{SS} = V_{EE}$ = 0 V

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		15	30	ns	
HIGH to LOW	10	t_{PHL}	5	10	ns	note 1
	15		5	10	ns	
	5		15	30	ns	
LOW to HIGH	10	t_{PLH}	5	10	ns	note 1
	15		5	10	ns	
$A_n \rightarrow V_{os}$	5		150	300	ns	
HIGH to LOW	10	t_{PHL}	60	120	ns	note 2
	15		45	90	ns	
	5		150	300	ns	
LOW to HIGH	10	t_{PLH}	65	130	ns	note 2
	15		45	90	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$	5		120	240	ns	
HIGH	10	t_{PHZ}	90	180	ns	note 3
	15		85	170	ns	
	5		145	290	ns	
LOW	10	t_{PLZ}	120	240	ns	note 3
	15		115	230	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$	5		140	280	ns	
HIGH	10	t_{PZH}	55	110	ns	note 3
	15		40	80	ns	
	5		140	280	ns	
LOW	10	t_{PZL}	55	110	ns	note 3
	15		40	80	ns	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
2. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PLH}; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PHL}; see Fig. 8.
3. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{DD}$ (square-wave);
   $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PHZ} and t_{PZH};
   $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 8.
4. $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_{is} = ½ V_{DD(p-p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $f_{is} = 1$ kHz; see Fig. 9.
5. $R_L = 1$ kΩ; $V_{is} = ½ V_{DD(p-p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 10.
6. $R_L = 10$ kΩ to V_{EE}; $C_L = 15$ pF to V_{EE}; $\overline{E}$ or $A_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 8.
7. $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_{is} = ½ V_{DD(p-p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 9.
8. $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_{is} = ½ V_{DD(p-p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 9.

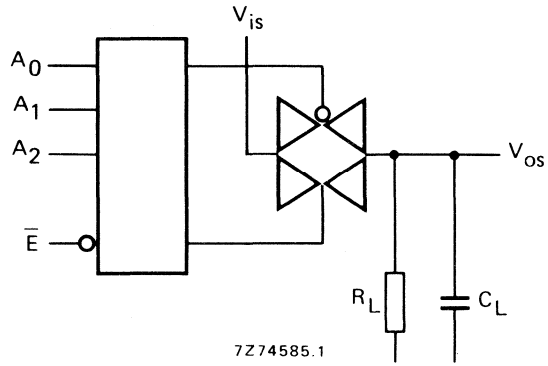


Fig. 8.

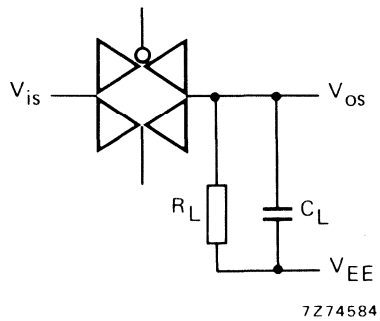


Fig. 9.

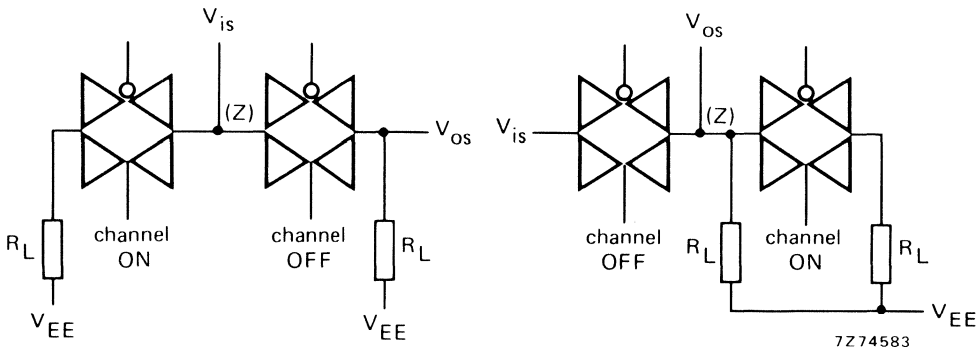


Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4051B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.

DUAL 4-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4052B is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (Y_0 to Y_3) and a common input/output (Z). The common channel select logic includes two address inputs (A_0 and A_1) and an active LOW enable input ($\overline{E}$).

Both multiplexers/demultiplexers contain four bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_3) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by A_0 and A_1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 and A_1.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0, A_1 and $\overline{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_3, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

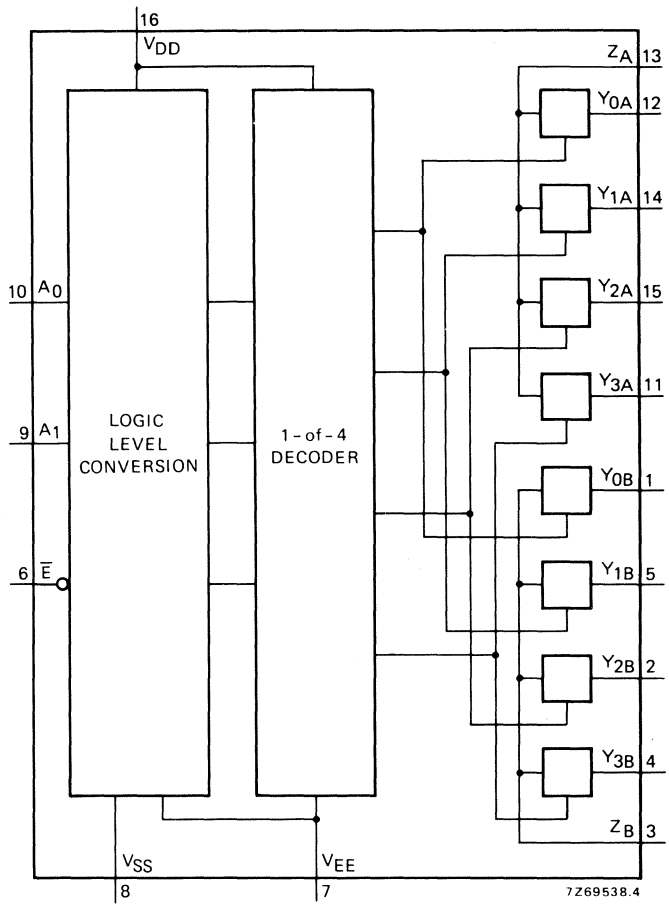


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

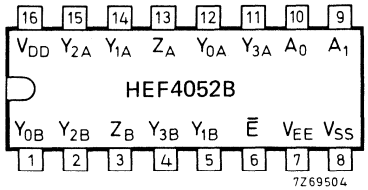


Fig. 2 Pinning diagram.

PINNING

Y_{0A} to Y_{3A}	independent inputs/outputs
Y_{0B} to Y_{3B}	independent inputs/outputs
A_0, A_1	address inputs
$\overline{E}$	enable input (active LOW)
Z_A, Z_B	common inputs/outputs

HEF4052BP : 16-lead DIL; plastic (SOT-38Z).
HEF4052BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4052BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

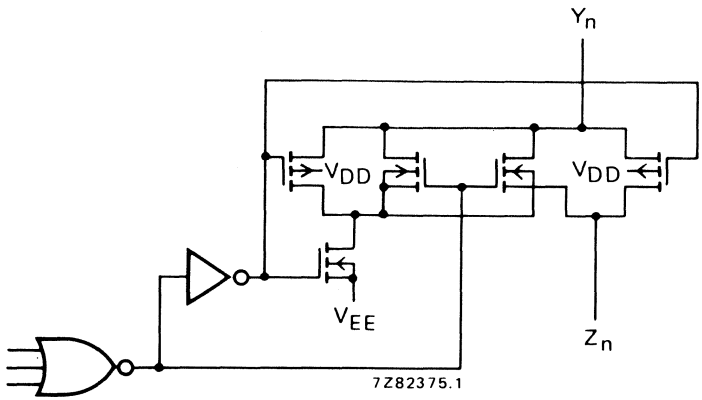


Fig. 3 Schematic diagram (one switch).

FUNCTION TABLE

inputs			channel ON
$\overline{E}$	A_1	A_0	
L	L	L	Y_{0A}–Z_A; Y_{0B}–Z_B
L	L	H	Y_{1A}–Z_A; Y_{1B}–Z_B
L	H	L	Y_{2A}–Z_A; Y_{2B}–Z_B
L	H	H	Y_{3A}–Z_A; Y_{3B}–Z_B
H	X	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

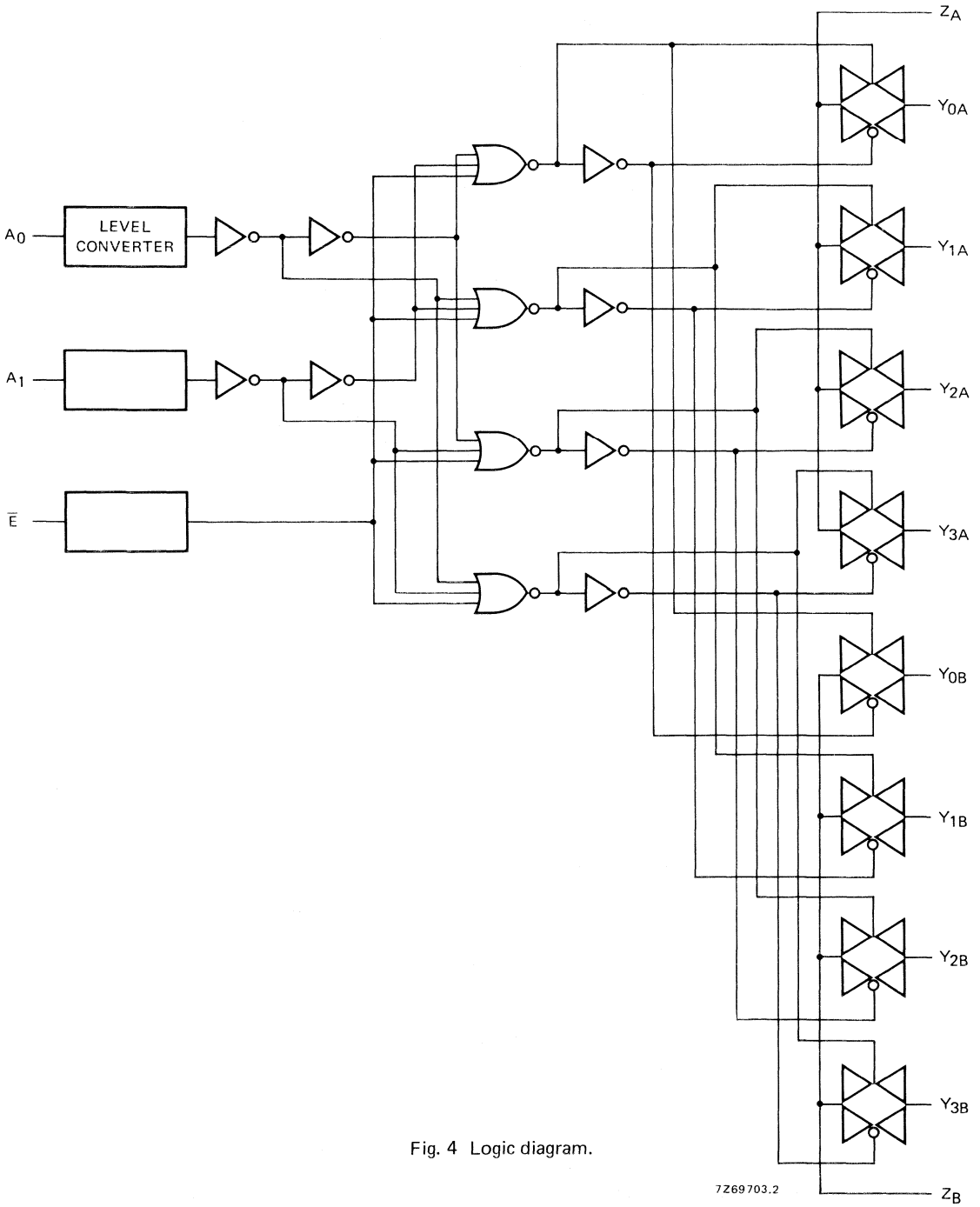


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.		conditions
ON resistance	5	R_{ON}	350	2500	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_{is} = 0 see Fig. 6
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_{is} = $V_{DD}-V_{EE}$ see Fig. 6
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	25	–	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

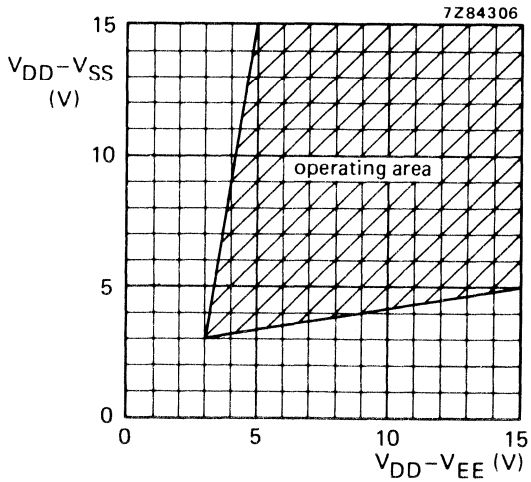


Fig. 5 Operating area as a function of the supply voltages.

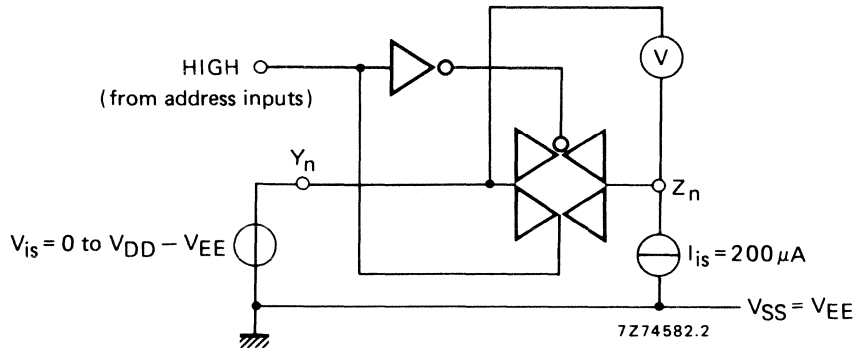


Fig. 6 Test set-up for measuring R_{ON}.

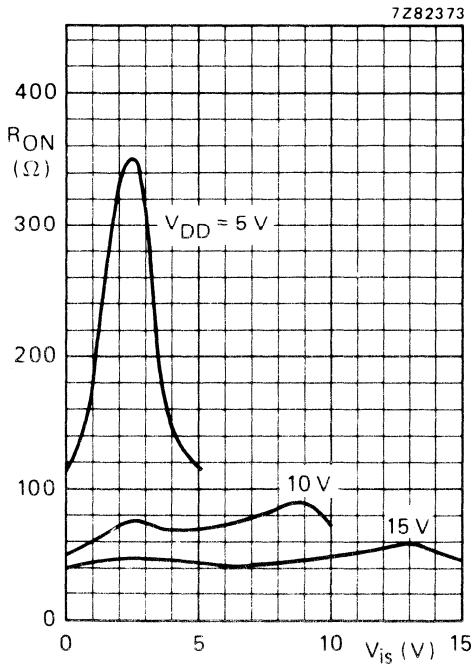


Fig. 7 Typical R_{ON} as a function of input voltage.
I_{is} = 200 μA
$V_{SS} = V_{EE}$ = 0 V

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		10	20	ns	
HIGH to LOW	10	t_{PHL}	5	10	ns	note 1
	15		5	10	ns	
	5		10	20	ns	
LOW to HIGH	10	t_{PLH}	5	10	ns	note 1
	15		5	10	ns	
$A_n \rightarrow V_{os}$	5		150	305	ns	
HIGH to LOW	10	t_{PHL}	65	135	ns	note 2
	15		50	100	ns	
	5		150	300	ns	
LOW to HIGH	10	t_{PLH}	75	150	ns	note 2
	15		50	100	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$	5		95	190	ns	
HIGH	10	t_{PHZ}	90	180	ns	note 3
	15		90	180	ns	
	5		100	205	ns	
LOW	10	t_{PLZ}	90	180	ns	note 3
	15		90	180	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$	5		130	260	ns	
HIGH	10	t_{PZH}	55	115	ns	note 3
	15		45	85	ns	
	5		120	240	ns	
LOW	10	t_{PZL}	50	100	ns	note 3
	15		35	75	ns	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times $\leqslant 20$ ns

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
2. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PLH}; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PHL}; see Fig. 8.
3. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{DD}$ (square-wave);
   $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PHZ} and t_{PZH};
   $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 8.
4. $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $f_{is} = 1$ kHz; see Fig. 9.
5. $R_L = 1$ kΩ; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 10.
6. $R_L = 10$ kΩ to V_{EE}; $C_L = 15$ pF to V_{EE}; $\overline{E}$ or $A_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 8.
7. $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 9.
8. $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 9.

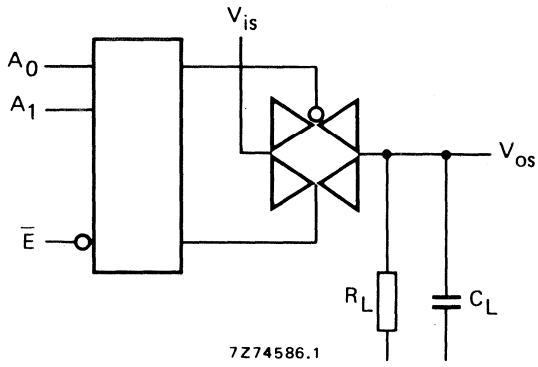


Fig. 8.

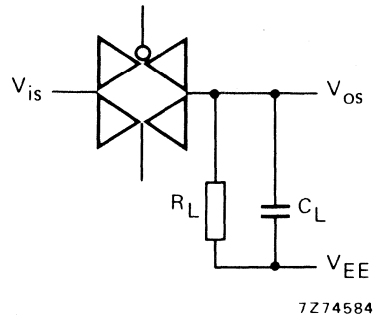


Fig. 9.

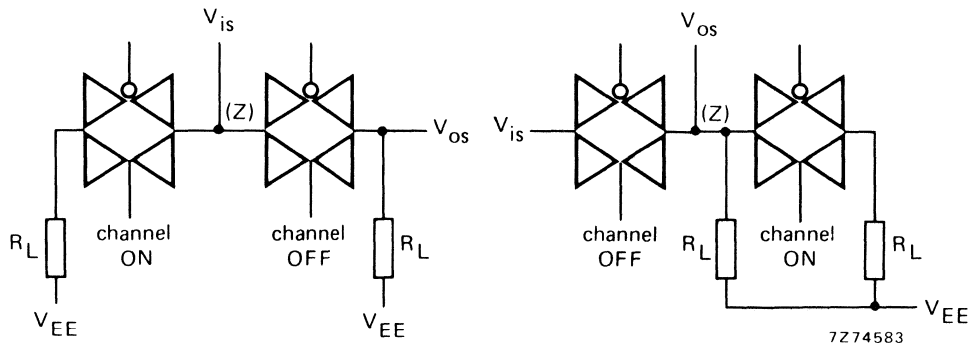


Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4052B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.

TRIPLE 2-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4053B is a triple 2-channel analogue multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (Y_0 and Y_1), a common input/output (Z), and select inputs (S_n). Each also contains two-bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 and Y_1) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_n. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_A to S_C.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_A to S_C and $\overline{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0, Y_1 and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

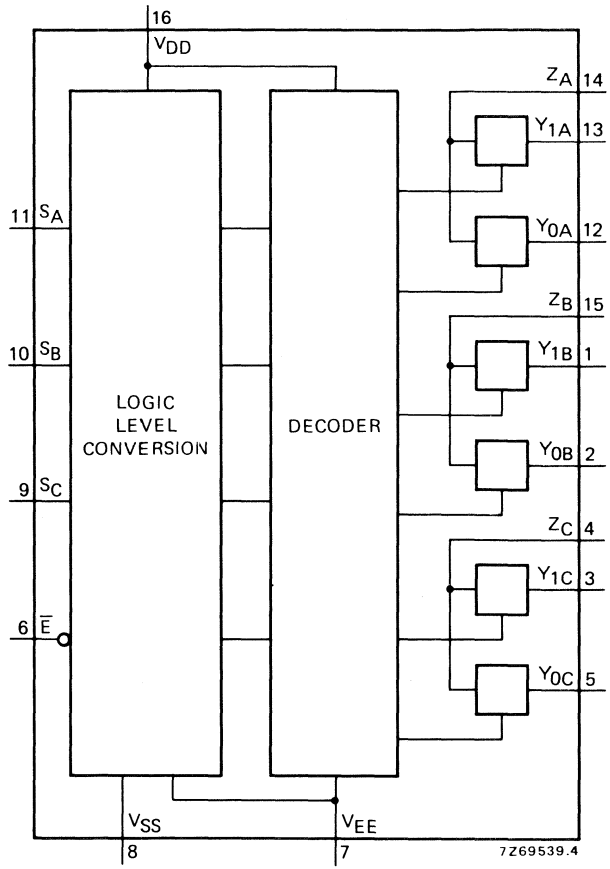


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Fig. 2 Pinning diagram.

PINNING

Y_{0A} to Y_{0C}	independent inputs/outputs
Y_{1A} to Y_{1C}	independent inputs/outputs
S_A to S_C	select inputs
$\overline{E}$	enable input (active LOW)
Z_A to Z_C	common inputs/outputs

HEF4053BP : 16-lead DIL; plastic (SOT-38Z).
HEF4053BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4053BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

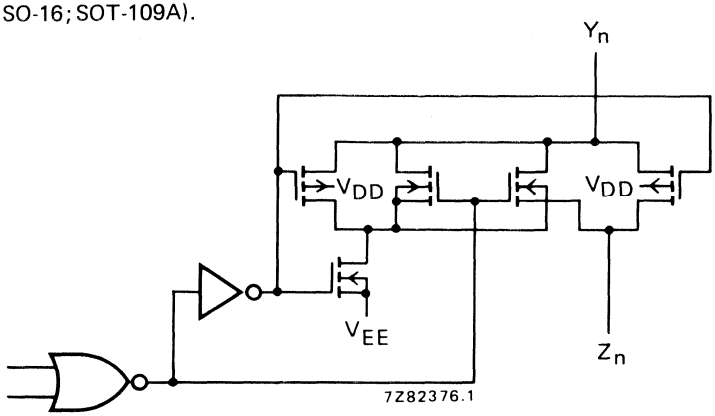


Fig. 3 Schematic diagram (one switch).

FUNCTION TABLE

inputs		channel ON
$\overline{E}$	S_n	
L	L	Y_{0n}–Z_n
L	H	Y_{1n}–Z_n
H	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

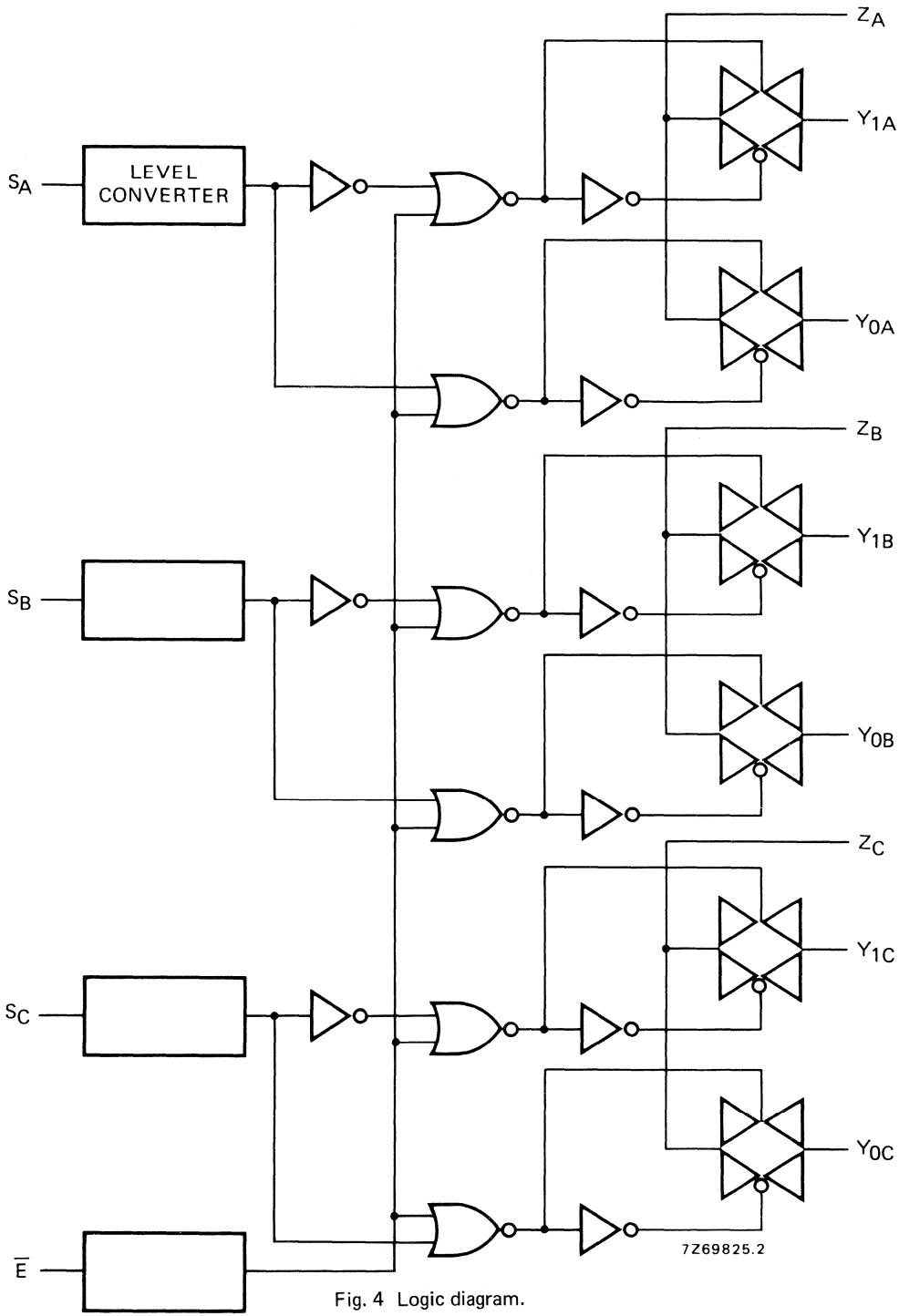


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.		conditions
ON resistance	5	R_{ON}	350	2500	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_{is} = 0 see Fig. 6
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_{is} = $V_{DD}-V_{EE}$ see Fig. 6
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	25	—	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	—	Ω	
	15		5	—	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	—	—	nA	$\overline{E}$ at V_{DD}
	10		—	—	nA	
	15		—	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	—	—	nA	$\overline{E}$ at V_{SS}
	10		—	—	nA	
	15		—	200	nA	

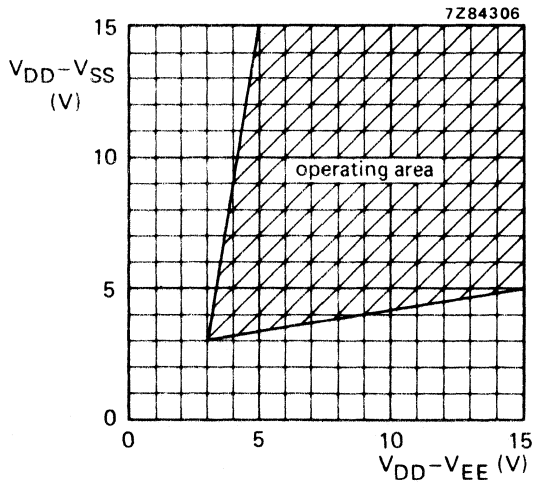


Fig. 5 Operating area as a function of the supply voltages.

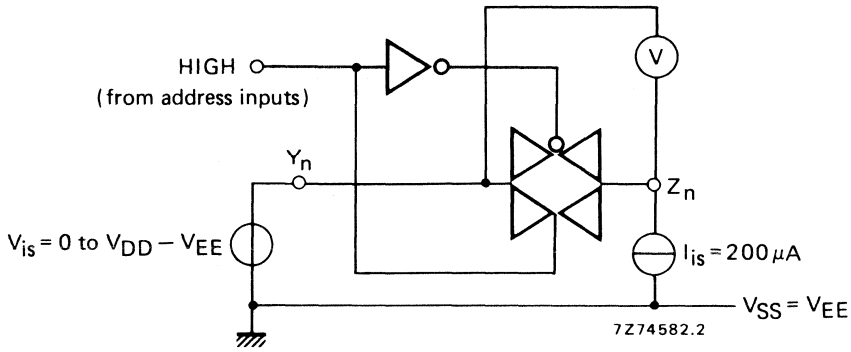


Fig. 6 Test set-up for measuring R_{ON}.

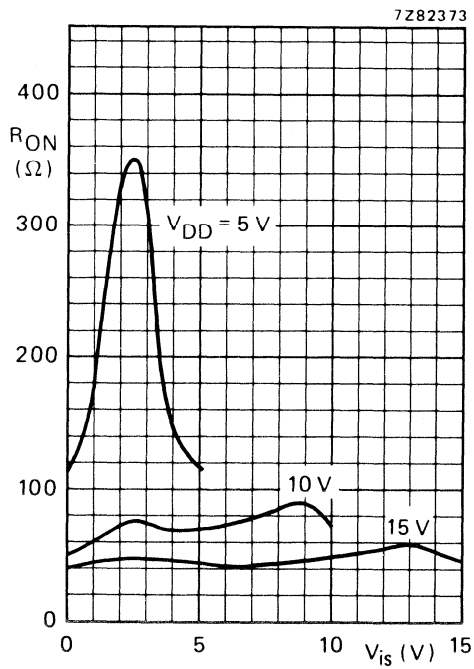


Fig. 7 Typical R_{ON} as a function of input voltage.

I_{is} = 200 μA
$V_{SS} = V_{EE}$ = 0 V

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$11\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$29\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \longrightarrow V_{os}$	5		10	20	ns	
HIGH to LOW	10	t_{PHL}	5	10	ns	note 1
	15		5	10	ns	
	5		15	30	ns	
LOW to HIGH	10	t_{PLH}	5	10	ns	note 1
	15		5	10	ns	
$S_n \longrightarrow V_{os}$	5		200	400	ns	
HIGH to LOW	10	t_{PHL}	85	170	ns	note 2
	15		65	130	ns	
	5		275	555	ns	
LOW to HIGH	10	t_{PLH}	100	200	ns	note 2
	15		65	130	ns	
Output disable times						
$\overline{E} \longrightarrow V_{os}$	5		200	400	ns	
HIGH	10	t_{PHZ}	115	230	ns	note 3
	15		110	220	ns	
	5		200	400	ns	
LOW	10	t_{PLZ}	120	245	ns	note 3
	15		110	215	ns	
Output enable times						
$\overline{E} \longrightarrow V_{os}$	5		260	525	ns	
HIGH	10	t_{PZH}	95	190	ns	note 3
	15		65	130	ns	
	5		280	565	ns	
LOW	10	t_{PZL}	105	205	ns	note 3
	15		70	140	ns	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
2. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $S_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PLH}; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PHL}; see Fig. 8.
3. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{DD}$ (square-wave);
   $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PHZ} and t_{PZH};
   $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 8.
4. $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); $f_{is} = 1$ kHz; see Fig. 9.
5. $R_L = 1$ kΩ; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 10.
6. $R_L = 10$ kΩ to V_{EE}; $C_L = 15$ pF to V_{EE}; $\overline{E}$ or $S_n = V_{DD}$ (square-wave); crosstalk is $\lvert V_{os} \rvert$ (peak value); see Fig. 8.
7. $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 9.
8. $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 9.

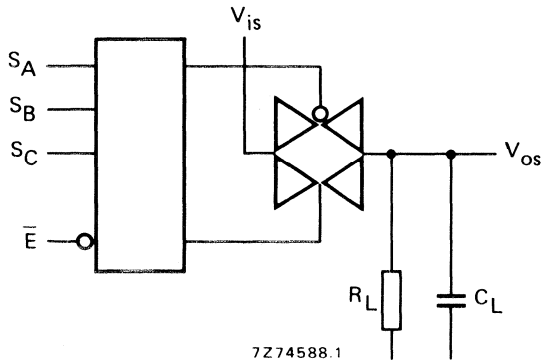


Fig. 8.

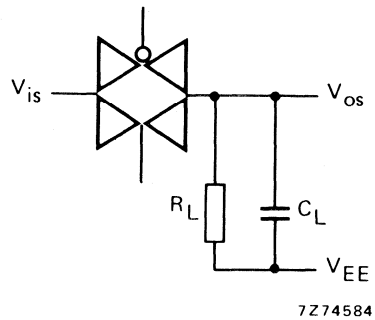


Fig. 9.

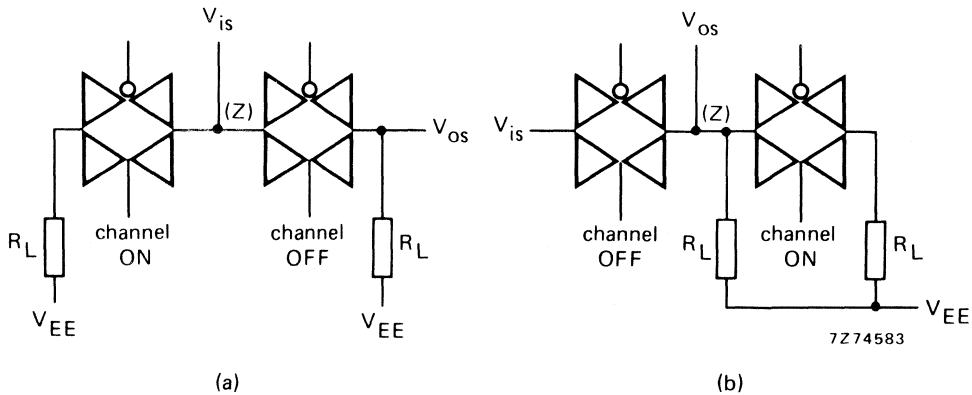


Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4053B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.

PROGRAMMABLE DIVIDE-BY-N COUNTER

The HEF4059B is a divide-by-n counter which can be programmed to divide an input frequency by any number *n* from 3 to 15 999. The output signal is a one clock-cycle wide pulse and occurs at a rate equal to the input frequency divided by *n*. The single output (O) has TTL drive capability. The down counter is preset by means of 16 jam inputs (J1 to J16); continued on next page.

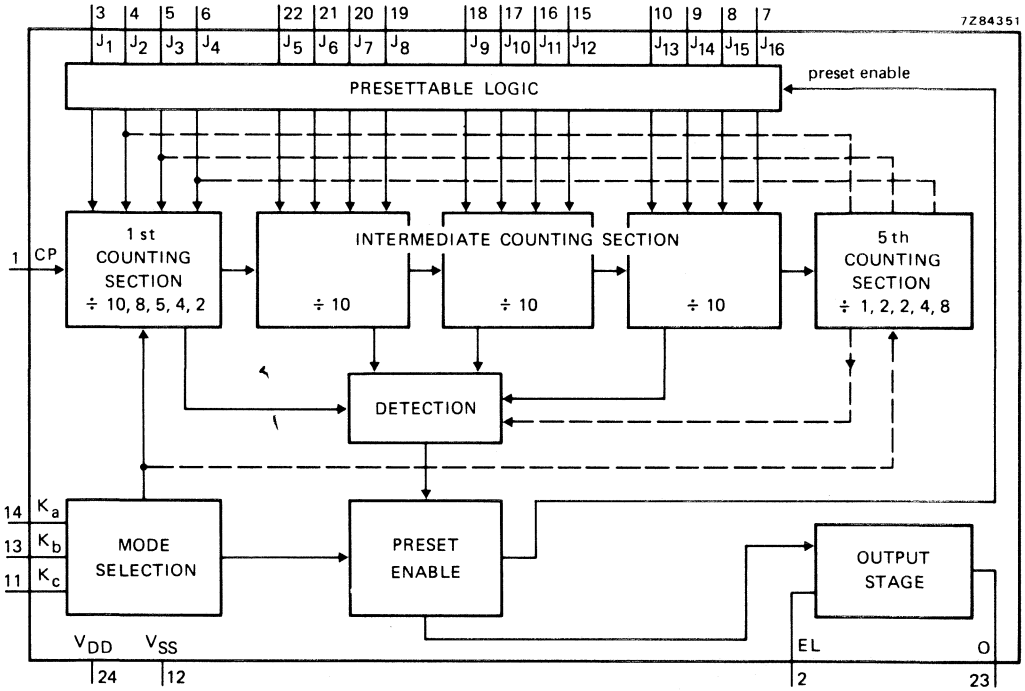


Fig. 1 Functional block diagram.

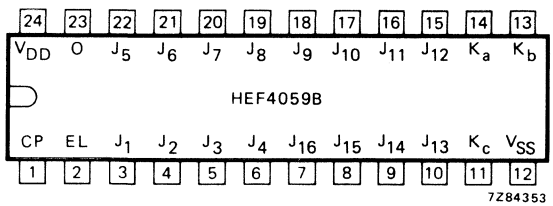


Fig. 2 Pinning diagram.

PINNING

CP	clock input
K_a, K_b, K_c	mode select inputs
J_1 to J_{16}	programmable jam inputs (BCD)
EL	latch enable input
O	divide-by-n output

HEF4059BP : 24-lead DIL; plastic (SOT-101A).
HEF4059BD: 24-lead DIL; ceramic (cerdip) (SOT-94).
HEF4059BT : 24-lead mini-pack; plastic (SO-24; SOT-137A).

FAMILY DATA

I_{DD} LIMITS catagory LSI

see Family Specifications

The three mode selection inputs K_a, K_b and K_c determine the modulus ('divide-by' number) of the first and last counting sections in accordance with Table 1.

Every time the first (fastest) counting section goes through one cycle, it reduces, by 1, the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section (which consists of flip-flops that are not needed for operating the first counting section).

For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last (5th) counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands.

This counting mode is selected when K_a, K_b and K_c are set to HIGH. In this case input J_1 is used to preset the first counting section and J_2 to J_4 are used to preset the last (5th) counting section.

If ÷ 10 mode is desired for the first section, K_a is set HIGH, K_b to HIGH and K_c to LOW. The jam inputs J_1 to J_4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters, presettable by means of the jam inputs J_5 to J_{16}.

When clock pulses are applied to the clock input after a number *n* has been preset into the counter, the counter counts down until the DETECTION circuit detects the zero state. At this time the PRESET ENABLE circuit is enabled to preset again the number *n* into the counter and to produce an output pulse.

The preset of the counter to a desired ÷ *n* is achieved as follows:

n = (MODE*) (1000 x decade 5 preset + 100 x decade 4 preset + 10 x decade 3 preset + 1 x decade 2 preset) + decade 1 preset.

* MODE = first counting section divider (10, 8, 5, 4 or 2).

To calculate preset values for any *n* count, divide the *n* count by the selected mode. The resultant is the corresponding preset values of the 5th to the 2nd decade with the remainder being equal to the 1st decade value.

$$\text{preset value} = \frac{n}{\text{mode}}.$$

If *n* = 8479, and the selected mode = 5, the preset value = 8479 ÷ 5 = 1695 with a remainder of 4, thus the jam inputs must be set as follows:

4			1	5				9				6			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L

The mode select inputs permit frequency-synthesizer channel separations of 10, 12,5, 20, 25 and 50 parts. These inputs set the maximum value of *n* at 9999 (when the first counting section divides by 5 or 10) or at 15 999 (when the first counting section divides by 8, 4 or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9. In this case the first cycle of a counter consists of 15 count pulses, the next cycles consisting of 10 count pulses. Thus the place value of the three decades are still 1, 10 and 100. For example, in the ÷ 8 mode, the number from which the intermediate counting section begins to count-down can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
	1665

The last counting section can be preset to a maximum of 1, with a place value of 1000. The total of these numbers (2665) times 8 equals 21 320. The first counting section can be preset to a maximum of 7. Therefore, 21 327 is the maximum possible count in the ÷ 8 mode. The highest count of the various modes is shown in Table 1, in the column entitled 'extended counter range'. Control inputs K_b and K_c can be used to initiate and lock the counter in the 'master preset' mode. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that mode as long as K_b and K_c both remain LOW. The counter begins to run down from the preset state when a counting mode other than the 'master preset' mode is selected. Whenever the 'master preset' mode is used, control signals K_b = L and K_c = L must be applied for at least 3 full clock pulses. After the master preset mode inputs have been changed to one of the counting modes, the next positive-going clock transitition changes an internal flip-flop so that the count-down can begin at the second positive-going clock transition. Thus, after a 'master preset' mode, there is always one extra count before the output goes HIGH. Figure 3 illustrates the operation of the counter in mode ÷ 8 starting from the preset state 3.

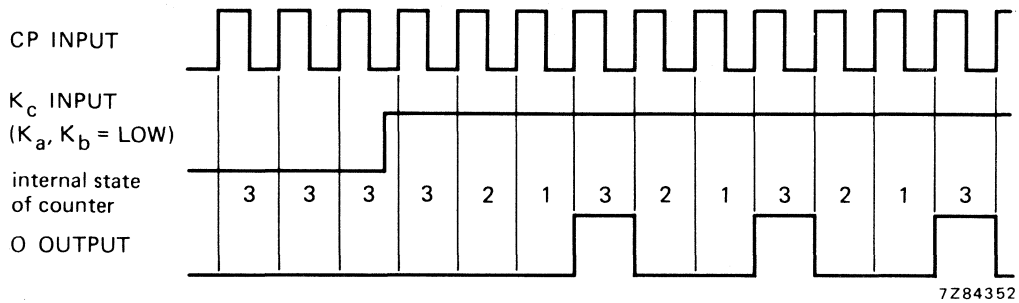


Fig. 3 Total count of 3.

If the 'master preset' mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the 'master preset' mode is not used the counter is preset in accordance with the 'jam inputs when the output pulse appears. A HIGH level at the latch enable input (EL) will cause the counter output to remain in the HIGH state until EL input returns to LOW. If the EL input is LOW, the output pulse will remain HIGH for only one cycle of the clock input signal.
When K_a = L, K_b = H, K_c = L and EL = L, the counter operates in the 'preset inhibit' mode, with which the dividend of the counter is fixed to 10 000, independent of the state of the jam inputs.
When in the same state of mode select inputs EL = H, the counter operates in the normal ÷ 10 mode, however, without the latch operation at the output.
Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

Table 1

latch enable input	mode select inputs			first counting section			last counting section			counter range	
EL	K_a	K_b	K_c	**MODE** divides by	max. preset state	jam inputs used	**MODE** divides by	max. preset state	jam inputs used	design max.	extended max.
X	H	H	H	2	1	J_1	8	7	$J_2J_3J_4$	15 999	17 331
X	L	H	H	4	3	J_1J_2	4	3	J_3J_4	15 999	18 663
X	H	L	H	5	4	$J_1J_2J_3$	2	1	J_4	9 999	13 329
X	L	L	H	8	7	$J_1J_2J_3$	2	1	J_4	15 999	21 327
X	H	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659
H	L	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659
L	L	H	L	preset inhibit			preset inhibit			fixed 10 000	–
X	X	L	L	master preset			master preset			–	–

D.C. CHARACTERISTICS V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C)			unit	
			−40 min.	+ 25 min.	+ 85 min.		
Output (sink) current LOW	4,75	I_{OL}	2,7	2,3	1,8	mA	V_O = 0,4 V; V_I = 0 or 4,75 V
	10		9,5	8	6,3	mA	V_O = 0,5 V; V_I = 0 or 10 V
	15		24	20	16	mA	V_O = 1,5 V; V_I = 0 or 15 V
Output (source) current HIGH	5	$-I_{OH}$	0,8	0,7	0,5	mA	V_O = 4,6 V; V_I = 0 or 5 V
	10		2,4	2	1,6	mA	V_O = 9,5 V; V_I = 0 or 10 V
	15		8,4	7	5,6	mA	V_O = 13,5 V; V_I = 0 or 15 V
Output (source) current HIGH	5	$-I_{OH}$	2,4	2	1,6	mA	V_O = 2,5 V; V_I = 0 or 5 V

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	
Dynamic power dissipation per package (P); n = 3	5	1 100 f_i + Σ($f_o C_L$) x V_{DD}^2	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5 500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	15 000 f_i + Σ($f_o C_L$) x V_{DD}^2	
n = 1000	5	500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	10	3 500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	9 000 f_i + Σ($f_o C_L$) x V_{DD}^2	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays	5			90	180	ns	78 ns + (0,25 ns/pF) C_L
CP → O	10	t_{PHL}		45	90	ns	40 ns + (0,10 ns/pF) C_L
HIGH to LOW	15			35	70	ns	32 ns + (0,07 ns/pF) C_L
	5			100	200	ns	76 ns + (0,48 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	40 ns + (0,20 ns/pF) C_L
	15			40	80	ns	33 ns + (0,15 ns/pF) C_L
Output transition times	5			30	60	ns	10 ns + (0,40 ns/pF) C_L
HIGH to LOW	10	t_{THL}		15	30	ns	6 ns + (0,18 ns/pF) C_L
	15			10	20	ns	4 ns + (0,13 ns/pF) C_L
	5			45	90	ns	10 ns + (0,70 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		25	50	ns	9 ns + (0,33 ns/pF) C_L
	15			16	32	ns	5 ns + (0,23 ns/pF) C_L
Maximum clock pulse frequency	5		3,5	7		MHz	
	10	f_{max}	7,5	15		MHz	
	15		10,0	20		MHz	

14-STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER AND OSCILLATOR

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (O_3 to O_9 and O_{11} to O_{13}) and an overriding asynchronous master reset input (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (O_3 to O_9 and O_{11} to O_{13} = LOW), independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

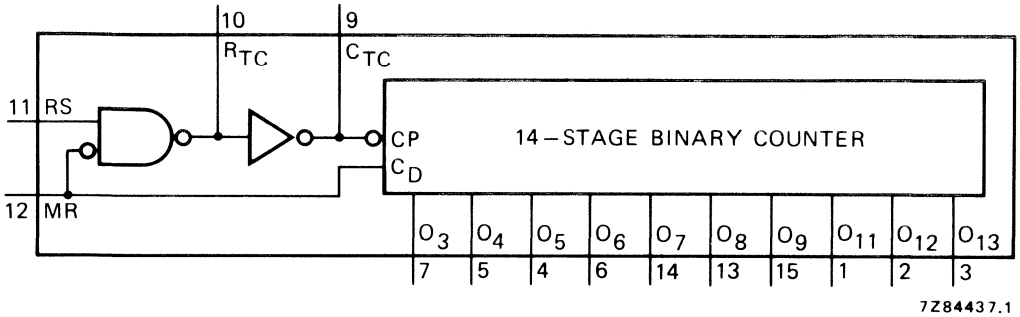


Fig. 1 Functional diagram.

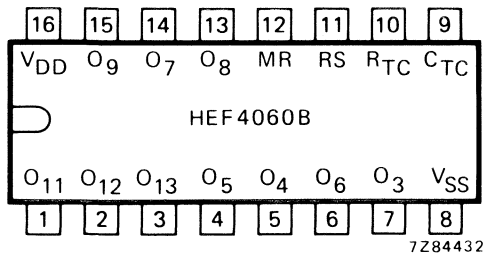


Fig. 2 Pinning diagram.

PINNING

MR	master reset
RS	clock input/oscillator pin
R_{TC}	oscillator pin
C_{TC}	external capacitor connection
O_3 to O_9, O_{11} to O_{13}	counter outputs

HEF4060BP : 16-lead DIL; plastic (SOT-38Z).
HEF4060BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4060BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI — see Family Specifications

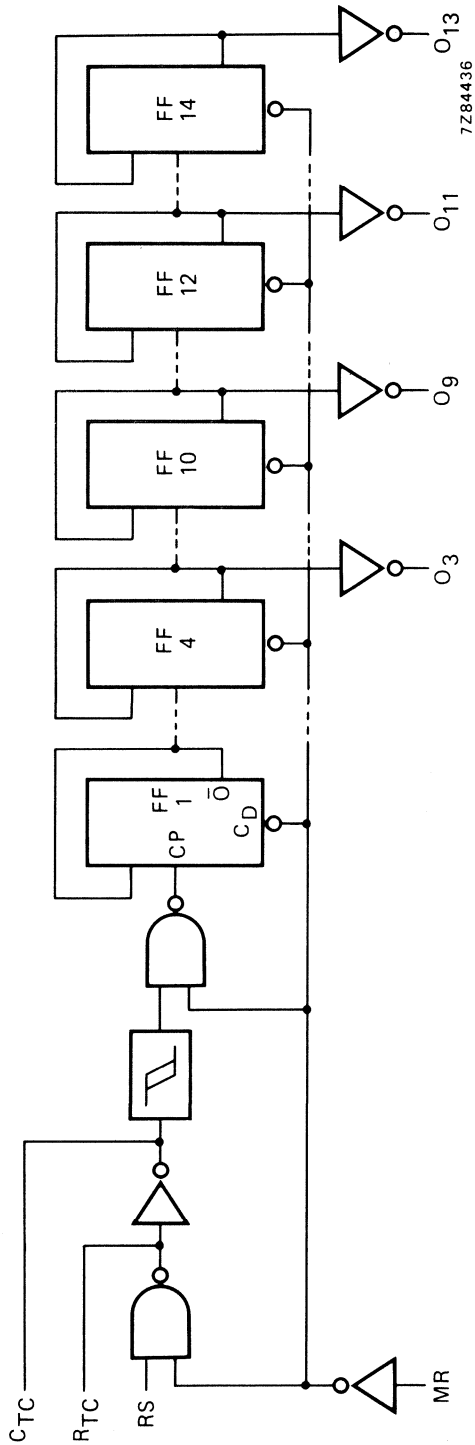


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
RS → O_3	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
O_n → O_{n+1}	5			25	50	ns	
HIGH to LOW	10	t_{PHL}		10	20	ns	
	15			6	12	ns	
	5			25	50	ns	
LOW to HIGH	10	t_{PLH}		10	20	ns	
	15			6	12	ns	
MR → O_n	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
times	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum clock pulse	5		120	60		ns	
width input RS	10	t_{WRSH}	50	25		ns	
HIGH	15		30	15		ns	
Minimum MR pulse	5		50	25		ns	
width; HIGH	10	t_{WMRH}	30	15		ns	
	15		20	10		ns	
Recovery time	5		160	80		ns	
for MR	10	t_{RMR}	80	40		ns	
	15		60	30		ns	
Maximum clock pulse	5		4	8		MHz	
frequency input RS	10	f_{max}	10	20		MHz	
	15		15	30		MHz	

A.C. CHARACTERISTICS

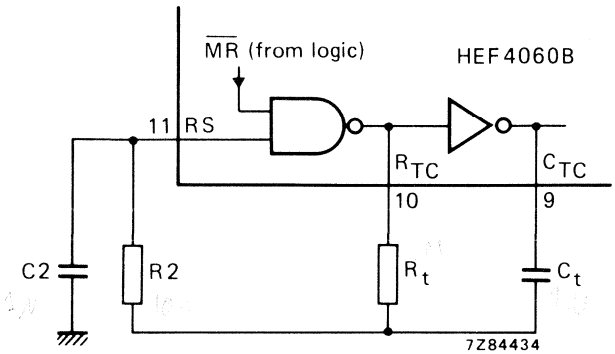
V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)*
Dynamic power dissipation per package (P)	5	$700\ f_i + f_o C_L V_{DD}^2$
	10	$3\,300\ f_i + f_o C_L V_{DD}^2$
	15	$8\,900\ f_i + f_o C_L V_{DD}^2$
Total power dissipation when using the on-chip oscillator (P)	5	$700\ f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 690\ V_{DD}$
	10	$3\,300\ f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 6\,900\ V_{DD}$
	15	$8\,900\ f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 22\,000\ V_{DD}$

* where:

f_i = input frequency (MHz)
f_o = output frequency (MHz)
C_L = load capacitance (pF)
V_{DD} = supply voltage (V)
C_t = timing capacitance (pF)
f_{osc} = oscillator frequency (MHz)

RC oscillator



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2{,}3 \times R_t \times C_t}$$

Fig. 4 External component connection for RC oscillator.

Timing component limitations

The oscillator frequency is mainly determined by R_tC_t, provided $R_t \ll R2$ and $R2C2 \ll R_tC_t$. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500 Ω at V_{DD} = 5 V, 300 Ω at V_{DD} = 10 V and 200 Ω at V_{DD} = 15 V.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t \geqslant 100$ pF, up to any practical value,
$10\ k\Omega \leqslant R_t \leqslant 1\ M\Omega$.

Typical crystal oscillator circuit

In Fig. 5, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.

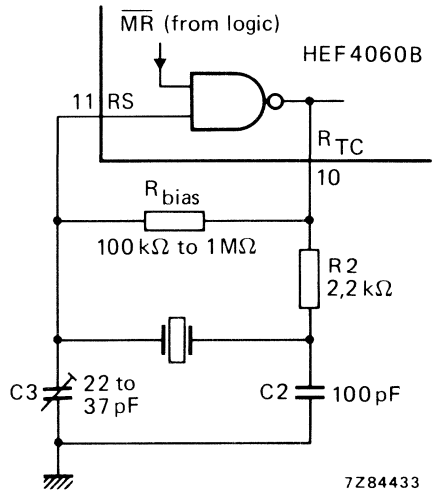


Fig. 5 External component connection for crystal oscillator.

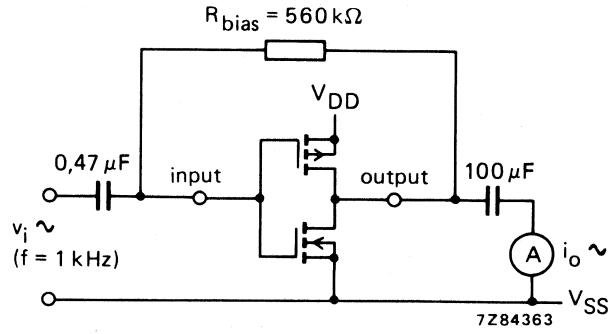
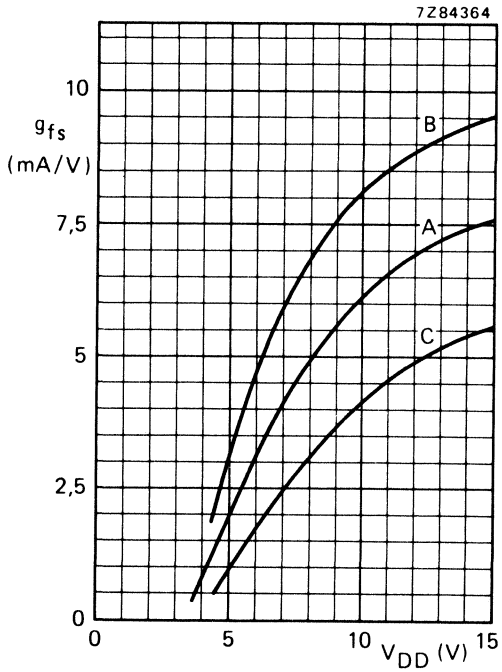


Fig. 6 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 7); MR = LOW.



Curves in Fig. 7:

A: average
B: average + 2 s,
C: average − 2 s, in where:
's' is the observed standard deviation.

Fig. 7 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

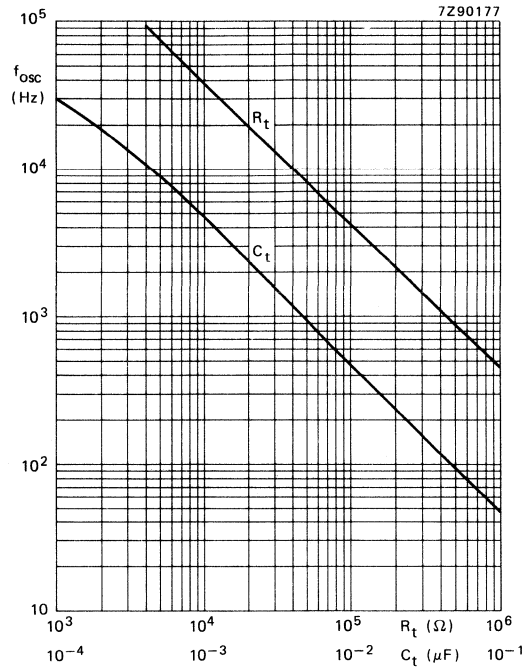


Fig. 8 RC oscillator frequency as a function of R_t and C_t at V_{DD} = 5 to 15 V; T_{amb} = 25 °C.
C_t curve at R_t = 100 kΩ; R2 = 470 kΩ.
R_t curve at C_t = 1 nF; R2 = 5 R_t.

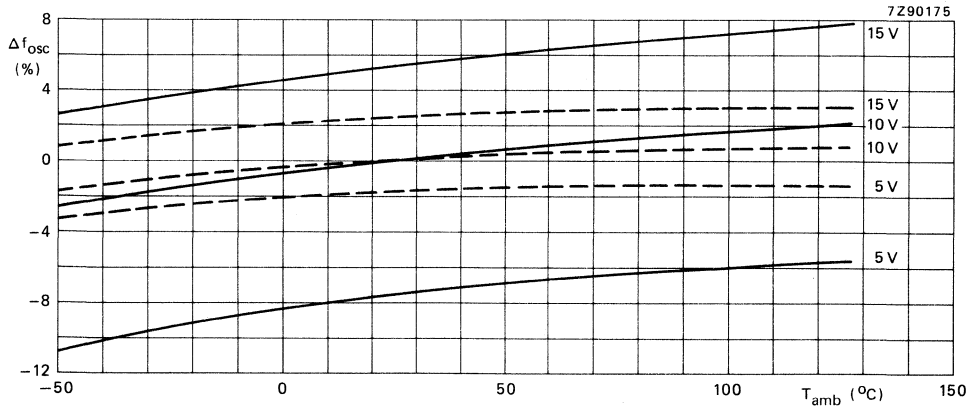


Fig. 9 Oscillator frequency deviation (Δf_{osc}) as a function of ambient temperature; referenced at: f_{osc} at T_{amb} = 25 °C and V_{DD} = 10 V.

——— R_t = 100 kΩ; C_t = 1 nF; R2 = 0.
– – – R_t = 100 kΩ; C_t = 1 nF; R2 = 300 kΩ.

QUADRUPLE BILATERAL SWITCHES

The HEF4066B has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is disabled and a high impedance between Y and Z is established (OFF condition).

The HEF4066B is pin compatible with the HEF4016B but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.

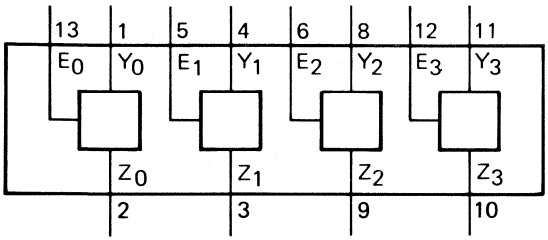


Fig. 1 Functional diagram.

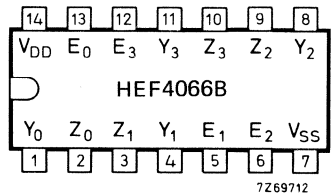


Fig. 2 Pinning diagram.

PINNING

E_0 to E_3 enable inputs

Y_0 to Y_3 input/output terminals

Z_0 to Z_3 input/output terminals

HEF4066BP : 14-lead DIL; plastic (SOT-27).
HEF4066BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4066BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

APPLICATION INFORMATION

An example of application for the HEF4066B is:

- Analogue and digital switching

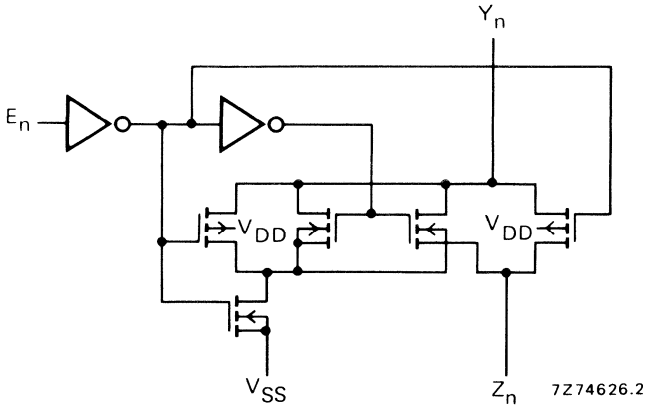


Fig. 3 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch — P max. 100 mW

For other RATINGS see Family Specifications

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	V_{DD} V	symbol	min.	typ.	max.		conditions
ON resistance	5	R_{ON}	–	350	2500	Ω	E_n at V_{DD}; V_{is} = V_{SS} to V_{DD}; see Fig. 4
	10		–	80	245	Ω	
	15		–	60	175	Ω	
ON resistance	5	R_{ON}	–	115	340	Ω	E_n at V_{DD}; V_{is} = V_{SS}; see Fig. 4
	10		–	50	160	Ω	
	15		–	40	115	Ω	
ON resistance	5	R_{ON}	–	120	365	Ω	E_n at V_{DD}; V_{is} = V_{DD}; see Fig. 4
	10		–	65	200	Ω	
	15		–	50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	–	25	–	Ω	E_n at V_{DD}; V_{is} = V_{SS} to V_{DD}; see Fig. 4
	10		–	10	–	Ω	
	15		–	5	–	Ω	
OFF state leakage current, any channel OFF	5	I_{OZ}	–	–	–	nA	E_n at V_{SS}
	10		–	–	–	nA	
	15		–	–	200	nA	
E_n input voltage LOW	5	V_{IL}	–	2,25	1	V	I_{is} = 10 μA; see Fig. 9
	10		–	4,50	2	V	
	15		–	6,75	2	V	

	V_{DD} V	symbol	T_{amb} (°C) −40 max.	+ 25 max.	+ 85 max.		conditions
Quiescent device current	5	I_{DD}	1,0	1,0	7,5	μA	V_{SS} = 0; all valid input combinations; V_I = V_{SS} or V_{DD}
	10		2,0	2,0	15,0	μA	
	15		4,0	4,0	30,0	μA	
Input leakage current at E_n	15	$\pm I_{IN}$	–	300	1000	nA	E_n at V_{SS} or V_{DD}

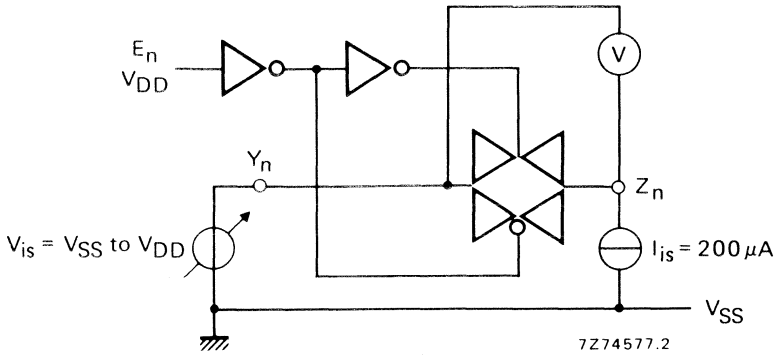


Fig. 4 Test set-up for measuring R_{ON}.

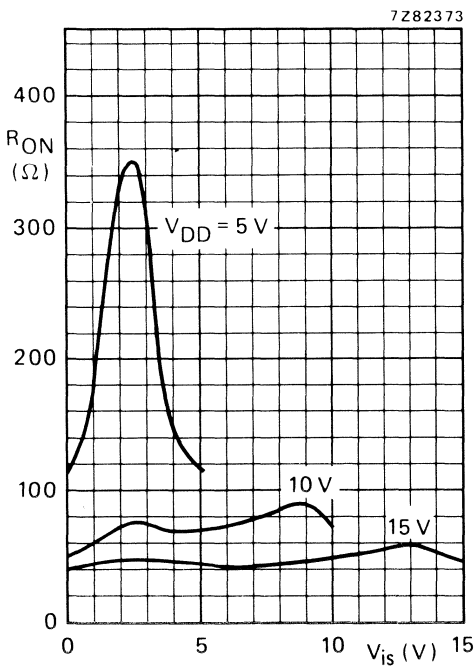


Fig. 5 Typical R_{ON} as a function of input voltage.

E_n at V_{DD}
I_{is} = 200 μA
V_{SS} = 0 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS}.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		10	20	ns	
HIGH to LOW	10	t_{PHL}	5	10	ns	note 1
	15		5	10	ns	
	5		10	20	ns	
LOW to HIGH	10	t_{PLH}	5	10	ns	note 1
	15		5	10	ns	
Output disable times						
$E_n \rightarrow V_{os}$	5		80	160	ns	
HIGH	10	t_{PHZ}	65	130	ns	note 2
	15		60	120	ns	
	5		80	160	ns	
LOW	10	t_{PLZ}	70	140	ns	note 2
	15		70	140	ns	
Output enable times						
$E_n \rightarrow V_{os}$	5		40	80	ns	
HIGH	10	t_{PZH}	20	40	ns	note 2
	15		15	30	ns	
	5		45	90	ns	
LOW	10	t_{PZL}	20	40	ns	note 2
	15		15	30	ns	
Distortion, sine-wave	5		0,25		%	
response	10		0,04		%	note 3
	15		0,04		%	
Crosstalk between	5		–		MHz	
any two channels	10		1		MHz	note 4
	15		–		MHz	
Crosstalk; enable	5		–		mV	
input to output	10		50		mV	note 5
	15		–		mV	
OFF-state	5		–		MHz	
feed-through	10		1		MHz	note 6
	15		–		MHz	
ON-state frequency	5		–		MHz	
response	10		90		MHz	note 7
	15		–		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; E_n = V_{DD}; V_{is} = V_{DD} (square-wave); see Figs 6 and 10.
2. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; E_n = V_{DD} (square-wave);
   V_{is} = V_{DD} and R_L to V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} = V_{SS} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Figs 6 and 11.
3. R_L = 10 kΩ; C_L = 15 pF; E_n = V_{DD}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   f_{is} = 1 kHz; see Fig. 7.
4. R_L = 1 kΩ; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}\,(B)}{V_{is}\,(A)}$ = −50 dB; E_n (A) = V_{SS}; E_n (B) = V_{DD}; see Fig. 8.
5. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; E_n = V_{DD} (square-wave); crosstalk is $|V_{os}|$ (peak value);
   see Fig. 6.
6. R_L = 1 kΩ; C_L = 5 pF; E_n = V_{SS}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}}$ = −50 dB; see Fig. 7.
7. R_L = 1 kΩ; C_L = 5 pF; E_n = V_{DD}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}}$ = −3 dB; see Fig. 7.

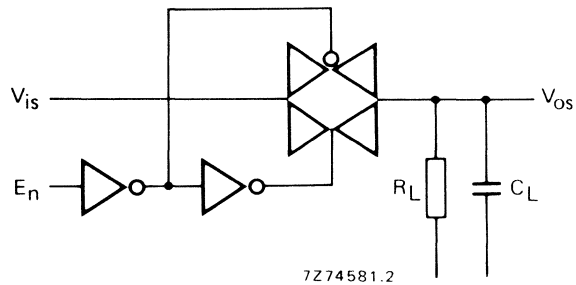


Fig. 6.

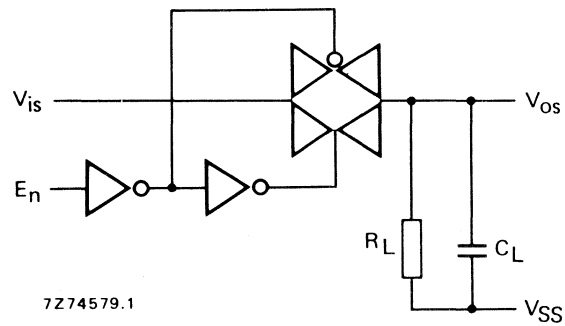


Fig. 7.

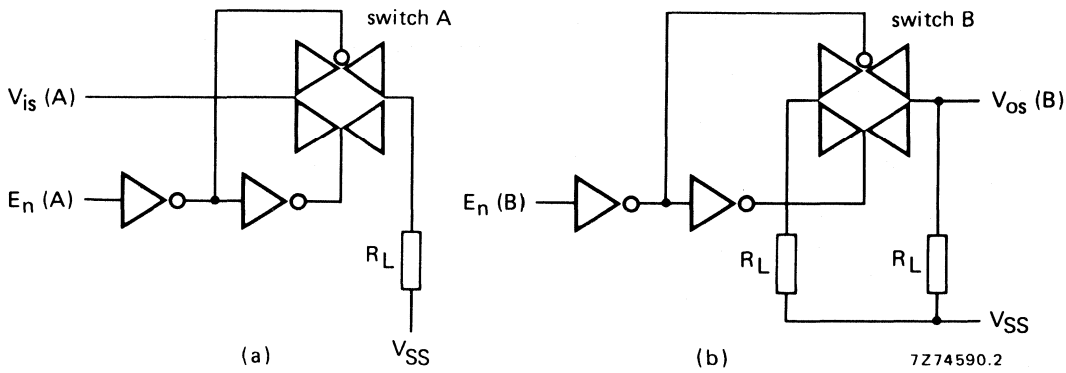

switch A
V_{is} (A)
E_n (A)
R_L
(a)
V_{SS}
switch B
V_{os} (B)
E_n (B)
R_L
R_L
V_{SS}
(b)
7Z74590.2

Fig. 8.

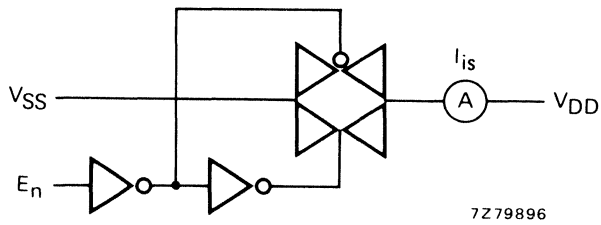

I_{is}
V_{SS}
A
V_{DD}
E_n
7Z79896

Fig. 9.

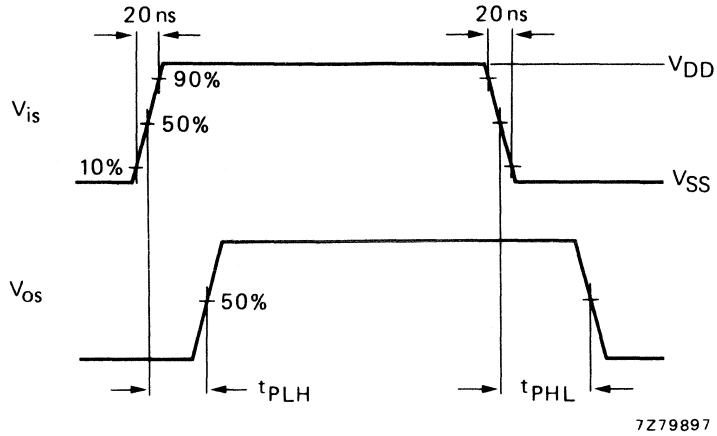
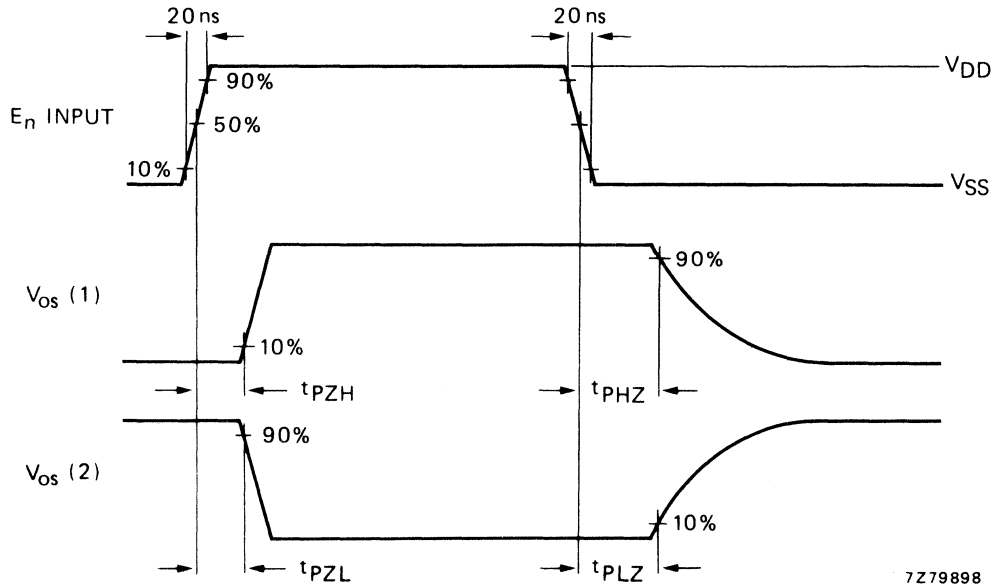


Fig. 10 Waveforms showing propagation delays from V_{is} to V_{os}.



(1) V_{is} at V_{DD}; (2) V_{is} at V_{SS}.

Fig. 11 Waveforms showing output disable and enable times.

16-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4067B is a 16-channel analogue multiplexer/demultiplexer with four address inputs (A_0 to A_3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The device contains sixteen bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to the common input/output (Z).

With $\overline{E}$ LOW, one of the sixteen switches is selected (low impedance ON-state) by A_0 to A_3. All unselected switches are in the high impedance OFF-state. With $\overline{E}$ HIGH all switches are in the high impedance OFF-state, independent of A_0 to A_3.

The analogue inputs/outputs (Y_0 to Y_{15} and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 15 V.

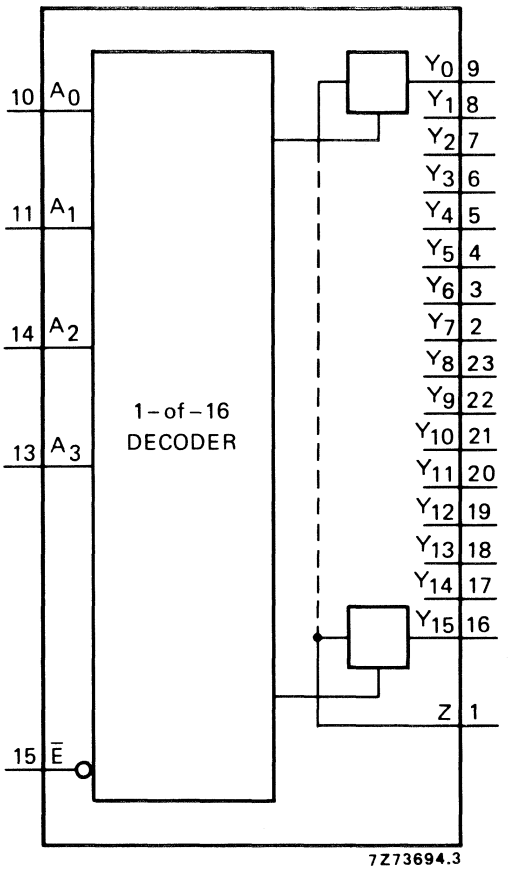


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

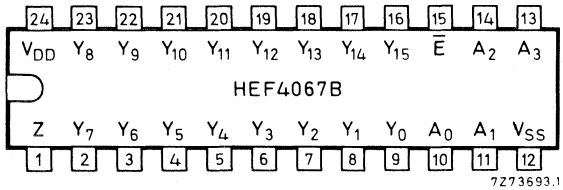


Fig. 2 Pinning diagram.

HEF4067BP : 24-lead DIL; plastic (SOT-101A).
HEF4067BD: 24-lead DIL; ceramic (cerdip) (SOT-94).
HEF4067BT : 24-lead mini-pack;plastic (SO-24; SOT-137A).

PINNING

Y_0 to Y_{15}	independent inputs/outputs
A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
Z	common input/output

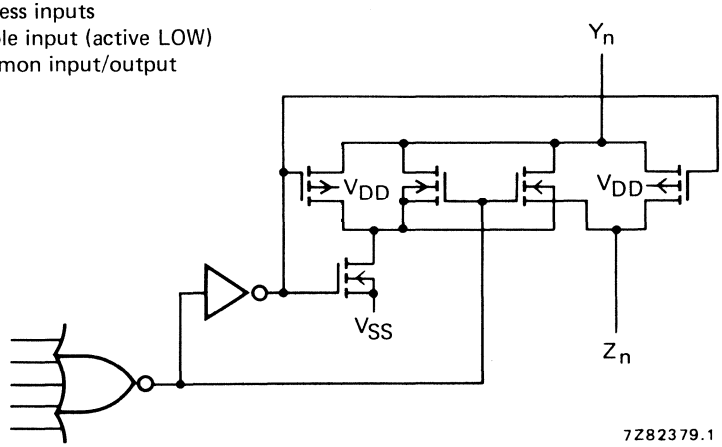


Fig. 3 Schematic diagram (one switch).

FUNCTION TABLE

inputs					channel
$\overline{E}$	A_3	A_2	A_1	A_0	ON
L	L	L	L	L	$Y_0 - Z$
L	L	L	L	H	$Y_1 - Z$
L	L	L	H	L	$Y_2 - Z$
L	L	L	H	H	$Y_3 - Z$
L	L	H	L	L	$Y_4 - Z$
L	L	H	L	H	$Y_5 - Z$
L	L	H	H	L	$Y_6 - Z$
L	L	H	H	H	$Y_7 - Z$
L	H	L	L	L	$Y_8 - Z$
L	H	L	L	H	$Y_9 - Z$
L	H	L	H	L	$Y_{10} - Z$
L	H	L	H	H	$Y_{11} - Z$
L	H	H	L	L	$Y_{12} - Z$
L	H	H	L	H	$Y_{13} - Z$
L	H	H	H	L	$Y_{14} - Z$
L	H	H	H	H	$Y_{15} - Z$
H	X	X	X	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

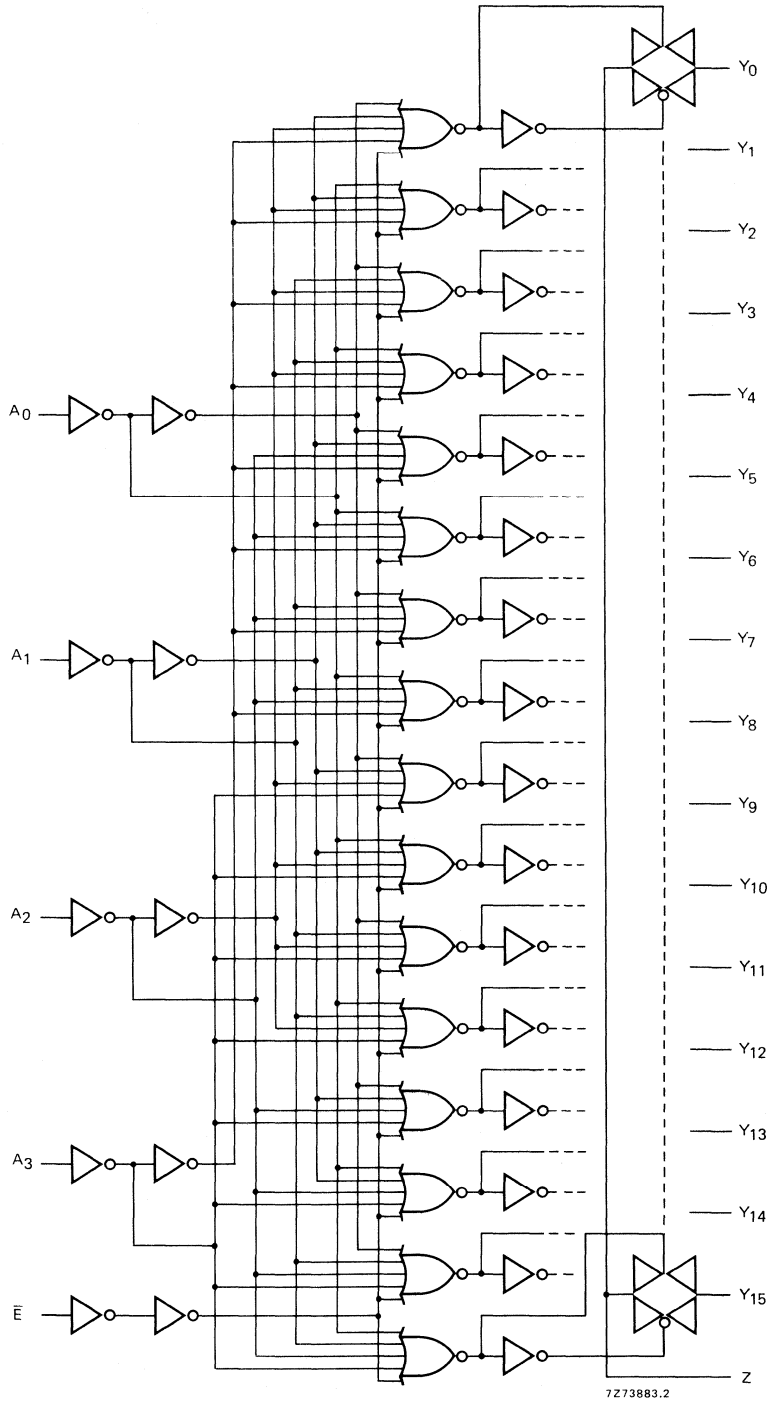


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	V_{DD} V	symbol	typ.	max.		conditions
ON resistance	5	R_{ON}	350	2500	Ω	V_{is} = V_{SS} to V_{DD} see Fig. 5
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_{is} = V_{SS} see Fig. 5
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_{is} = V_{DD} see Fig. 5
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	25	–	Ω	V_{is} = V_{SS} to V_{DD} see Fig. 5
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

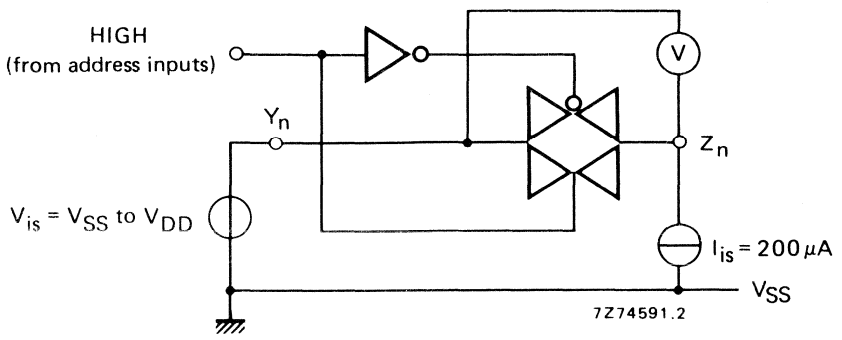


Fig. 5 Test set-up for measuring R_{ON}.

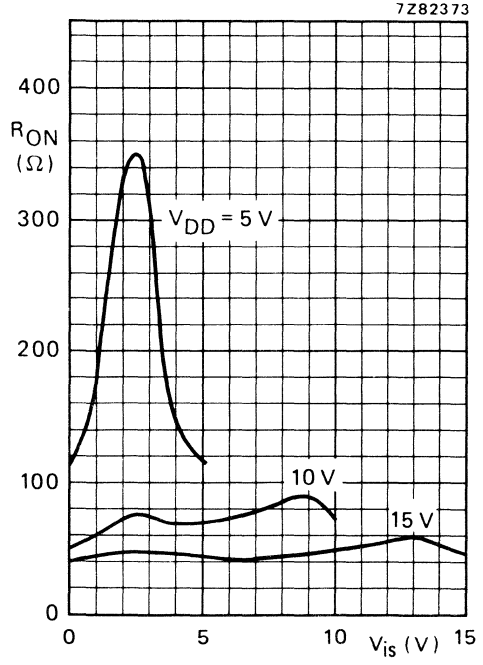


Fig. 6 Typical R_{ON} as a function of input voltage.
I_{is} = 200 μA
V_{SS} = 0 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS}.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\,300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		30	60	ns	
HIGH to LOW	10	t_{PHL}	15	25	ns	note 1
	15		10	20	ns	
	5		25	50	ns	
LOW to HIGH	10	t_{PLH}	10	20	ns	note 1
	15		10	20	ns	
$A_n \rightarrow V_{os}$	5		190	380	ns	
HIGH to LOW	10	t_{PHL}	70	145	ns	note 2
	15		50	100	ns	
	5		175	345	ns	
LOW to HIGH	10	t_{PLH}	70	140	ns	note 2
	15		50	100	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$	5		195	385	ns	
HIGH	10	t_{PHZ}	140	280	ns	note 3
	15		130	260	ns	
	5		215	435	ns	
LOW	10	t_{PLZ}	180	355	ns	note 3
	15		170	340	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$	5		155	315	ns	
HIGH	10	t_{PZH}	70	135	ns	note 3
	15		50	100	ns	
	5		170	340	ns	
LOW	10	t_{PZL}	70	140	ns	note 3
	15		50	100	ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{SS}; V_{is} = V_{DD} (square-wave); see Fig. 7.
2. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{SS}; A_n = V_{DD} (square-wave); V_{is} = V_{DD} and R_L to V_{SS} for t_{PLH}; V_{is} = V_{SS} and R_L to V_{DD} for t_{PHL}; see Fig. 7.
3. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{DD} (square-wave);
   V_{is} = V_{DD} and R_L to V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} = V_{SS} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 7.
4. R_L = 10 kΩ; C_L = 15 pF; channel ON; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); f_{is} = 1 kHz; see Fig. 8.
5. R_L = 1 kΩ; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 9.
6. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; $\overline{E}$ or A_n = V_{DD} (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 7.
7. R_L = 1 kΩ; C_L = 5 pF; channel OFF; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 8.
8. R_L = 1 kΩ; C_L = 5 pF; channel ON; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 8.

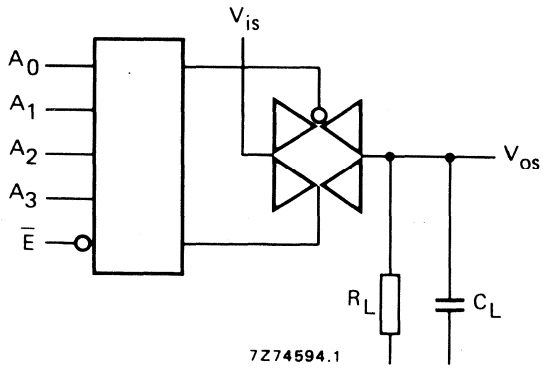


Fig. 7.

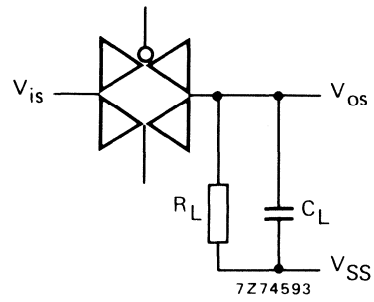


Fig. 8.

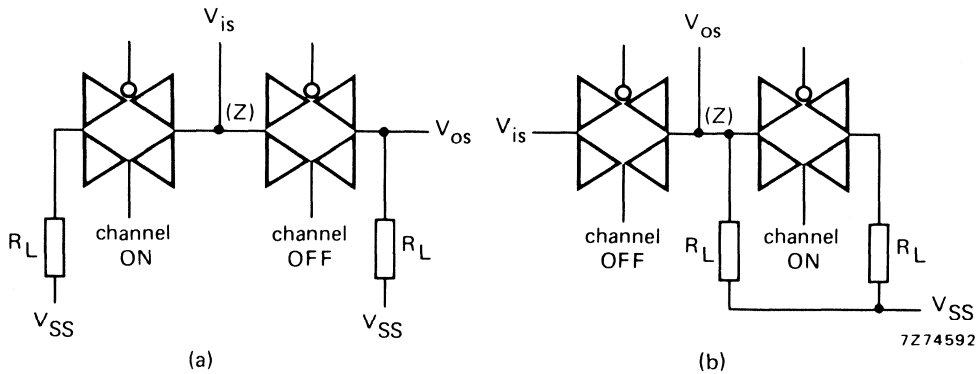


Fig. 9.

APPLICATION INFORMATION

Some examples of applications for the HEF4067B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.

8-INPUT NAND GATE

The HEF4068B provides the 8-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

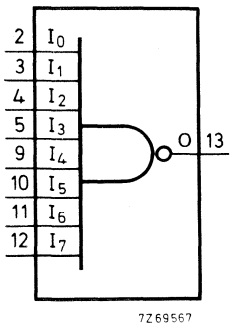


Fig. 1 Functional diagram.

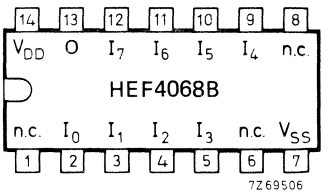


Fig. 2 Pinning diagram.

HEF4068BP : 14-lead DIL; plastic (SOT-27).
HEF4068BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4068BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

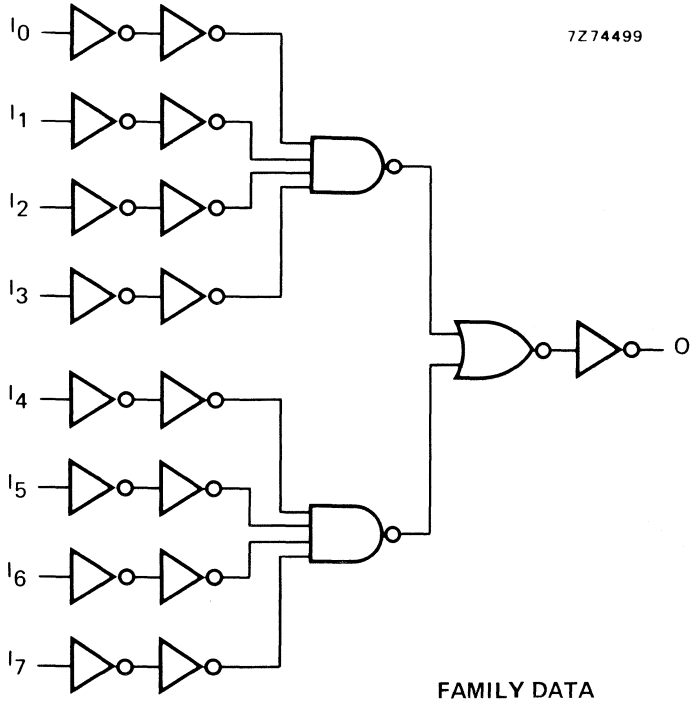


Fig. 3 Logic diagram.

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O$	5		95	195	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	40	85	ns	29 ns + (0,23 ns/pF) C_L
	15		30	65	ns	22 ns + (0,16 ns/pF) C_L
	5		80	165	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	700 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2900 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	7200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

HEX INVERTER

The HEF4069UB is a general purpose hex inverter. Each of the six inverters is a single stage.

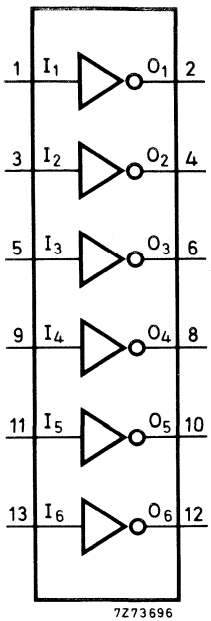


Fig. 1 Functional diagram.

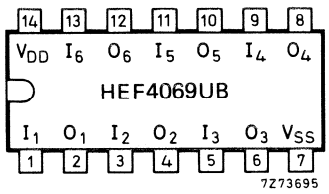


Fig. 2 Pinning diagram.

HEF4069UBP : 14-lead DIL; plastic (SOT-27).
HEF4069UBD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4069UBT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

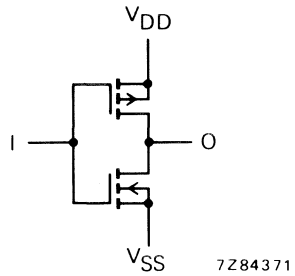


Fig. 3 Schematic diagram (one inverter).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications for V_{IH}/V_{IL} unbuffered stages

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.	typical extrapolation formula
Propagation delays	5		45	90 ns	18 ns + (0,55 ns/pF) C_L
$I_n \rightarrow O_n$	10	t_{PHL}	20	40 ns	9 ns + (0,23 ns/pF) C_L
HIGH to LOW	15		15	25 ns	7 ns + (0,16 ns/pF) C_L
	5		40	80 ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40 ns	9 ns + (0,23 ns/pF) C_L
	15		15	30 ns	7 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60 ns	9 ns + (0,42 ns/pF) C_L
	15		20	40 ns	6 ns + (0,28 ns/pF) C_L
	5		60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60 ns	9 ns + (0,42 ns/pF) C_L
	15		20	40 ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	600 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	22 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

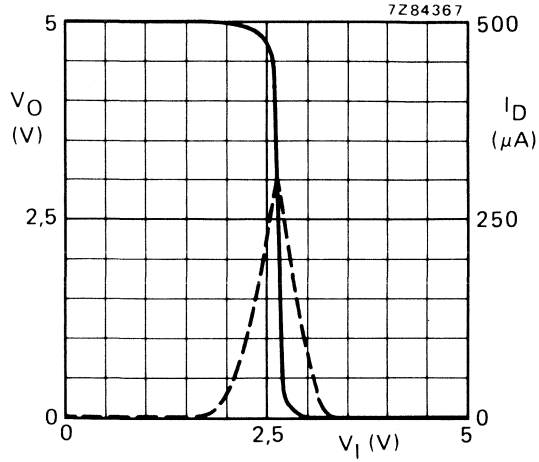


Fig. 4 Typical transfer characteristics; —— V_O; – – – I_D(drain current); $I_O = 0$; $V_{DD} = 5$ V.

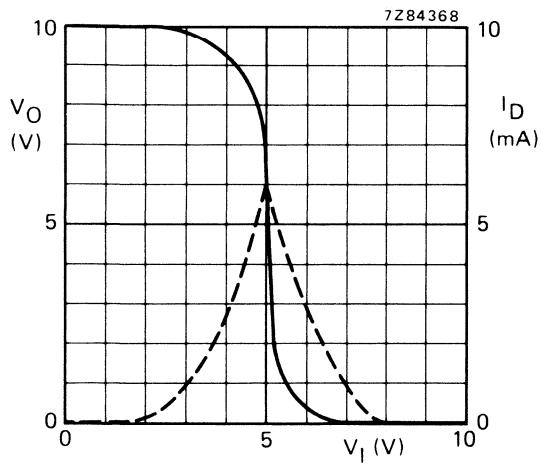


Fig. 5 Typical transfer characteristics; —— V_O; – – – I_D(drain current); $I_O = 0$; $V_{DD} = 10$ V.

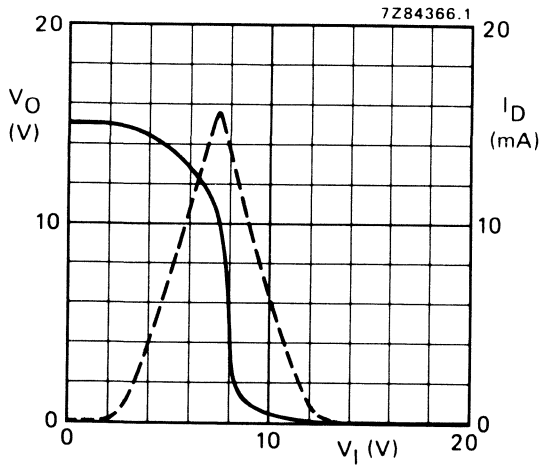
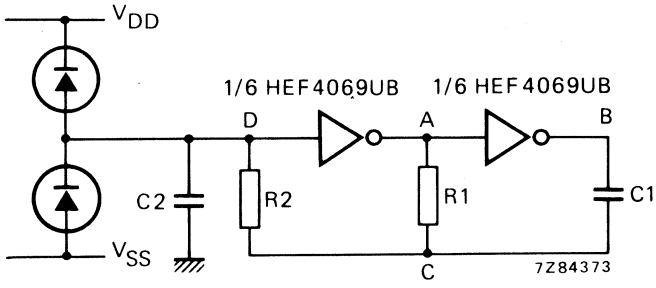


Fig. 6 Typical transfer characteristics; —— V_O; – – – I_D(drain current) $I_O = 0$; $V_{DD} = 15$ V.

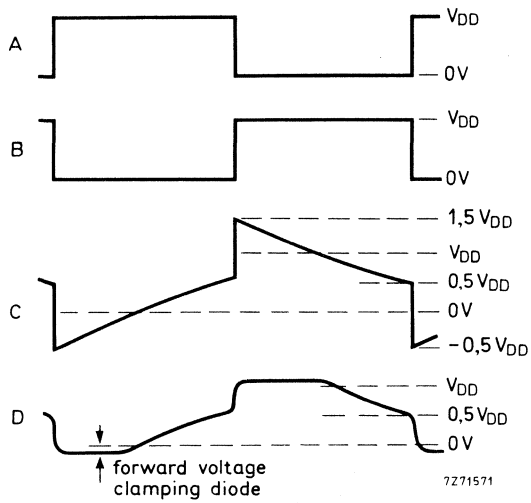
APPLICATION INFORMATION

Some examples of applications for the HEF4069UB are shown below.

In Fig. 7 an astable relaxation oscillator is given. The oscillation frequency is mainly determined by R1C1, provided R1 << R2 and R2C2 << R1C1.



(a)



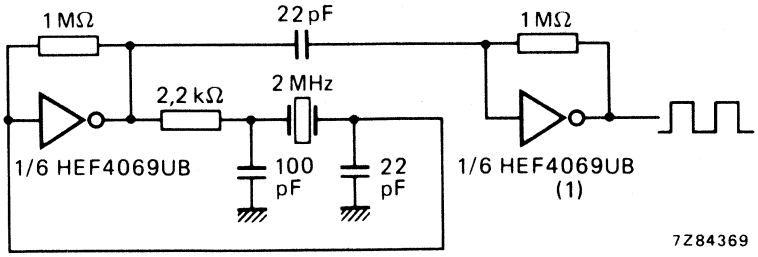
(b)

Fig. 7(a) Astable relaxation oscillator using two HEF4069UB inverters; the diodes may be BAW62; C2 is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \text{ and } T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \text{ where}$$

V_{ST} is the signal threshold level of the inverter. The period is fairly independent of V_{DD}, V_{ST} and temperature. The duty factor, however, is influenced by V_{ST}.



(1) This inverter is added to amplify the oscillator output voltage to a level sufficient to drive other LOCMOS circuits.

Fig. 8 Crystal oscillator for frequencies up to 10 MHz, using two HEF4069UB inverters.

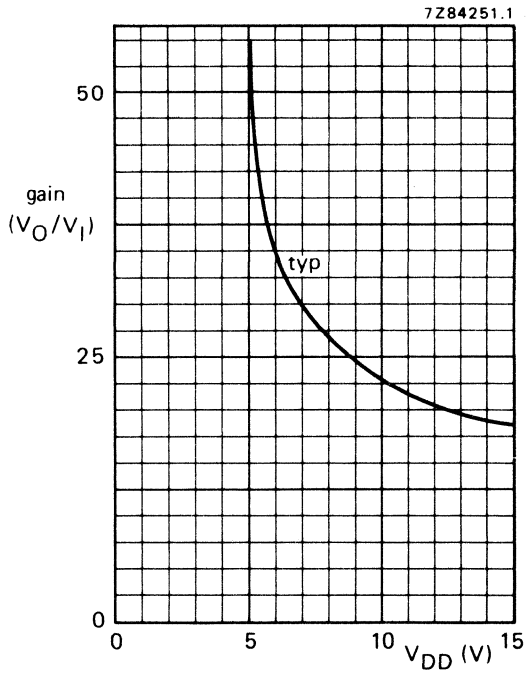


Fig. 9 Voltage gain (V_O/V_I) as a function of supply voltage.

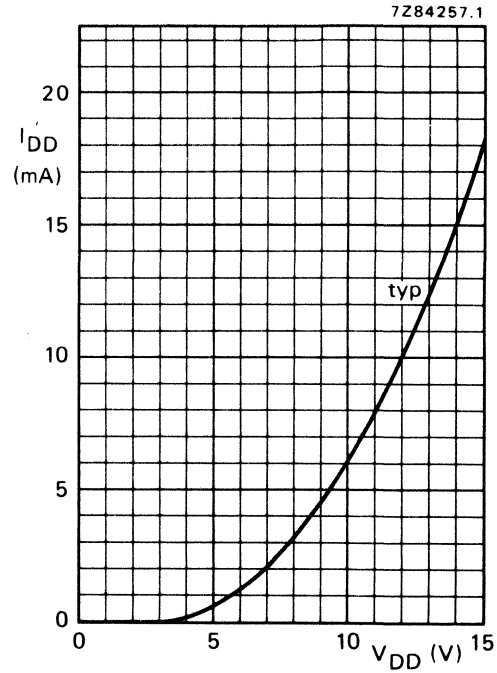


Fig. 10 Supply current as a function of supply voltage.

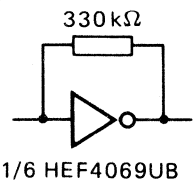


Fig. 11 Test set-up for measuring graphs of Figs 9 and 10.
It is also an example of an analogue amplifier using one HEF4069UB.

APPLICATION INFORMATION (continued)

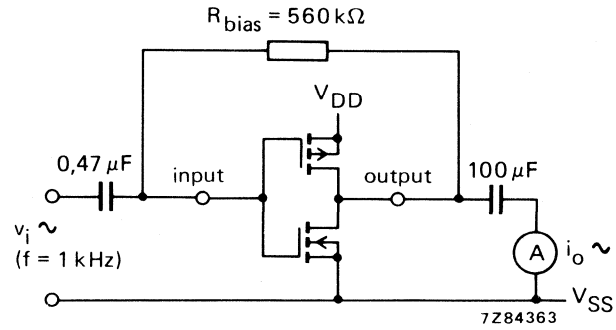
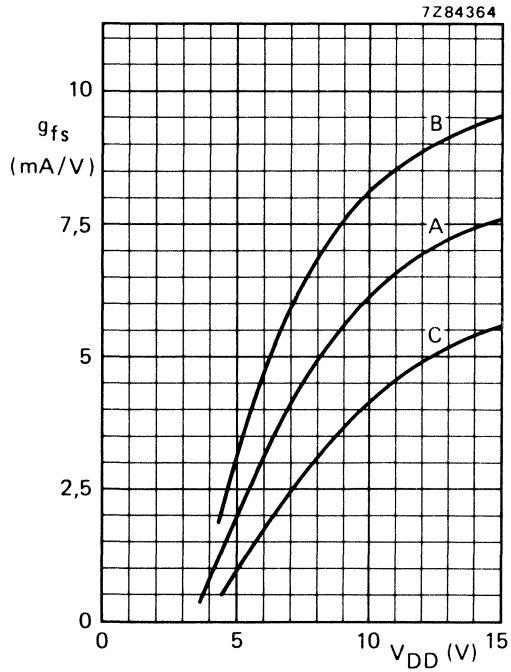


Fig. 12 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 13).



Curves in Fig. 13:

A : average,
B : average + 2 s,
C : average −2 s, in where:
's' is the observed standard deviation.

Fig. 13 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

QUADRUPLE EXCLUSIVE-OR GATE

The HEF4070B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

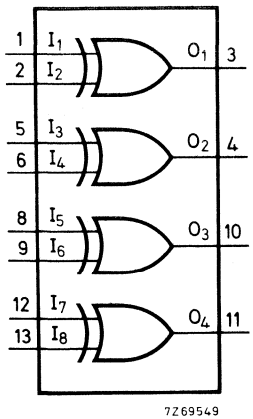


Fig. 1 Functional diagram.

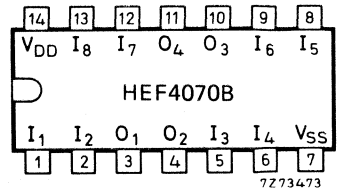


Fig. 2 Pinning diagram.

HEF4070BP : 14-lead DIL; plastic (SOT-27).
HEF4070BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4070BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

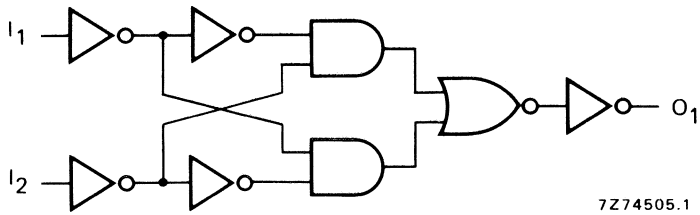


Fig. 3 Logic diagram (one gate).

APPLICATION INFORMATION

Some examples of applications for the HEF4070B are:

- Logical comparators
- Parity checkers and generators

TRUTH TABLE

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		85	175	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	75	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	21 ns + (0,16 ns/pF) C_L
	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	65	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$14\,400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT OR GATE

The HEF4071B is a positive logic quadruple 2-input OR gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

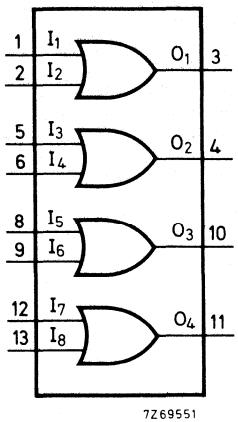


Fig. 1 Functional diagram.

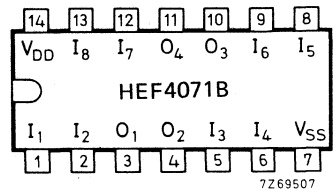


Fig. 2 Pinning diagram.

HEF4071BP : 14-lead DIL; plastic (SOT-27).
HEF4071BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4071BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

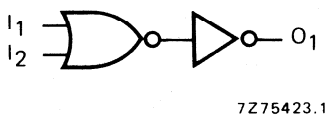


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transistion times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		55	115	ns	28 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	15 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L
	5		45	90	ns	18 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	45	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1150\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$19\ 700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

DUAL 4-INPUT OR GATE

The HEF4072B provides the positive dual 4-input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

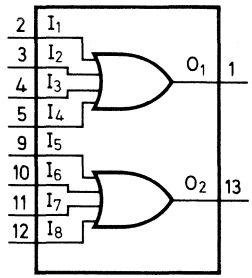


Fig. 1 Functional diagram.

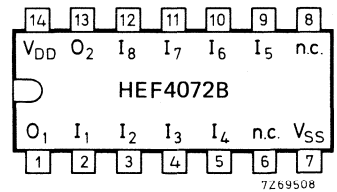


Fig. 2 Pinning diagram.

HEF4072BP : 14-lead DIL; plastic (SOT-27).
HEF4072BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4072BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

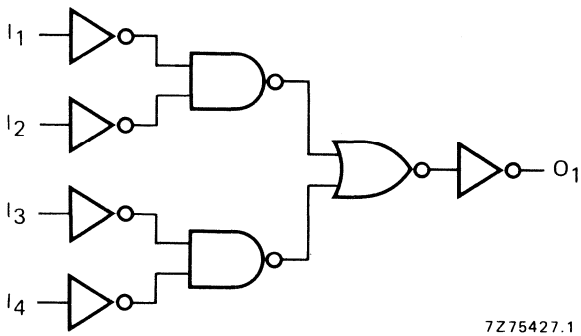


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		80	155	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	55	ns	17 ns + (0,16 ns/pF) C_L
	5		75	145	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	55	ns	17 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	950 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4500 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	13 700 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

TRIPLE 3-INPUT AND GATE

The HEF4073B provides the positive triple 3-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

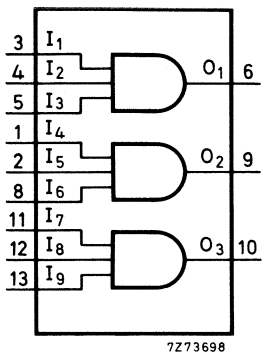


Fig.1 Functional diagram.

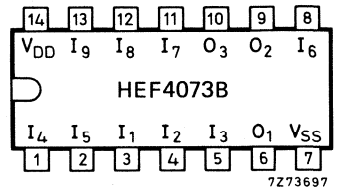


Fig.2 Pinning diagram.

HEF4073BP : 14-lead DIL; plastic (SOT-27).
HEF4073BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4073BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

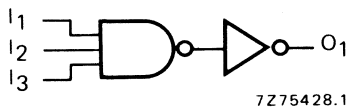


Fig.3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		55	110	ns	23 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		45	90	ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	600 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2700 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	8400 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

TRIPLE 3-INPUT OR GATE

The HEF4075B provides the positive triple 3-input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

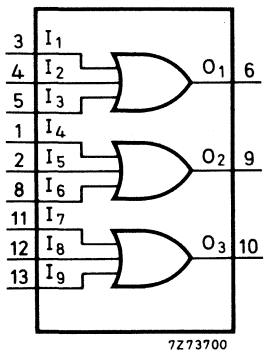


Fig.1 Functional diagram.

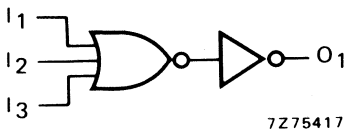


Fig.3 Logic diagram (one gate).

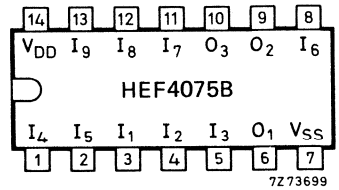


Fig.2 Pinning diagram.

HEF4075BP : 14-lead DIL; plastic (SOT-27).
HEF4075BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4075BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

Products approved to CECC 90 104-050.

A.C. CHARACTERISTICS

V_{SS}= 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays	5		65	130	ns	38 ns + (0,55 ns/pF) C_L
$I_n \rightarrow O_n$	10	t_{PHL}	30	60	ns	19 ns + (0,23 ns/pF) C_L
HIGH to LOW	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		65	130	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	750 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	3 600 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	11 200 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE D-TYPE REGISTER WITH 3-STATE OUTPUTS

The HEF4076B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), two active LOW data enable inputs ($\overline{ED}_0$ and $\overline{ED}_1$), a common clock input (CP), four 3-state outputs (O_0 to O_3), two active LOW output enable inputs ($\overline{EO}_0$ and $\overline{EO}_1$), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is stored in the four flip-flops on the LOW to HIGH transition of CP if both $\overline{ED}_0$ and $\overline{ED}_1$ are LOW. A HIGH on either $\overline{ED}_0$ or $\overline{ED}_1$ prevents the flip-flops from changing on the LOW to HIGH transition of CP, independent of the information on D_0 to D_3. When both $\overline{EO}_0$ and $\overline{EO}_1$ are LOW, the contents of the four flip-flops are available at O_0 to O_3. A HIGH on either $\overline{EO}_0$ or $\overline{EO}_1$ forces O_0 to O_3 into the high impedance OFF-state. A HIGH on MR resets all four flip-flops, independent of all other input conditions.

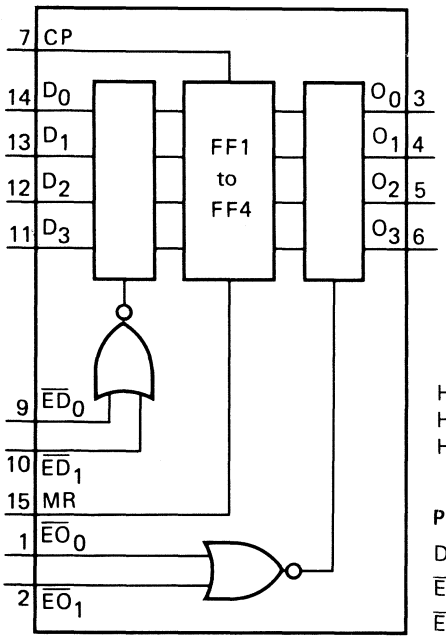


Fig. 1 Functional diagram.

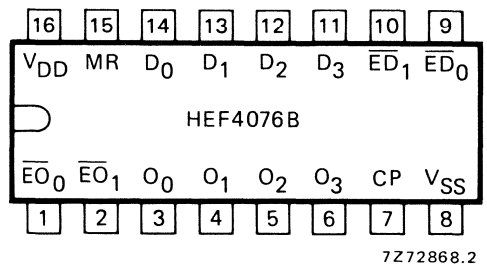


Fig. 2 Pinning diagram.

HEF4076BP : 16-lead DIL; plastic (SOT-38Z).
HEF4076BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4076BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_0 to D_3	data inputs
$\overline{ED}_0$, $\overline{ED}_1$	data enable inputs (active LOW)
$\overline{EO}_0$, $\overline{EO}_1$	output enable inputs (active LOW)
CP	clock input (LOW to HIGH, edge-triggered)
MR	master reset input
O_0 to O_3	data outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

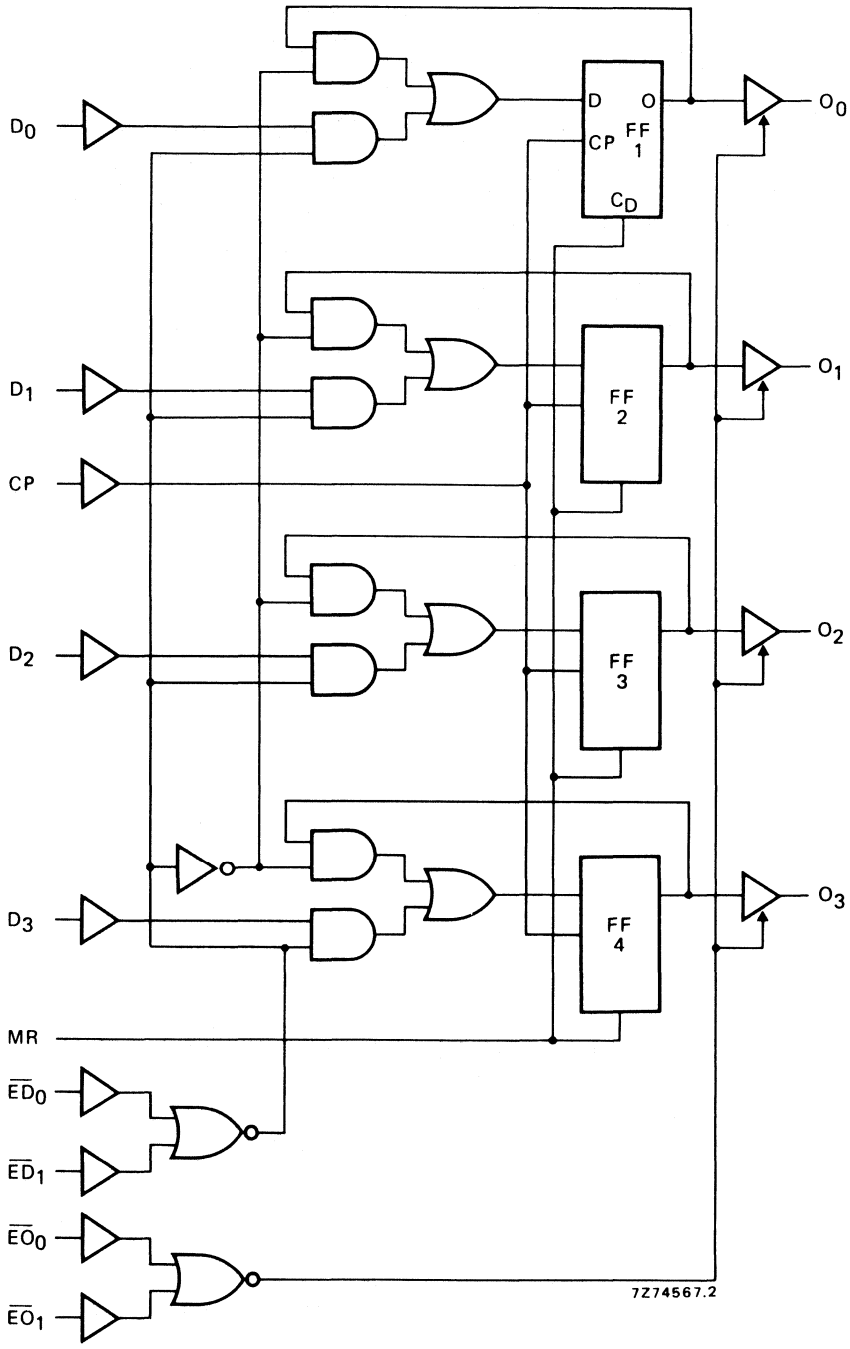


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs					outputs
MR	CP	$\overline{ED}_0$	$\overline{ED}_1$	D_n	O_n
H	X	X	X	X	L
L	∫	H	X	X	no change
L	∫	X	H	X	no change
L	∫	L	L	H	H
L	∫	L	L	L	L
L	⌡	X	X	X	no change

$\overline{EO}_0 = \overline{EO}_1$ = LOW

When either $\overline{EO}_0$ or $\overline{EO}_1$ is HIGH, the outputs are disabled (high impedance OFF-state).
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌡ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP → O_n	5			150	305 ns	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	85 ns	37 ns + (0,16 ns/pF) C_L
	5			160	320 ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
MR → O_n	5			95	190 ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85 ns	29 ns + (0,23 ns/pF) C_L
	15			30	65 ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays						
Output disable times	5			50	105 ns	
$\overline{EO}_n$ → O_n	10	t_{PHZ}		35	70 ns	
HIGH	15			30	65 ns	
	5			45	90 ns	
LOW	10	t_{PLZ}		30	65 ns	
	15			30	60 ns	
Output enable times	5			65	130 ns	
$\overline{EO}_n$ → O_n	10	t_{PZH}		30	55 ns	
HIGH	15			20	40 ns	
	5			60	120 ns	
LOW	10	t_{PZL}		25	50 ns	
	15			20	35 ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Set-up times	5		10	−15		ns	
$D_n \rightarrow CP$	10	t_{su}	0	−10		ns	
	15		0	−5		ns	
	5		0	−50		ns	
$\overline{ED}_n \rightarrow CP$	10	t_{su}	0	−20		ns	
	15		0	−15		ns	
Hold times	5		55	30		ns	
$D_n \rightarrow CP$	10	t_{hold}	20	10		ns	
	15		15	10		ns	
	5		25	−25		ns	
$\overline{ED}_n \rightarrow CP$	10	t_{hold}	10	−10		ns	
	15		5	−5		ns	see also waveforms Fig. 4
Minimum clock pulse width; LOW	5		120	60		ns	
	10	t_{WCPL}	45	20		ns	
	15		30	15		ns	
Minimum MR pulse width; HIGH	5		55	25		ns	
	10	t_{WMRH}	30	15		ns	
	15		20	10		ns	
Recovery time for MR	5		90	45		ns	
	10	t_{RMR}	35	15		ns	
	15		20	10		ns	
Maximum clock pulse frequency	5		4	8		MHz	
	10	f_{max}	11	22		MHz	
	15		16	32		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$9300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$24\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

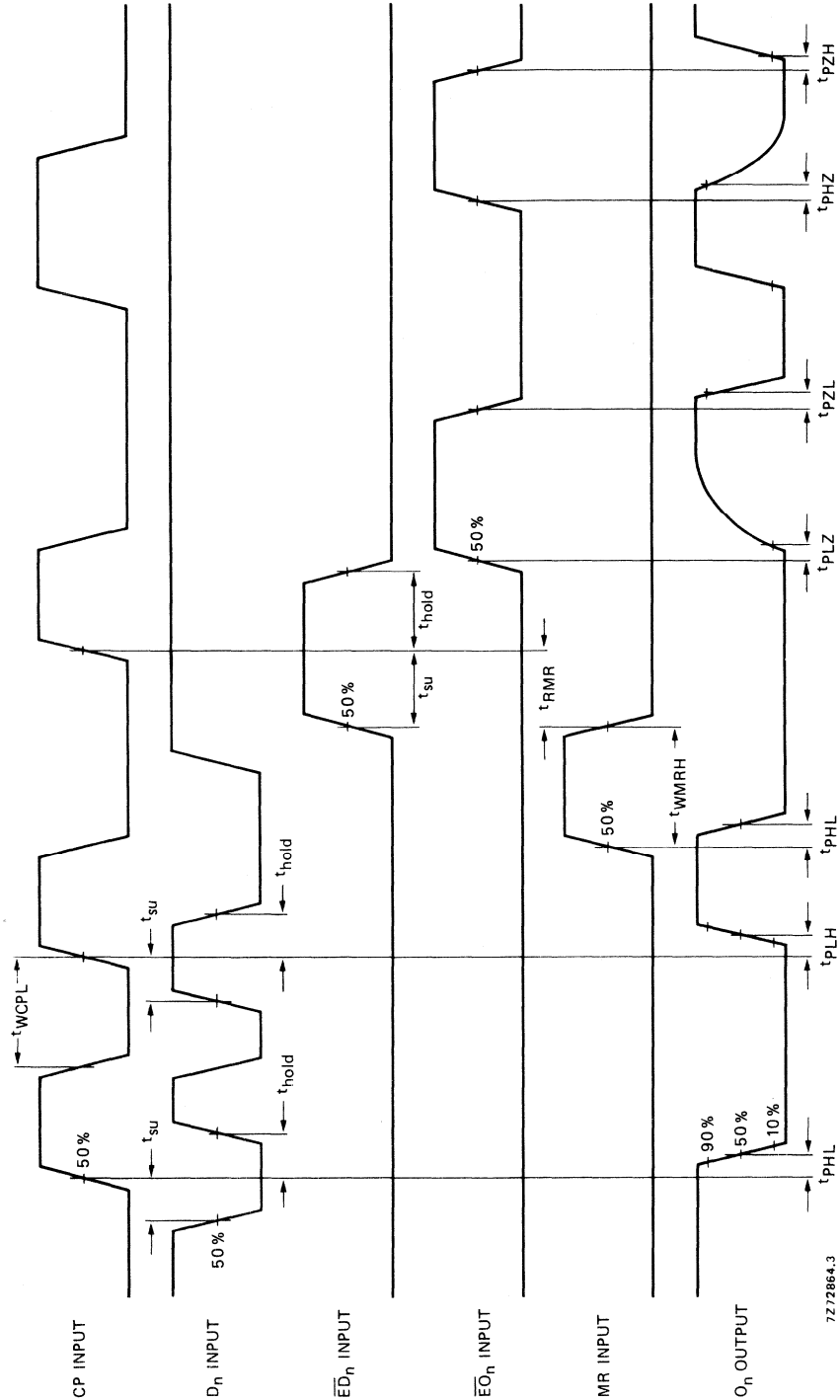


Fig. 4 Waveforms showing propagation delays, output disable/enable times, minimum CP and MR pulse widths, set-up and hold times for D_n to CP and $\overline{ED}_n$ to CP, and recovery time for MR. Set-up and hold times are shown as positive values but may be specified as negative values.

QUADRUPLE EXCLUSIVE-NOR GATE

The HEF4077B provides the exclusive-NOR function. The outputs are fully buffered for best performance.

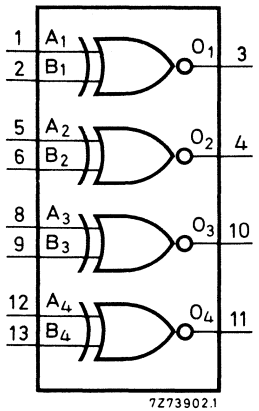


Fig. 1 Functional diagram.

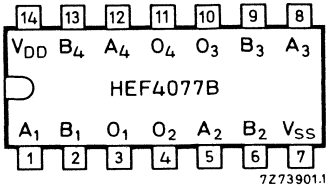


Fig. 2 Pinning diagram.

HEF4077BP : 14-lead DIL; plastic (SOT-27).
HEF4077BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4077BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

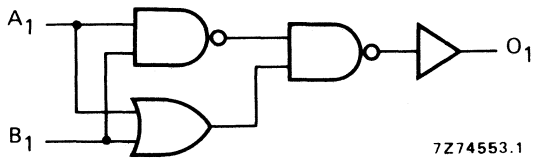


Fig. 3 Logic diagram (one gate).

TRUTH TABLE

A_n	B_n	O_n
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
A_n, B_n → O_n	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5		70	145	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	850 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4 500 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	14 700 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

8-INPUT NOR GATE

The HEF4078B provides the positive 8-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

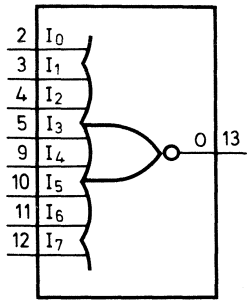


Fig. 1 Functional diagram.

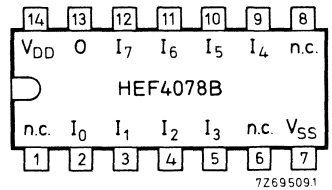


Fig. 2 Pinning diagram.

HEF4078BP : 14-lead DIL; plastic (SOT-27).
HEF4078BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4078BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

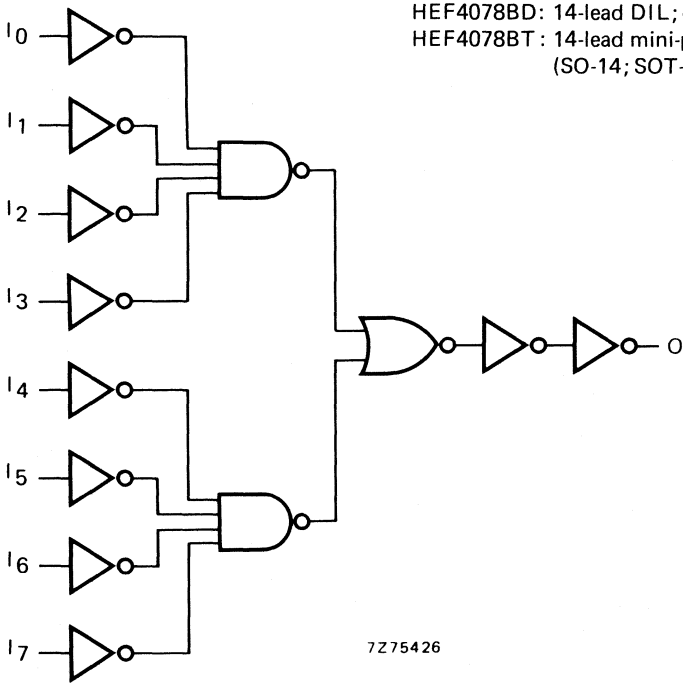


Fig. 3 Logic diagram.

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		80	160	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
	5		80	160	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	750 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2800 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	7500 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

QUADRUPLE 2-INPUT AND GATE

The HEF4081B provides the positive quadruple 2-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

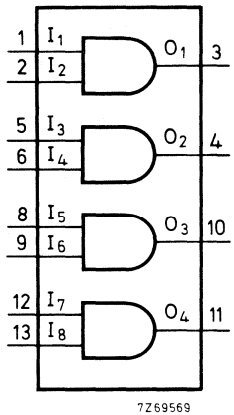


Fig.1 Functional diagram.

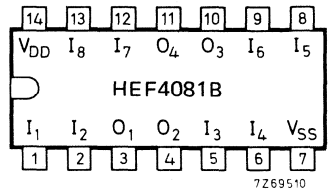


Fig.2 Pinning diagram.

HEF4081BP : 14-lead DIL; plastic (SOT-27).
HEF4081BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4081BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

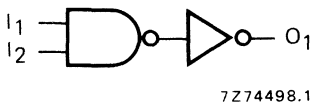


Fig.3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		55	110	ns	28 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		45	90	ns	18 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	450 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2 900 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	11 700 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

DUAL 4-INPUT AND GATE

The HEF4082B provides the positive dual 4-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

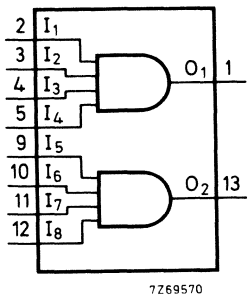


Fig. 1 Functional diagram.

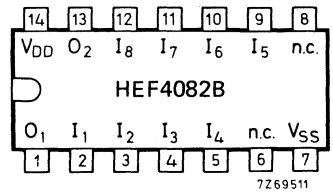


Fig. 2 Pinning diagram.

HEF4082BP : 14-lead DIL; plastic (SOT-27).
HEF4082BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4082BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

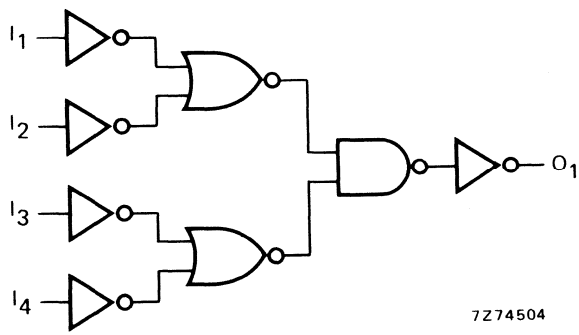


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays	5		65	125	ns	38 ns + (0,55 ns/pF) C_L
$I_n \longrightarrow O_n$	10	t_{PHL};t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	45	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

The HEF4085B is a dual 2-wide 2-input AND-OR-invert gate, each with an additional input (A_4 or B_4) which can be used as either an expander input or an inhibit input. A HIGH on A_4 or B_4 forces the output (O_A or O_B) LOW independent of the other inputs (A_0 to A_3 or B_0 to B_3). The outputs O_A and O_B are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

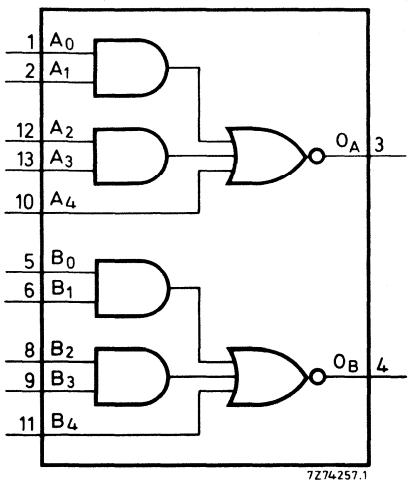


Fig. 1 Functional diagram.

Fig. 2 Pinning diagram.

HEF4085BP : 14-lead DIL; plastic (SOT-27).
HEF4085BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4085BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

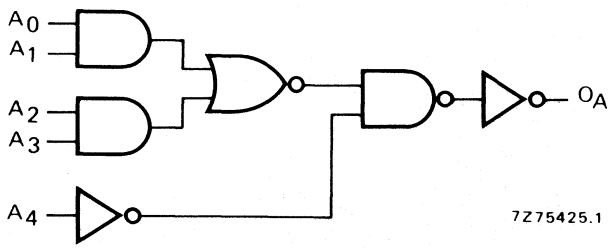


Fig. 3 Logic diagram (one gate).

LOGIC FUNCTION

$$O_A = \overline{A_0 \cdot A_1 + A_2 \cdot A_3 + A_4}$$

$$O_B = \overline{B_0 \cdot B_1 + B_2 \cdot B_3 + B_4}$$

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
A_n, B_n → O_n	5		75	155	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		65	135	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	55	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	750 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	3200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	9200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

4-WIDE 2-INPUT AND-OR-INVERT GATE

The HEF4086B is a 4-wide 2-input AND-OR-invert (AOI) gate with two additional inputs (I_8 and $\bar{I}_9$) which can be used as either expander or inhibit inputs by connecting them to any standard LOCMOS output. A HIGH on I_8 or a LOW on $\bar{I}_9$ forces the output (O) LOW independent of the other eight inputs (I_0 to I_7). The output (O) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.

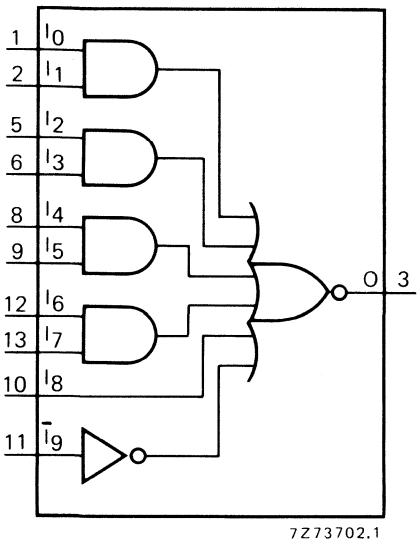


Fig. 1 Functional diagram.

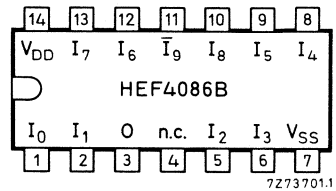


Fig. 2 Pinning diagram.

HEF4086BP : 14-lead DIL; plastic (SOT-27).
HEF4086BD : 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4086BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

PINNING

I_0 to I_8	gate inputs
$\bar{I}_9$	gate input (active LOW)
O	output (active LOW)

FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

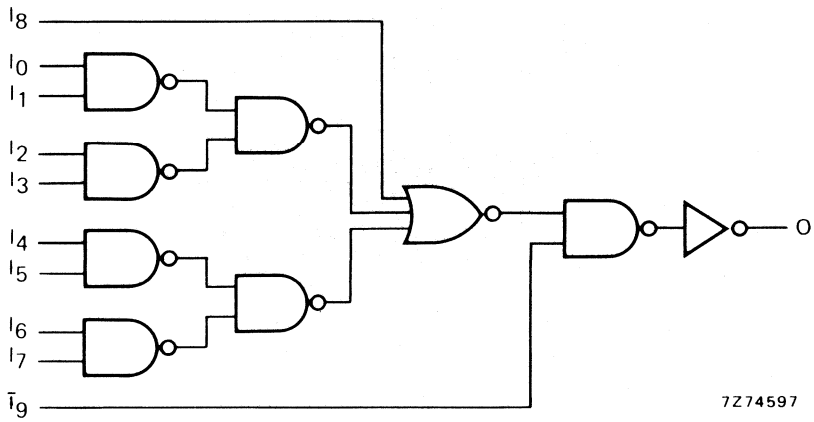


Fig. 3 Logic diagram.

LOGIC EQUATION

$$O = \overline{I_0 \cdot I_1 + I_2 \cdot I_3 + I_4 \cdot I_5 + I_6 \cdot I_7 + I_8 + I_9}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
I_0 to I_7 → O	5		90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	65	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		80	155	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
I_8 → O	5		70	140	ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	55	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		55	115	ns	28 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	25	ns	7 ns + (0,16 ns/pF) C_L
$\overline{I_9}$ → O	5		55	105	ns	28 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	20	45	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
	5		45	90	ns	18 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	15	35	ns	4 ns + (0,23 ns/pF) C_L
	15		10	25	ns	2 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	525 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	2600 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	7300 f_i + Σ($f_o C_L$) x V_{DD}^2	

APPLICATION INFORMATION

Figure 4 shows two HEF4086B ICs connected to obtain an 8-wide 2-input AOI function. The output (O_A) of the first IC is fed directly into the $\overline{I}_{9B}$ gate input of the second IC. Similarly, any NAND gate output can be fed directly into the $\overline{I}_9$ gate input to obtain a 5-wide AOI function. In addition, any AND gate output can be fed directly into the I_8 gate input with the same result.

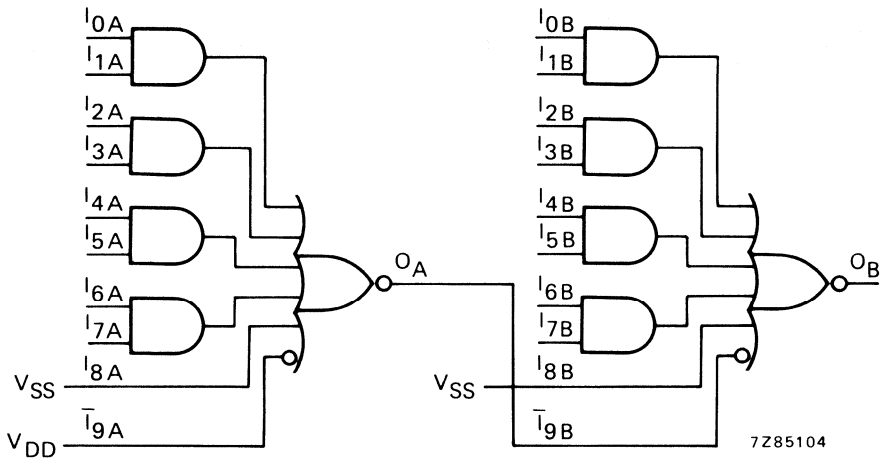


Fig. 4 Two HEF4086B ICs connected as an 8-wide 2-input AOI gate.

Logic equation for Fig. 4:

$$O_B = \overline{I_{0A} \cdot I_{1A} + I_{2A} \cdot I_{3A} + I_{4A} \cdot I_{5A} + I_{6A} \cdot I_{7A} + I_{0B} \cdot I_{1B} + I_{2B} \cdot I_{3B} + I_{4B} \cdot I_{5B} + I_{6B} \cdot I_{7B}}$$

QUADRUPLE 2-INPUT NAND SCHMITT TRIGGER

The HEF4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H).

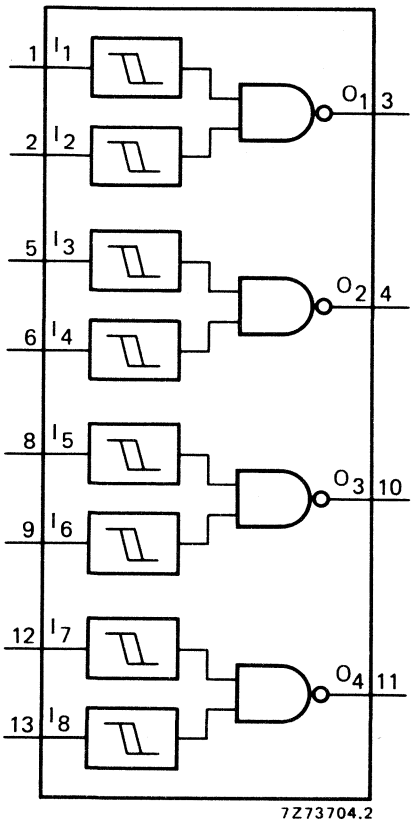


Fig. 1 Functional diagram.

Fig. 2 Pinning diagram.

HEF4093BP : 14-lead DIL; plastic (SOT-27).
HEF4093BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4093BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

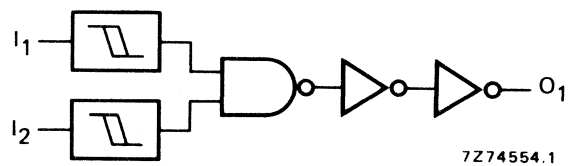


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C

	V_{DD} V	symbol	min.	typ.	max.	
Hysteresis voltage	5	V_H	0,4	0,7	–	V
	10		0,6	1,0	–	V
	15		0,7	1,3	–	V
Switching levels positive-going input voltage	5	V_P	1,9	2,9	3,5	V
	10		3,6	5,2	7	V
	15		4,7	7,3	11	V
negative-going input voltage	5	V_N	1,5	2,2	3,1	V
	10		3	4,2	6,4	V
	15		4	6,0	10,3	V

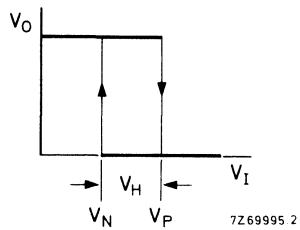


Fig. 4 Transfer characteristic.

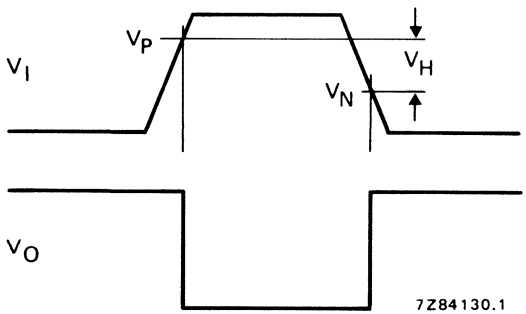


Fig. 5 Waveforms showing definition of V_P, V_N and V_H; where V_N and V_P are between limits of 30% and 70%.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays	5		90	185	ns	63 ns + (0,55 ns/pF) C_L
$I_n \rightarrow O_n$	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF) C_L
HIGH to LOW	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1300 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	6400 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	
	15	18 700 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	

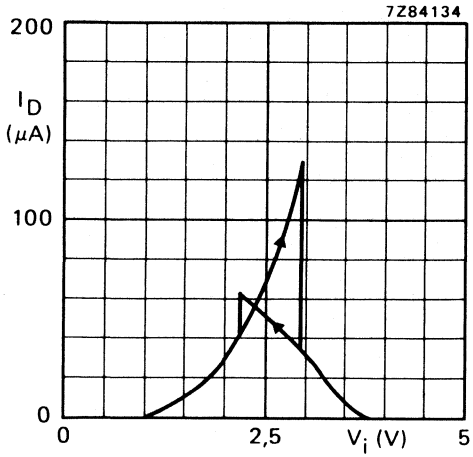


Fig. 6 Typical drain current as a function of input voltage; V_{DD} = 5 V; T_{amb} = 25 °C.

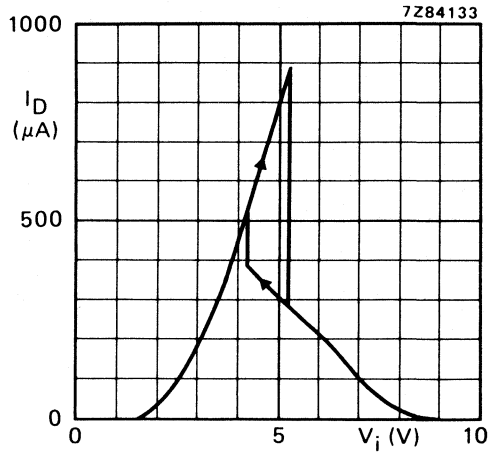


Fig. 7 Typical drain current as a function of input voltage; V_{DD} = 10 V; T_{amb} = 25 °C.

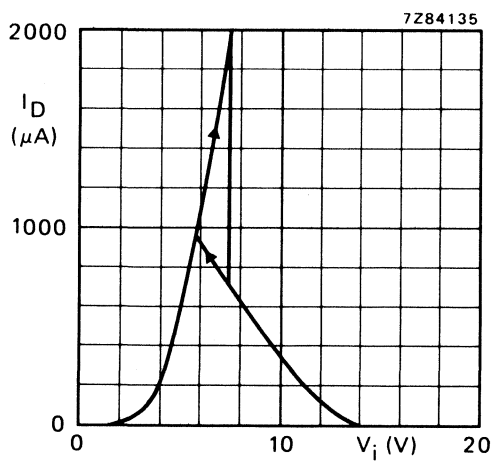


Fig. 8 Typical drain current as a function of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

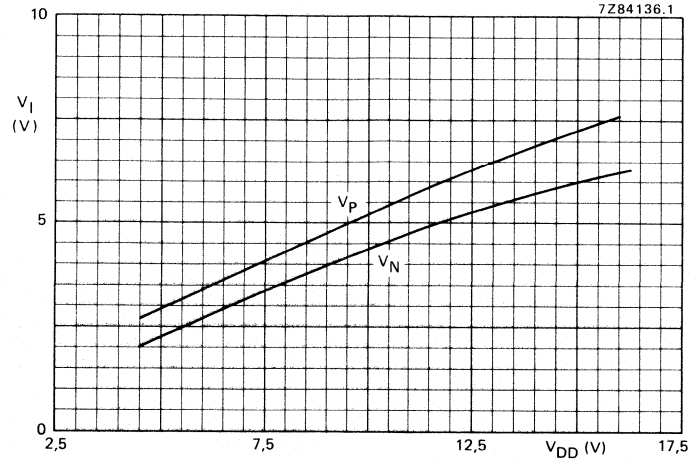


Fig. 9 Typical switching levels as a function of supply voltage V_{DD}; T_{amb} = 25 °C.

APPLICATION INFORMATION

Some examples of applications for the HEF4093B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

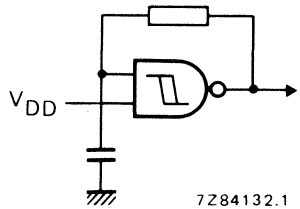


Fig. 10 The HEF4093B used as a astable multivibrator.

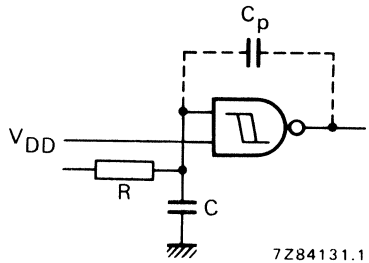


Fig. 11 Schmitt trigger driven via a high impedance ($R > 1\ k\Omega$).

If a Schmitt trigger is driven via a high impedance ($R > 1\ k\Omega$) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD}-V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

C_p is the external parasitic capacitance between inputs and output; the value depends on the circuit board layout.

Note

The two inputs may be connected together, but this will result in a larger through-current at the moment of switching.

8-STAGE SHIFT-AND-STORE BUS REGISTER

The HEF4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs O_0 to O_7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_S and O'_S) are available for cascading a number of HEF4094B devices. Data is available at O_S on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O'_S on the next negative-going clock edge and provides cascading HEF4094B devices when the clock rise time is slow.

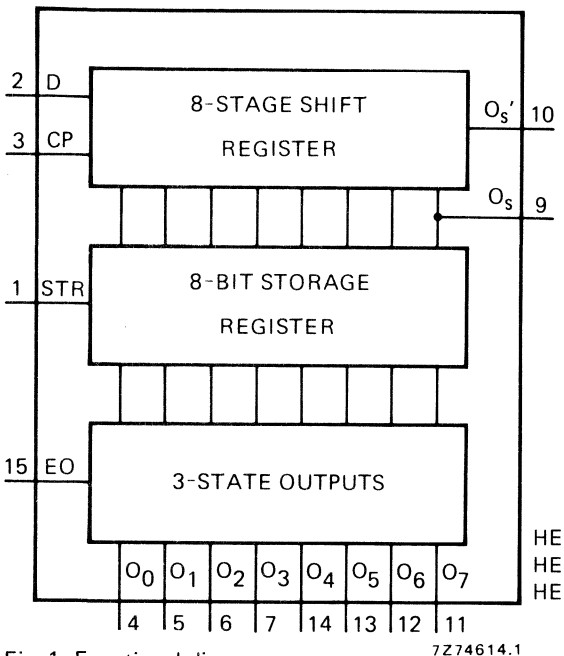


Fig. 1 Functional diagram.

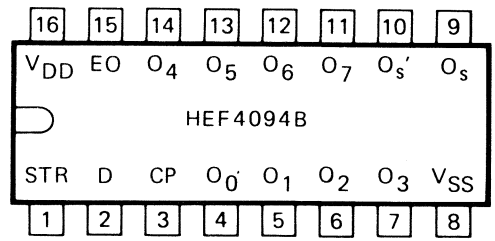


Fig. 2 Pinning diagram.

HEF4094BP : 16-lead DIL; plastic (SOT-38Z).
HEF4094BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4094BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D	data input	EO	output enable input
CP	clock input	O_S, O'_S	serial outputs
STR	strobe input	O_0 to O_7	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

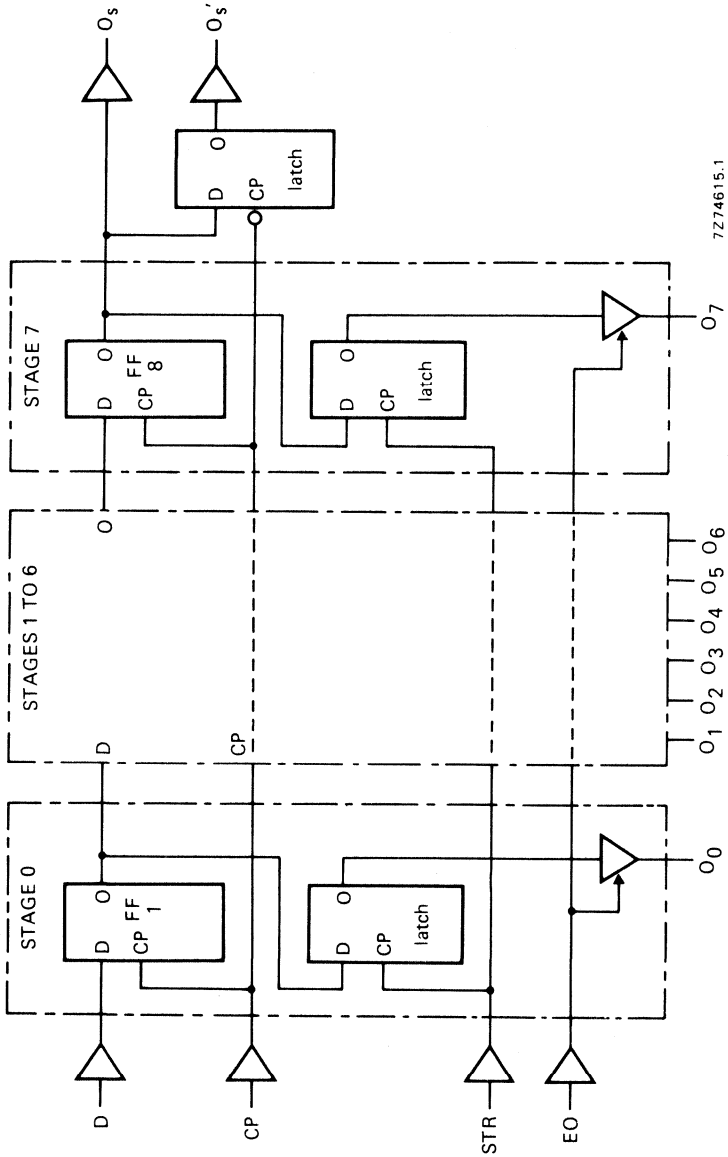


Fig. 3a Logic diagram.

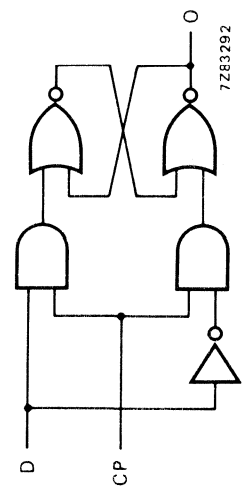


Fig. 3b One D-latch.

FUNCTION TABLE

inputs				parallel outputs		serial outputs	
CP	EO	STR	D	O_0	O_n	O_s	O'_s
∫	L	X	X	Z	Z	O'_6	nc
⌞	L	X	X	Z	Z	nc	O_7
∫	H	L	X	nc	nc	O'_6	nc
∫	H	H	L	L	O_{n-1}	O'_6	nc
∫	H	H	H	H	O_{n-1}	O'_6	nc
⌞	H	H	H	nc	nc	nc	O_7

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌞ = negative-going transition
Z = high impedance off state
nc = no change
O'_6 = the information in the seventh shift register stage

At the positive clock edge the information in the 7th register stage is transferred to the 8th register stage and the O_s output.

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$9700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$26\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
CP → O_s	5		135	270	ns	108 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L
	5		105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
CP → O'_s	5		105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
	5		105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
CP → O_n	5		165	330	ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	75	150	ns	64 ns + (0,23 ns/pF) C_L
	15		55	110	ns	47 ns + (0,16 ns/pF) C_L
	5		150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		55	110	ns	47 ns + (0,16 ns/pF) C_L
STR → O_n	5		110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
	5		100	200	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	45	90	ns	34 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leqslant 20$ ns

	V_{DD} V	symbol	min.	typ.	max.	
3-state propagation delays						
Output enable times	5			40	80	ns
EO → O_n	10	t_{PZH}		25	50	ns
HIGH	15			20	40	ns
	5			40	80	ns
LOW	10	t_{PZL}		25	50	ns
	15			20	40	ns
Output disable times	5			75	150	ns
EO → O_n	10	t_{PHZ}		40	80	ns
HIGH	15			30	60	ns
	5			80	160	ns
LOW	10	t_{PLZ}		40	80	ns
	15			30	60	ns
Minimum clock	5		60	30		ns
pulse width	10	t_{WCPL}	30	15		ns
LOW	15		24	12		ns
Minimum strobe	5		40	20		ns
pulse width	10	t_{WSTRH}	30	15		ns
HIGH	15		24	12		ns
Set-up times	5		60	30		ns
D → CP	10	t_{su}	20	10		ns
	15		15	5		ns
Hold times	5		5	−15		ns
D → CP	10	t_{hold}	20	5		ns
	15		20	5		ns
Maximum clock	5		5	10		MHz
pulse frequency	10	f_{max}	11	22		MHz
	15		14	28		MHz

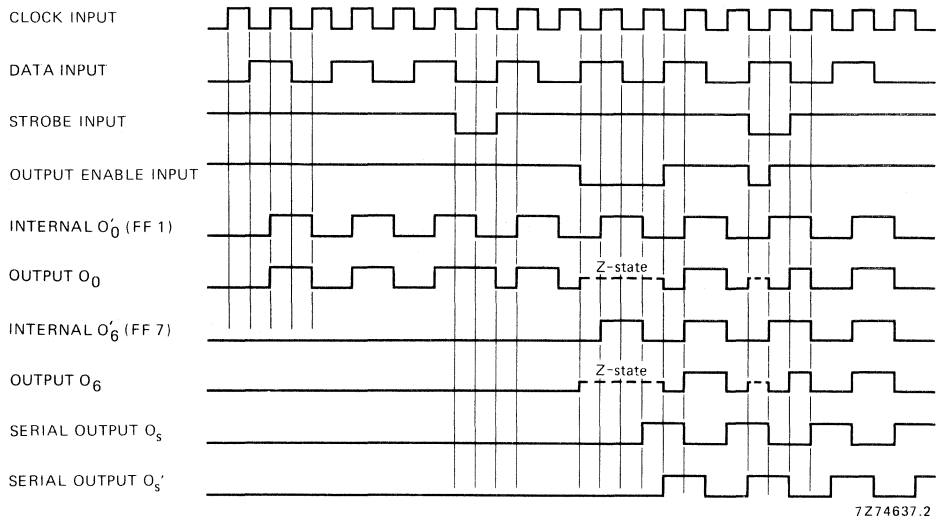


Fig. 4 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4094B are:

- Serial-to-parallel data conversion
- Remote control holding register

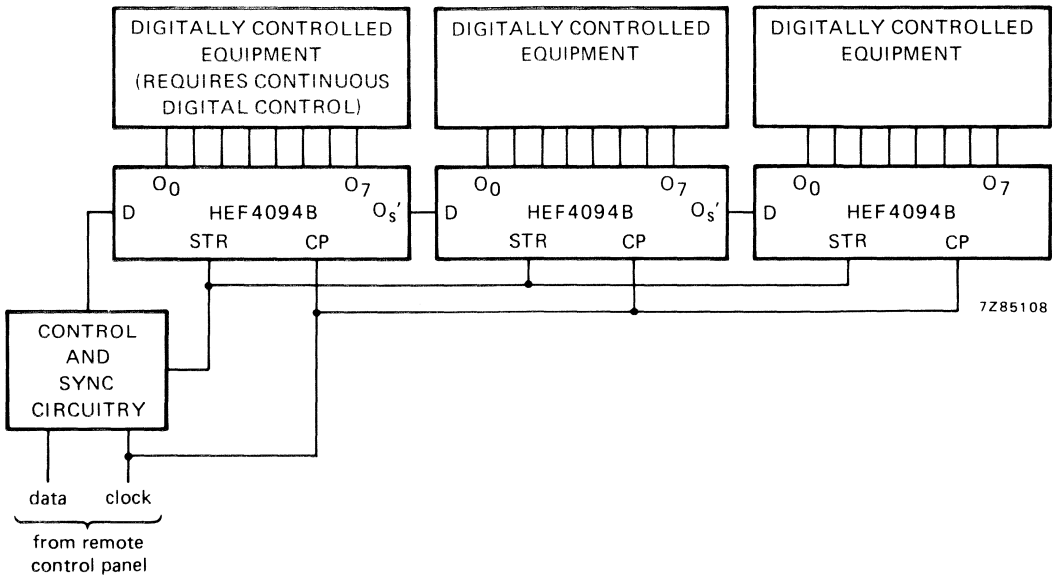


Fig. 5 Remote control holding register.

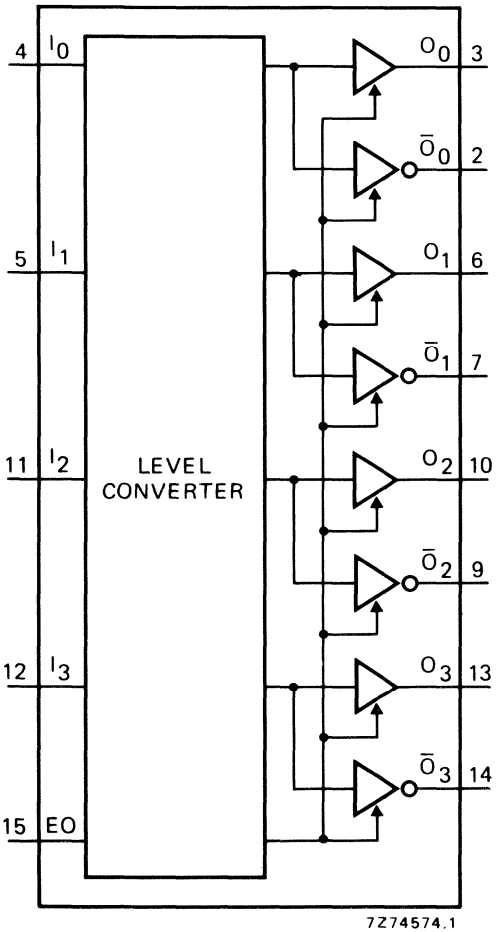
QUADRUPLE LOW TO HIGH VOLTAGE TRANSLATOR WITH 3-STATE OUTPUTS

The HEF4104B quadruple low voltage to high voltage translator with 3-state outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage LOCMOS and TTL to high voltage LOCMOS. It has four data inputs (I_0 to I_3), an active HIGH output enable input (EO), four data outputs (O_0 to O_3) and their complements ($\overline{O}_0$ to $\overline{O}_3$).

With EO HIGH, O_0 to O_3 and $\overline{O}_0$ to $\overline{O}_3$ are in the low impedance ON-state, either HIGH or LOW as determined by I_0 to I_3; with EO LOW, O_0 to O_3 and $\overline{O}_0$ to $\overline{O}_3$ are in the high impedance OFF-state.

The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. For the permissible operating range of V_{DDI} and V_{DDO} see graph Fig. 4.

Each input protection circuit is terminated between V_{DDO} and V_{SS}. This allows the input signals to be driven from any potential between V_{DDO} and V_{SS}, without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS}, the current at each input must be limited to 10 mA.



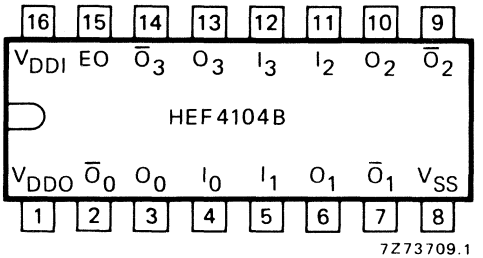


Fig. 2 Pinning diagram.

HEF4104BP : 16-lead DIL; plastic (SOT-38Z).
HEF4104BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4104BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

I_0 to I_3	data inputs
EO	output enable input
O_0 to O_3	data outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary data outputs

Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

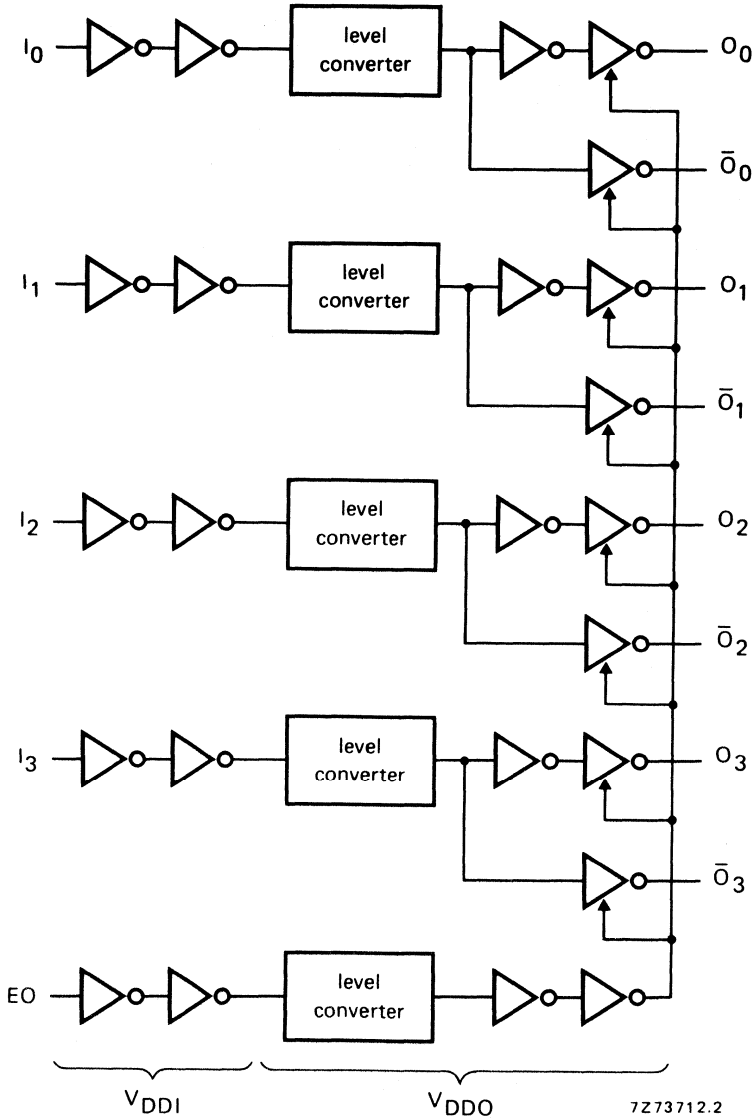


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n, \overline{O}_n$	5		170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	80	160	ns	69 ns + (0,23 ns/pF) C_L
	15		65	135	ns	57 ns + (0,16 ns/pF) C_L
	5		170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	80	160	ns	69 ns + (0,23 ns/pF) C_L
	15		70	140	ns	62 ns + (0,16 ns/pF) C_L
Output transition times						
HIGH to LOW	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays						
Output disable times						
$EO \rightarrow O_n, \overline{O}_n$	5		70	135	ns	
HIGH	10	t_{PHZ}	55	110	ns	
	15		60	120	ns	
	5		70	135	ns	
LOW	10	t_{PLZ}	55	105	ns	
	15		55	110	ns	
Output enable times						
$EO \rightarrow O_n, \overline{O}_n$	5		195	395	ns	
HIGH	10	t_{PZH}	95	195	ns	
	15		80	165	ns	
	5		195	395	ns	
LOW	10	t_{PZL}	95	190	ns	
	15		80	160	ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	3 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	12 200 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	31 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

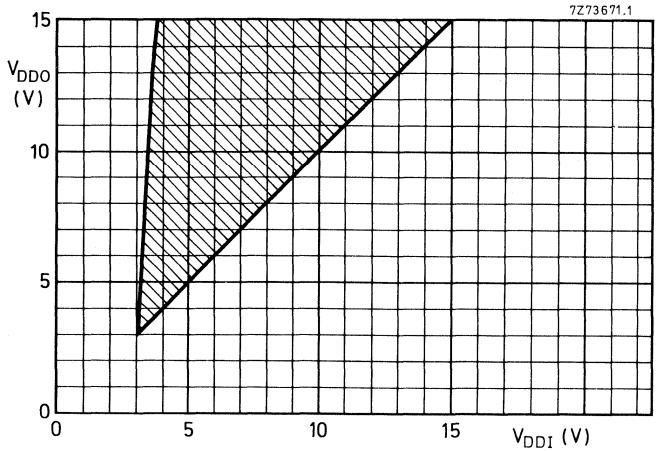


Fig. 4 V_{DDO} as a function of V_{DDI}; the shaded area shows the permissible operating range.

STROBED HEX INVERTER/BUFFER

The HEF4502B consists of six inverter/buffers with 3-state outputs. When the output enable input ($\overline{EO}$) is HIGH all six outputs (O_1 to O_6) are in the high impedance OFF-state. When the enable input ($\overline{E}$) is HIGH all six outputs are switched to LOW. The outputs have a 2-TTL load drive capability.

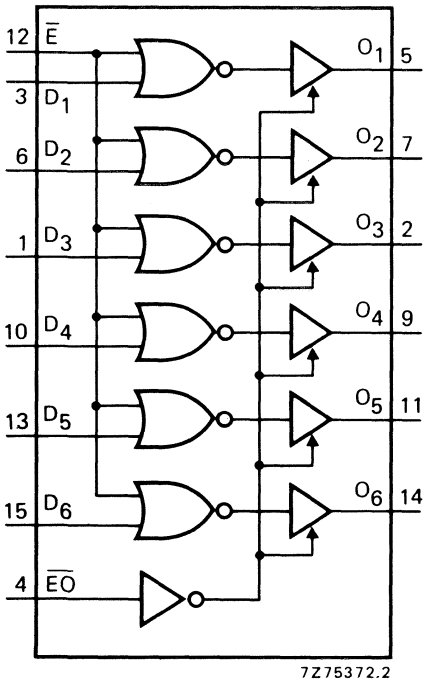


Fig. 1 Functional diagram.

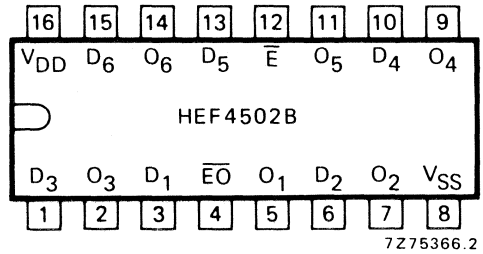


Fig. 2 Pinning diagram.

HEF4502BP : 16-lead DIL; plastic (SOT-38Z).
HEF4502BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4502BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_1 to D_6	data inputs
$\overline{E}$	enable input
$\overline{EO}$	output enable input
O_1 to O_6	3-state outputs

TRUTH TABLE

inputs			output
D_n	$\overline{E}$	$\overline{EO}$	O_n
L	L	L	H
H	L	L	L
X	H	L	L
X	X	H	Z

H = HIGH state (the more pos. voltage)
L = LOW state (the less pos. voltage)
X = state is immaterial
Z = high impedance off state

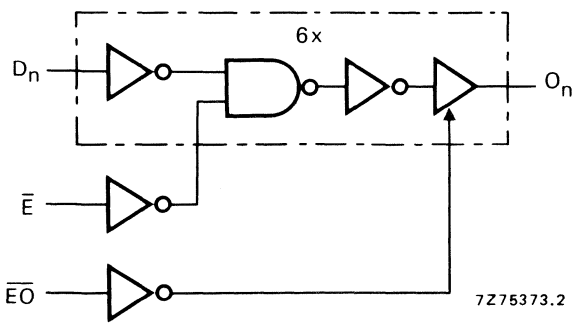


Fig. 3 Logic diagram.

FAMILY DATA
I_{DD} LIMITS category BUFFERS } see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+ 25 min.	+ 25 max.	+ 85 min.	+ 85 max.	
Output current HIGH	5	4,6		$-I_{OH}$	1,2		1,0		0,8		mA
	10	9,5			3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
Output current HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current LOW	4,75		0,4		3,5		2,9		2,3		mA
	10		0,5	I_{OL}	12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$5\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = output freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$25\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$85\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

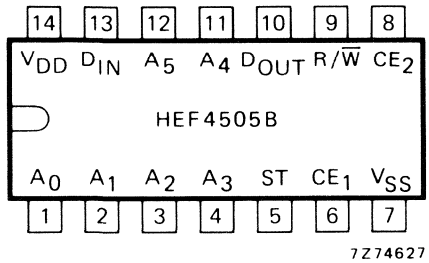
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.	typical extrapolation formula
Propagation delays					
D_n, $\overline{E}$ → O_n	5		85	170 ns	77 ns + (0,17 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	40	80 ns	37 ns + (0,06 ns/pF) C_L
	15		35	70 ns	33 ns + (0,04 ns/pF) C_L
	5		80	160 ns	66 ns + (0,28 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70 ns	28 ns + (0,13 ns/pF) C_L
	15		30	60 ns	25 ns + (0,10 ns/pF) C_L
Output transition times					
	5		25	50 ns	10 ns + (0,30 ns/pF) C_L
HIGH to LOW	10	t_{THL}	12	24 ns	7 ns + (0,11 ns/pF) C_L
	15		8	15 ns	5 ns + (0,07 ns/pF) C_L
	5		30	60 ns	5 ns + (0,50 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	15	30 ns	3 ns + (0,24 ns/pF) C_L
	15		12	24 ns	3 ns + (0,18 ns/pF) C_L
3-state propagation delays					
Output disable times					
$\overline{EO}$ → O_n	5		60	160 ns	
HIGH	10	t_{PHZ}	55	140 ns	
	15		55	140 ns	
	5		50	100 ns	
LOW	10	t_{PLZ}	35	70 ns	
	15		30	60 ns	
Output enable times					
$\overline{EO}$ → O_n	5		60	120 ns	
HIGH	10	t_{PZH}	35	70 ns	
	15		30	60 ns	
	5		55	110 ns	
LOW	10	t_{PZL}	25	50 ns	
	15		20	40 ns	

64-BIT, 1-BIT PER WORD RANDOM ACCESS READ/WRITE MEMORY

The HEF4505B is a 64-bit, 1-bit per word, fully decoded and completely static, random access memory. The memory is strobed for reading or writing only when the strobe input (ST), chip enable inputs (CE_1 and CE_2) are HIGH simultaneously. The output data is available at the data output (D_{OUT}) only when the memory is strobed, the read/write input ($R/\overline{W}$) is HIGH and after the read access time has passed. Note that the three-state output is initially disabled and always goes to the LOW state before data is valid. The output is disabled in the high-impedance OFF-state, when the memory is not strobed or $R/\overline{W}$ is LOW. $R/\overline{W}$ may remain HIGH during a read cycle or LOW during a write cycle. The output data has the same polarity as the input data.



HEF4505BP : 14-lead DIL; plastic (SOT-27).
HEF4505BD: 14-lead DIL; ceramic (cerdip) (SOT-73).

Fig. 1 Pinning diagram.

PINNING

A_0 to A_5	address inputs
CE_1, CE_2	chip enable inputs
$R/\overline{W}$	read/write input
ST	strobe input
D_{IN}	data input
D_{OUT}	data output

FUNCTION TABLE

ST, CE_1, CE_2	$R/\overline{W}$	D_{OUT}	mode
L	L	Z	disabled
H	L	Z	write
L	H	Z	disabled
H	H	equal to memory data	read

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
Z = high-impedance OFF-state

SUPPLY VOLTAGE

rating	operating
-0,5 to +15	4,5 to 15 V

Minimum standby voltage for data retention is 3 V.

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

Products approved to CECC 90 104-062.

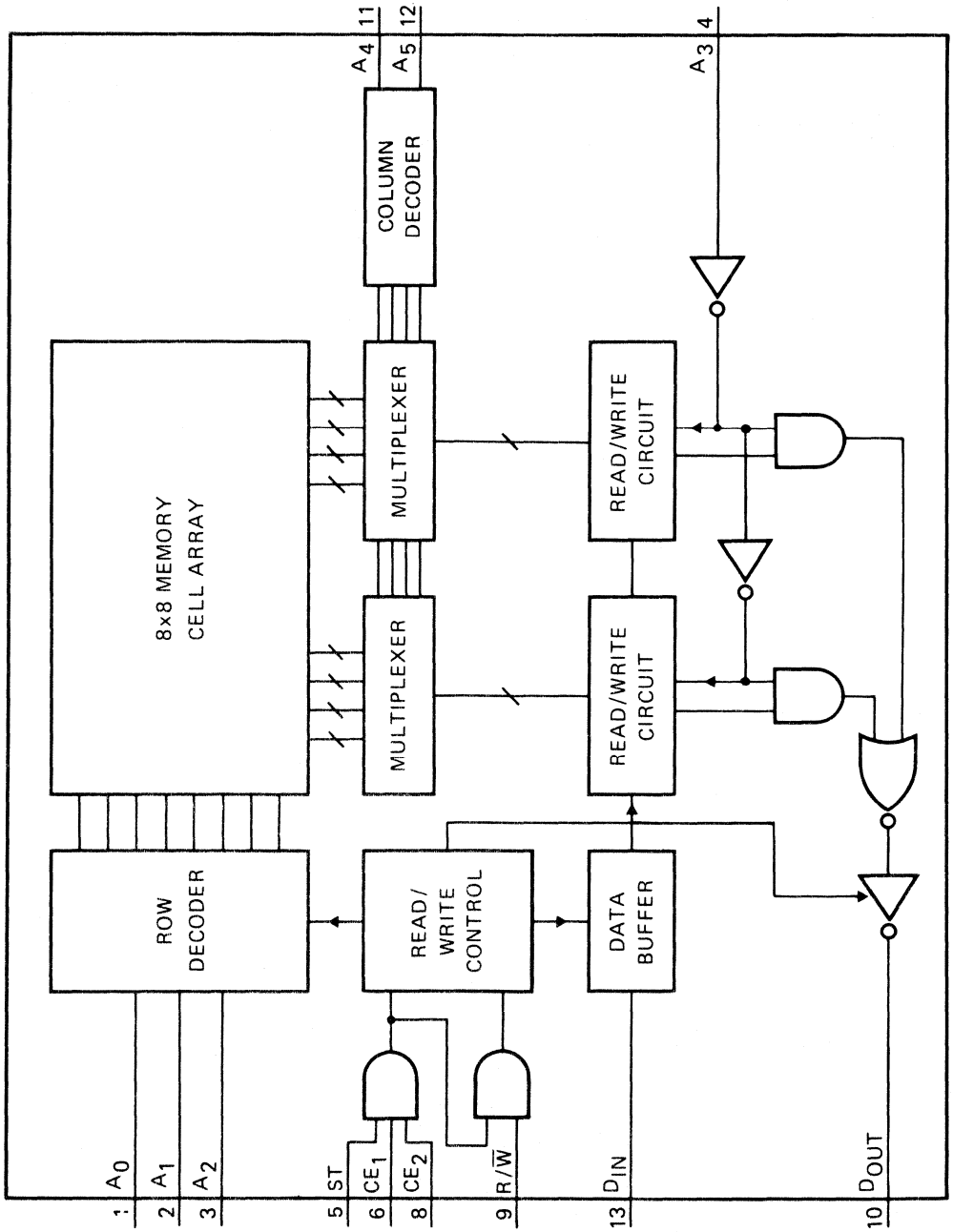
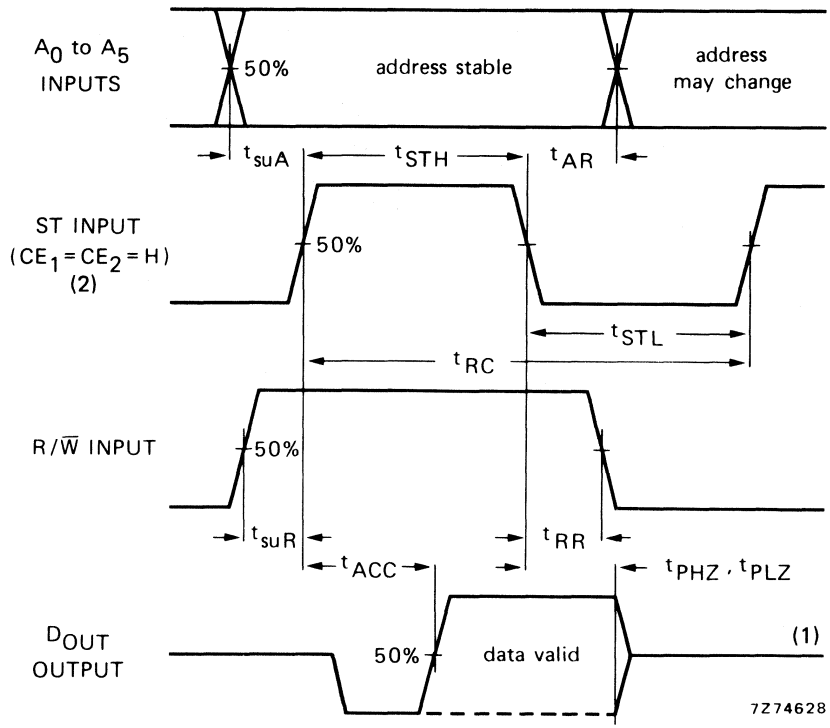


Fig. 2 Functional diagram.

A.C. CHARACTERISTICS

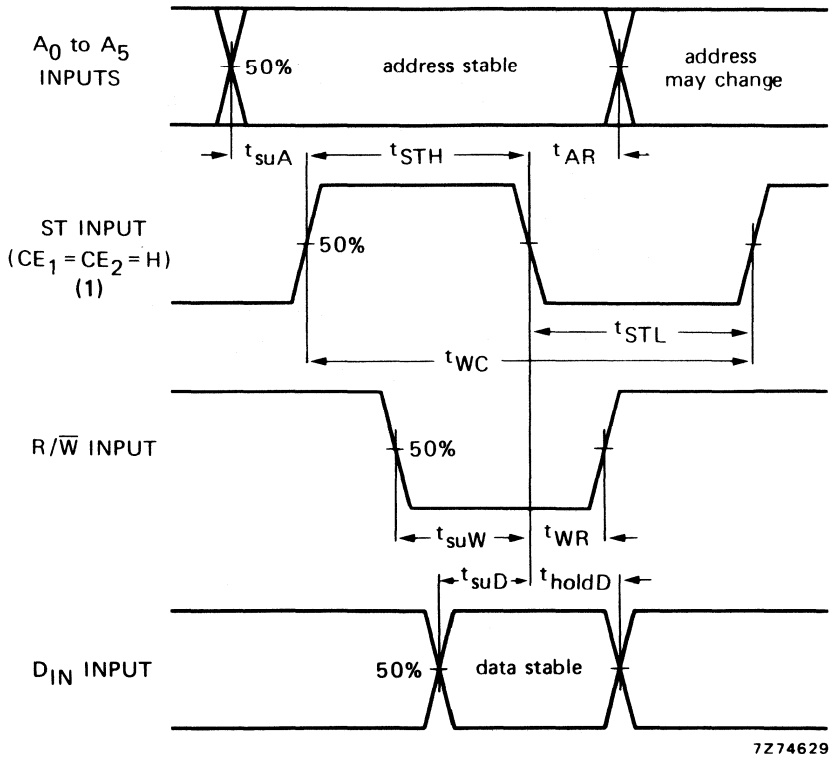
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Minimum strobe pulse width; LOW	5	t_{STL}	75	35		ns	
	10		45	22		ns	
	15		30	15		ns	
Read cycle time	5	t_{RC}		350	700	ns	
	10			250	500	ns	
	15			210	420	ns	
Write cycle time	5	t_{WC}		220	440	ns	
	10			125	250	ns	
	15			75	150	ns	
Read access time	5	t_{ACC}		330	660	ns	303 ns + (0,55 ns/pF) C_L
	10			135	270	ns	124 ns + (0,23 ns/pF) C_L
	15			100	200	ns	92 ns + (0,16 ns/pF) C_L
Address recovery time	5	t_{AR}	80	40		ns	
	10		40	20		ns	
	15		25	10		ns	
Read recovery time	5	t_{RR}	180	90		ns	
	10		120	60		ns	
	15		90	45		ns	
Write recovery time	5	t_{WR}	75	35		ns	
	10		45	25		ns	
	15		40	20		ns	
3-state propagation delays							
Output disable times	5	t_{PHZ}, t_{PLZ}		105	210	ns	
	10			60	125	ns	
	15			55	115	ns	
Set-up times							
$A_n \longrightarrow$ ST	5	t_{suA}	−20	−40		ns	
	10		−10	−20		ns	
	15		−5	−10		ns	
$R/\overline{W} \longrightarrow$ ST	5	t_{suR}	−30	−60		ns	
	10		−15	−30		ns	
	15		−5	−10		ns	
$D_{IN} \longrightarrow$ ST	5	t_{suD}	160	80		ns	
	10		75	35		ns	
	15		45	20		ns	
$R/\overline{W} \longrightarrow$ ST	5	t_{suW}	240	120		ns	
	10		100	50		ns	
	15		75	35		ns	
Hold time							
$D_{IN} \longrightarrow$ ST	5	t_{holdD}	−20	−40		ns	
	10		5	−10		ns	
	15		10	0		ns	



(1) Output in high impedance OFF-state.
(2) $t_{STHmin} = t_{RCmax} - t_{STLmin}$.

Fig. 3 Read cycle timing diagram.



(1) $t_{STHmin} = t_{WCmax} - t_{STLmin}$.

Fig. 4 Write cycle timing diagram.

APPLICATION INFORMATION

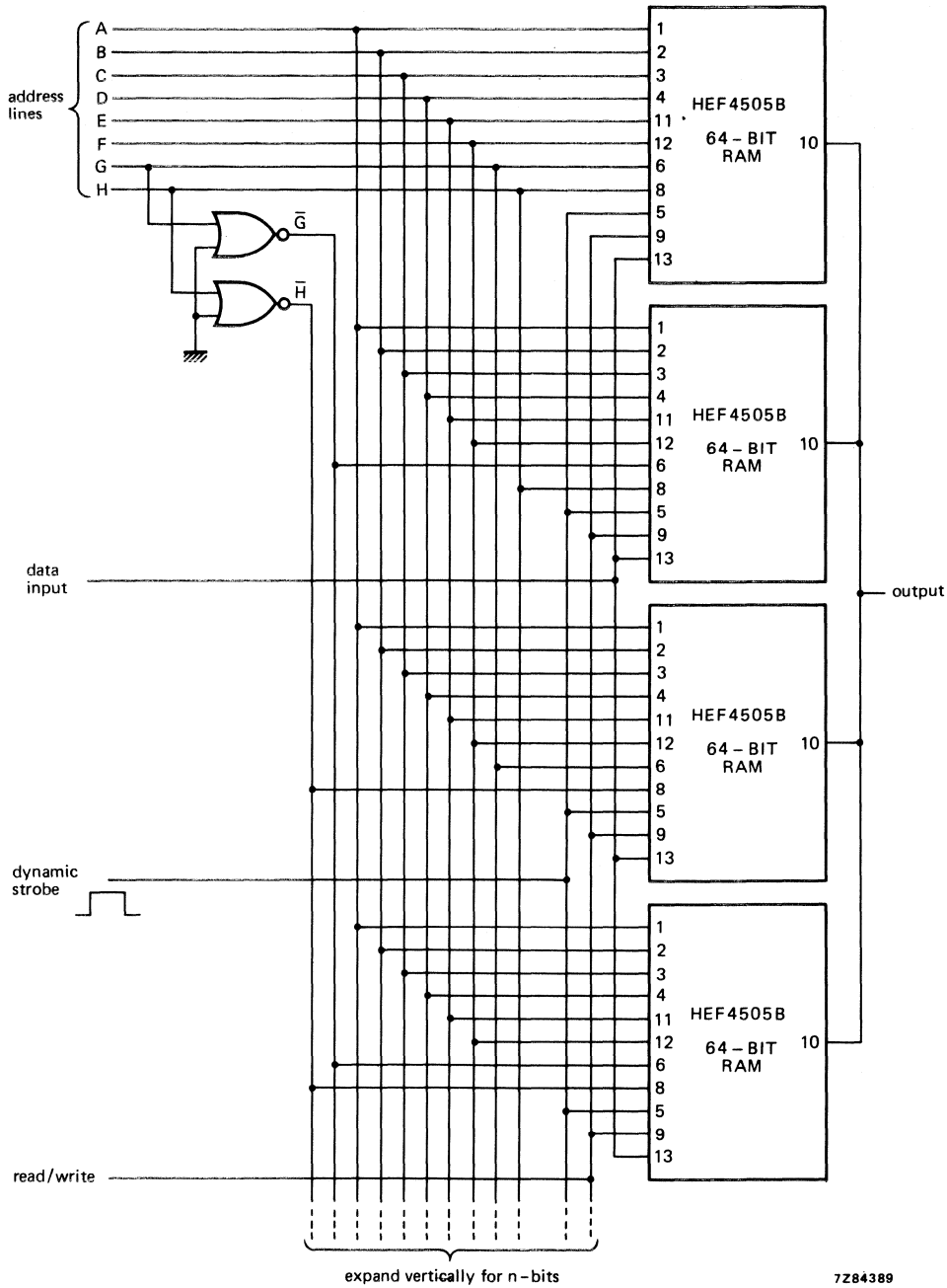


Fig. 5 256-word by n-bit static read/write memory using HEF4505B ICs.

Figure 5 shows a 256-word by n-bit static RAM system. The outputs of the four HEF4505B circuits are tied together to form 256 words by 1-bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and AND-ing them with the strobe input.

Fan-in and fan-out of the memory are limited only by speed requirements. The extremely low input and output leakage currents keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

The memory system shown in Fig. 5 can be interfaced directly with other ICs of the LOCMOS HE family. No external components are required.

Non-volatile information storage is allowed due to very low power dissipation when the memory is powered by a small standby battery. Figure 6 shows an optional standby power supply circuit for making a LOCMOS memory 'non-volatile'. When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor (R) which sets the charging rate. In Fig. 6 the sustaining voltage is V_B, and + V is the ordinary voltage from a power supply. V_{DD} is connected to the power supply pin of the memory. Low-leakage diodes are recommended to conserve battery power.

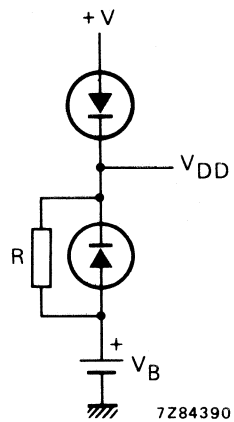


Fig. 6 Standby battery circuit.

DUAL 4-BIT LATCH

The HEF4508B is a dual 4-bit latch, which consists of two identical independent 4-bit latches with separate strobe (ST), master reset (MR), output-enable input ($\overline{EO}$) and 3-state outputs (O).

With the ST input in the HIGH state, the data on the D inputs appear at the corresponding outputs provided $\overline{EO}$ is LOW. Changing the ST input to the LOW state locks the data into the latch. A HIGH on the reset line forces the outputs to a LOW level regardless of the state of the ST input. The 3-state outputs are controlled by the output-enable input. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state regardless of other input conditions. This allows the outputs to interface directly with bus orientated systems. When $\overline{EO}$ is LOW the contents of the latches are available at the outputs.

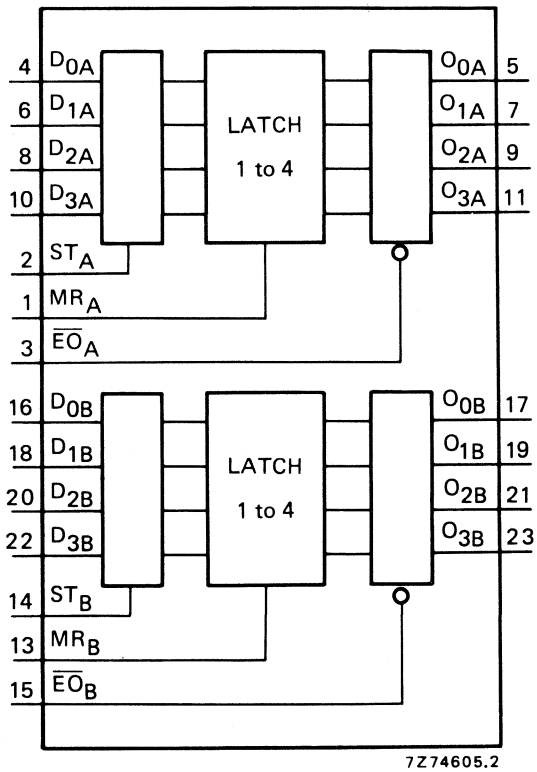


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Products approved to CECC 90 104-063.

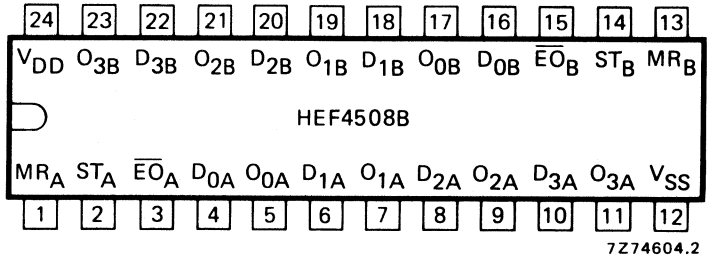


Fig. 2 Pinning diagram.

HEF4508BP : 24-lead DIL; plastic (SOT-101A).
HEF4508BD: 24-lead DIL; ceramic (cerdip) (SOT-94).
HEF4508BT : 24-lead mini-pack; plastic (SO-24; SOT-137A).

PINNING

D_{0A} to D_{3A}, D_{03} to D_{3B}	data inputs
ST_A, ST_B	strobe inputs
MR_A, MR_B	master reset inputs
$\overline{EO}_A$, $\overline{EO}_B$	output enable inputs
O_{0A} to O_{3A}, O_{0B} to O_{3B}	3-state outputs

FUNCTION TABLE

inputs				output
MR	ST	$\overline{EO}$	D_n	O_n
L	H	L	H	H
L	H	L	L	L
L	L	L	X	latched
H	X	L	X	L
X	X	H	X	Z

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance OFF state

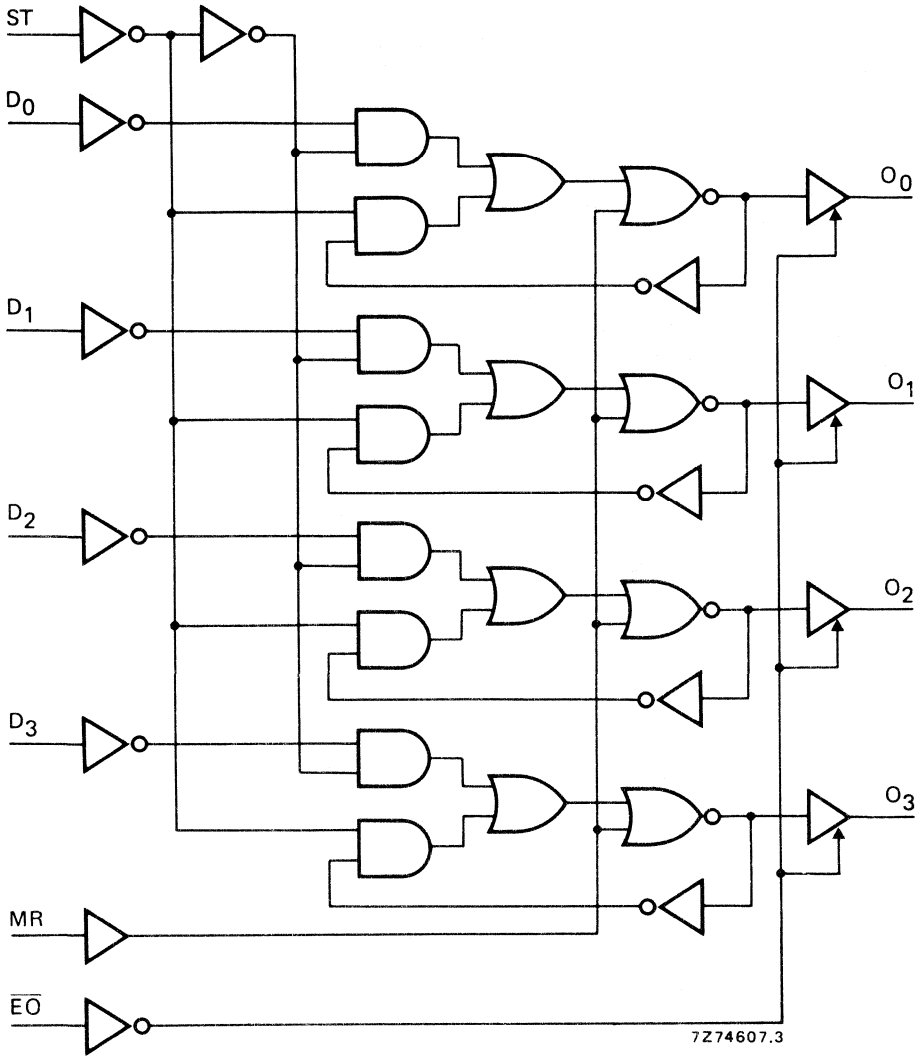


Fig. 3 Logic diagram (one 4-bit latch).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4.

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
ST → O_n	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
D_n → O_n	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
MR → O_n	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays							
Output enable times							
$\overline{EO}$ → O_n	5			45	90	ns	
HIGH	10	t_{PZH}		20	40	ns	
	15			18	36	ns	
	5			45	90	ns	
LOW	10	t_{PZL}		20	40	ns	
	15			18	36	ns	
Output disable times							
$\overline{EO}$ → O_n	5			35	70	ns	
HIGH	10	t_{PHZ}		20	40	ns	
	15			18	36	ns	
	5			45	90	ns	
LOW	10	t_{PLZ}		20	40	ns	
	15			18	36	ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum ST pulse width; HIGH	5	t_{WSTH}	50	25		ns	see also waveforms Fig. 4
	10		30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	40	20		ns	
	10		24	12		ns	
	15		20	10		ns	
Recovery time for MR	5	t_{RMR}	20	0		ns	
	10		20	0		ns	
	15		15	0		ns	
Set-up times $D_n \rightarrow$ ST	5	t_{su}	35	10		ns	
	10		25	5		ns	
	15		20	0		ns	
Hold times $D_n \rightarrow$ ST	5	t_{hold}	20	0		ns	
	10		20	0		ns	
	15		15	0		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$9\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$25\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

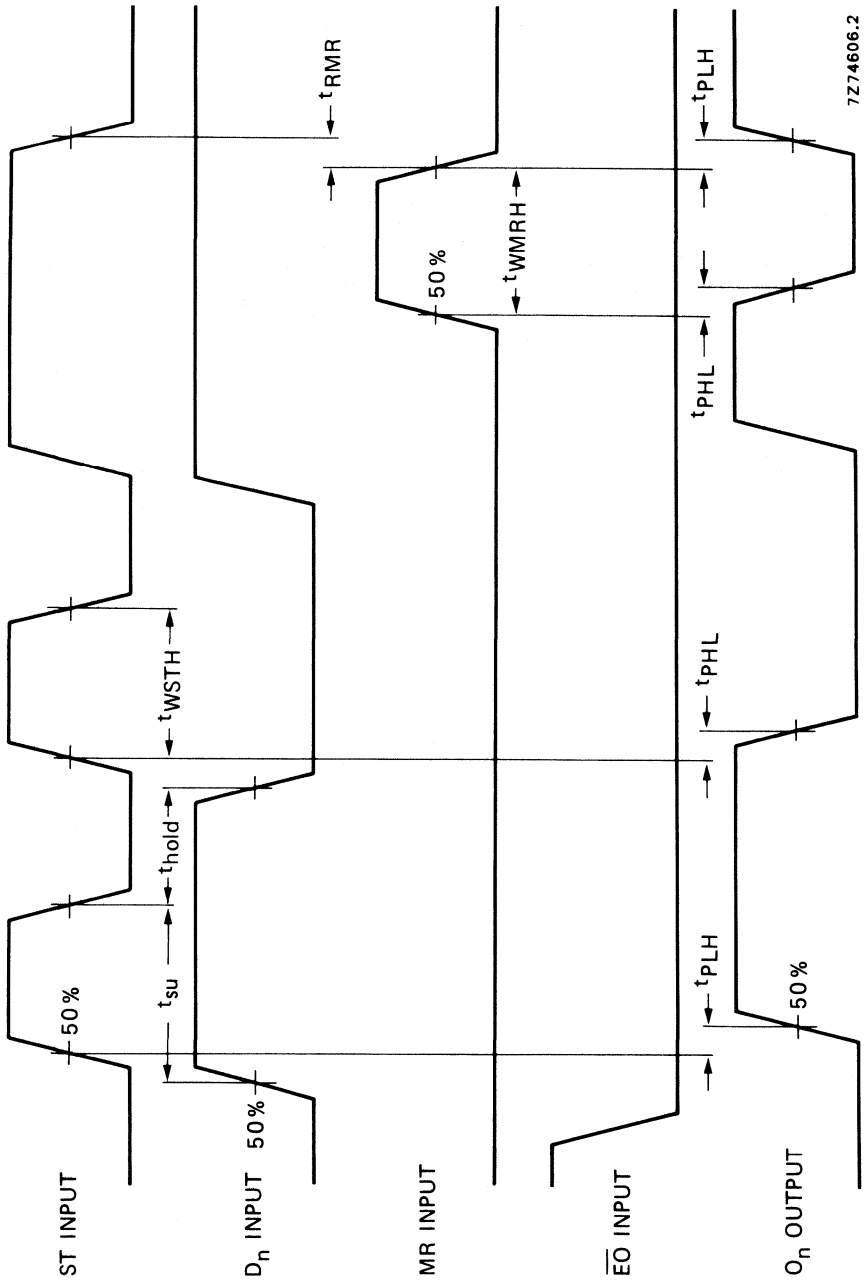


Fig. 4 Waveforms showing minimum ST and MR pulse widths, set-up and hold times for D_n to ST, recovery time for MR and propagation delays from ST to O_n, D_n to O_n and MR to O_n.

APPLICATION INFORMATION

Some examples of application for the HEF4508B are:

- Buffer storage
- Holding registers
- Data storage and multiplexing

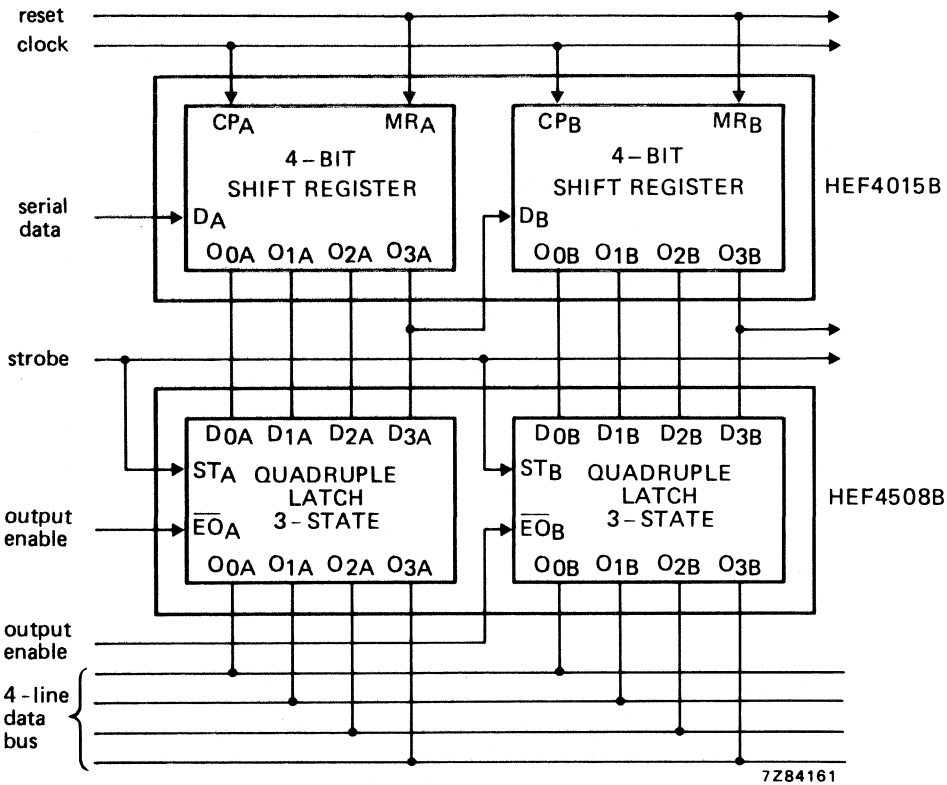


Fig. 5 Example of a bus register using HEF4508B and HEF4015B.

APPLICATION INFORMATION (continued)

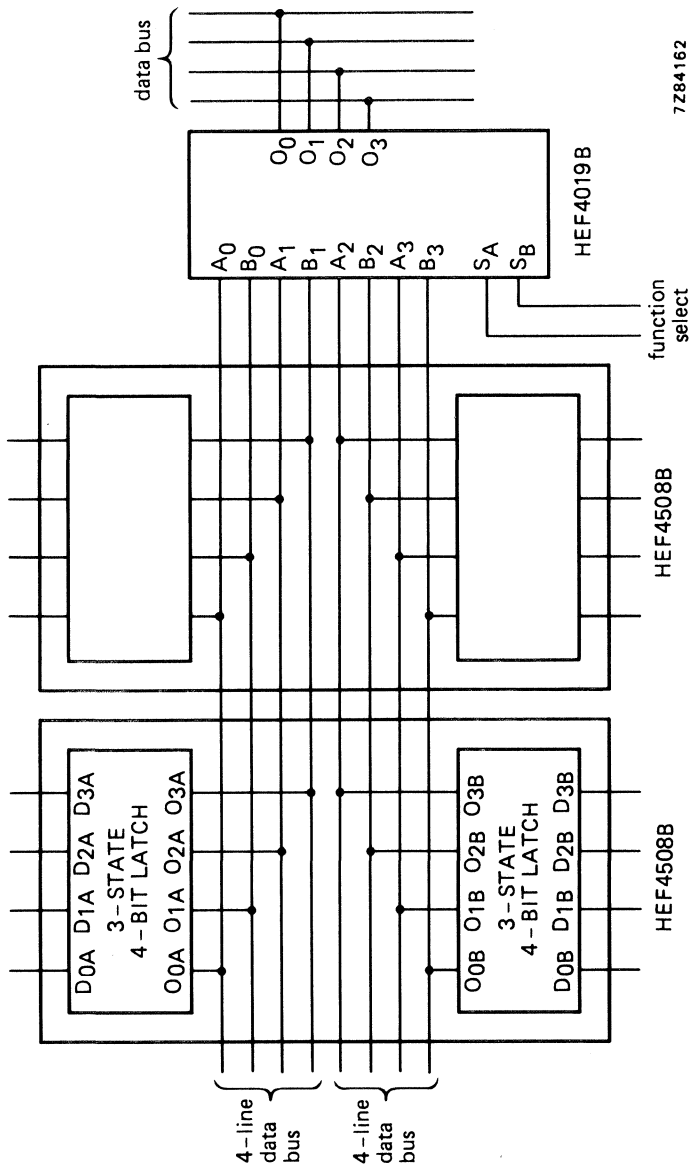


Fig. 6 Example of a dual multiplexed bus register with function select using two HEF4508B and one HEF4019B.

FUNCTION SELECT

S_A	S_B	function
L	L	inhibit (all L)
H	L	select A bus
L	H	select B bus
H	H	$A_1 + B_1$

BCD UP/DOWN COUNTER

The HEF4510B is an edge-triggered synchronous up/down BCD counter with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW to HIGH transition of CP if $\overline{CE}$ is LOW. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when O_0 and O_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when O_0 to O_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of all other input conditions.

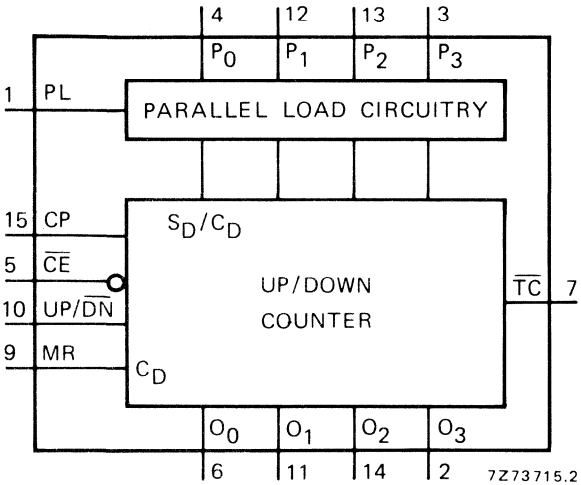


Fig. 1 Functional diagram.

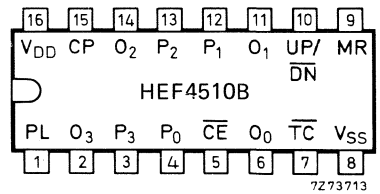


Fig. 2 Pinning diagram.

HEF4510BP : 16-lead DIL; plastic (SOT-38Z).
HEF4510BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4510BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

PL	parallel load input (active HIGH)	UP/$\overline{DN}$	up/down count control input
P_0 to P_3	parallel inputs	MR	master reset input
$\overline{CE}$	count enable input (active LOW)	$\overline{TC}$	terminal count output (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)	O_0 to O_3	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Products approved to CECC 90 104-064.

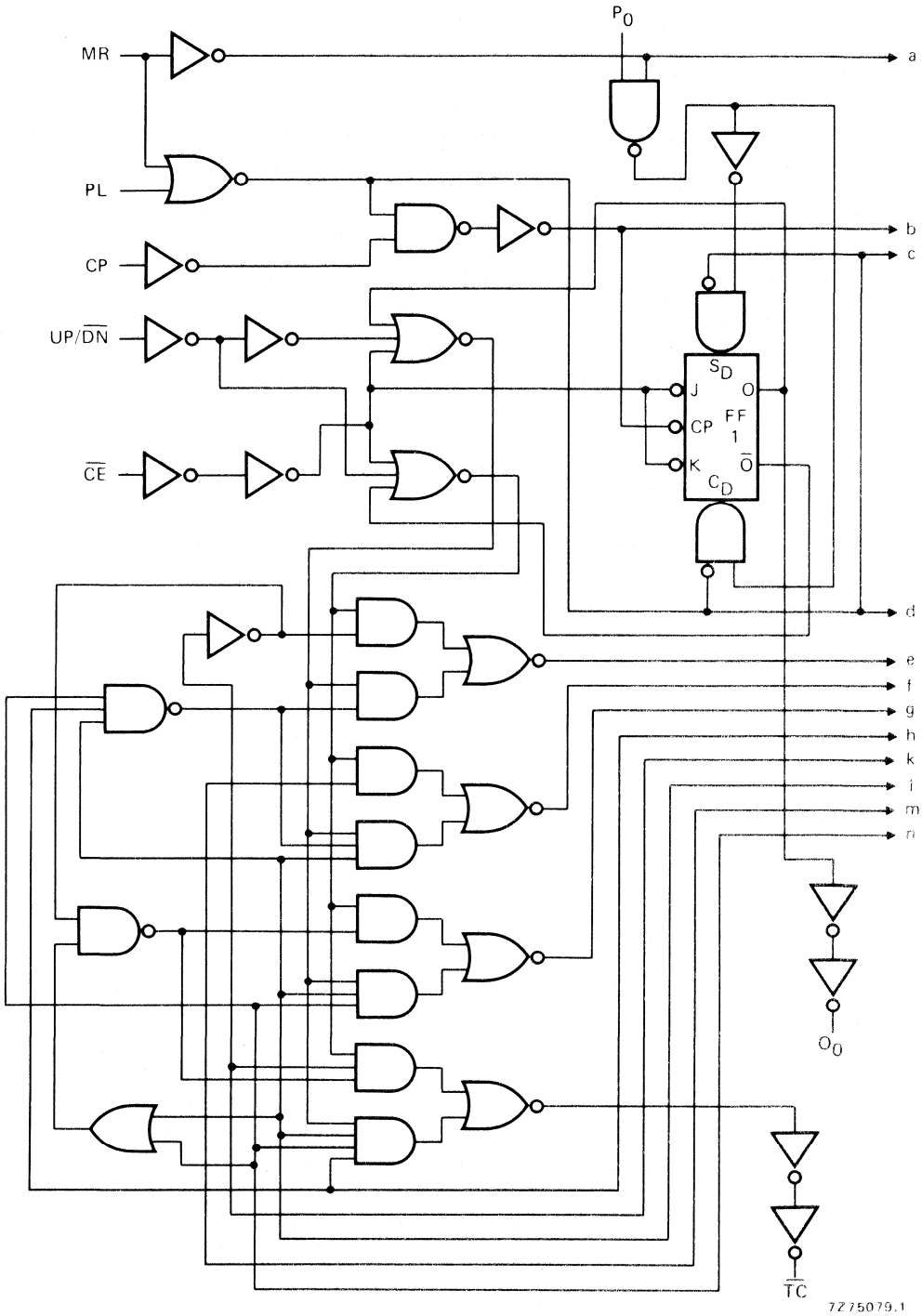


Fig. 3a Logic diagram (continued in Fig. 3b).

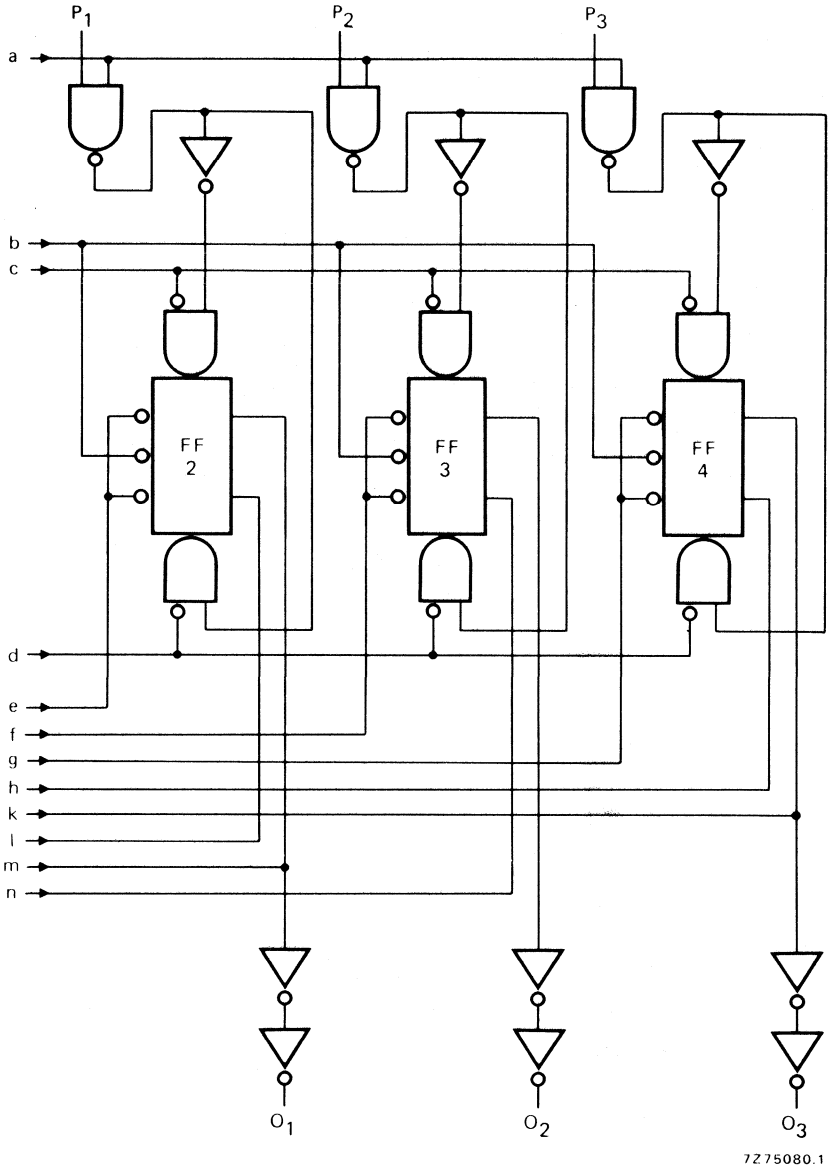


Fig. 3b Logic diagram (continued from Fig. 3a).

FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	∫	count down
L	L	H	L	∫	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition

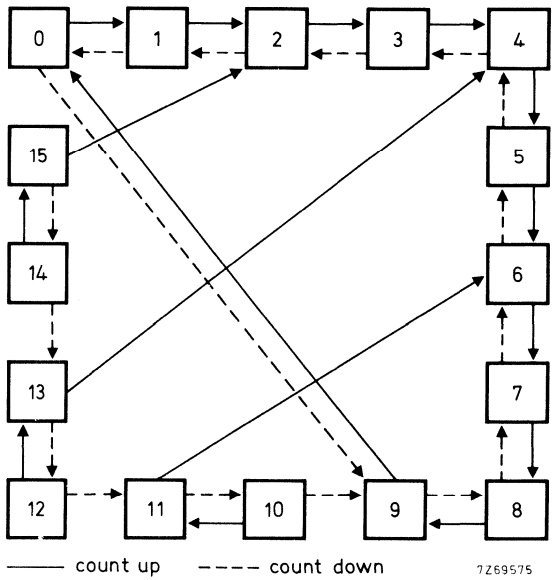


Fig. 4 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE}} \cdot \{ (UP/\overline{DN}) \cdot O_0 \cdot O_3 + \overline{(UP/\overline{DN})} \cdot \overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$11\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			155	310	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
CP → $\overline{TC}$	5			260	525	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		105	210	ns	94 ns + (0,23 ns/pF) C_L
	15			75	150	ns	67 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	115	ns	47 ns + (0,16 ns/pF) C_L
PL → O_n	5			125	255	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	85	ns	32 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
PL → $\overline{TC}$	5			250	500	ns	223 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		110	220	ns	99 ns + (0,23 ns/pF) C_L
	15			80	160	ns	72 ns + (0,16 ns/pF) C_L
	5			250	500	ns	223 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		110	220	ns	99 ns + (0,23 ns/pF) C_L
	15			80	160	ns	72 ns + (0,16 ns/pF) C_L
$\overline{CE}$ → $\overline{TC}$	5			165	330	ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	135	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	125	ns	49 ns + (0,23 ns/pF) C_L
	15			45	95	ns	37 ns + (0,16 ns/pF) C_L
MR → O_n, $\overline{TC}$	5			205	405	ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	85	ns	37 ns + (0,16 ns/pF) C_L
MR → $\overline{TC}$	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Output transition times	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
Minimum clock pulse width; LOW	5		95	45	ns	
	10	t_{WCPL}	35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5		105	55	ns	
	10	t_{WPLH}	45	25	ns	
	15		35	15	ns	
Minimum MR pulse width; HIGH	5		120	60	ns	
	10	t_{WMRH}	50	25	ns	
	15		40	20	ns	
Recovery time for MR	5		130	65	ns	
	10	t_{RMR}	45	20	ns	
	15		30	15	ns	
Recovery time for PL	5		150	75	ns	
	10	t_{RPL}	50	25	ns	
	15		30	15	ns	
Set-up times $P_n \longrightarrow$ PL	5		100	50	ns	
	10	t_{su}	50	25	ns	
	15		40	20	ns	see also waveforms Figs 5 and 6
	5		250	125	ns	
UP/$\overline{DN}$ $\longrightarrow$ CP	10	t_{su}	100	50	ns	
	15		75	35	ns	
	5		120	60	ns	
$\overline{CE}$ $\longrightarrow$ PL	10	t_{su}	40	20	ns	
	15		25	10	ns	
Hold times $P_n \longrightarrow$ PL	5		10	−40	ns	
	10	t_{hold}	5	−20	ns	
	15		0	−20	ns	
	5		35	−90	ns	
UP/$\overline{DN}$ $\longrightarrow$ CP	10	t_{hold}	15	−35	ns	
	15		15	−25	ns	
	5		20	−40	ns	
$\overline{CE}$ $\longrightarrow$ CP	10	t_{hold}	5	−15	ns	
	15		5	−10	ns	
Maximum clock pulse frequency	5		5	10	MHz	
	10	f_{max}	12	24	MHz	
	15		17	34	MHz	

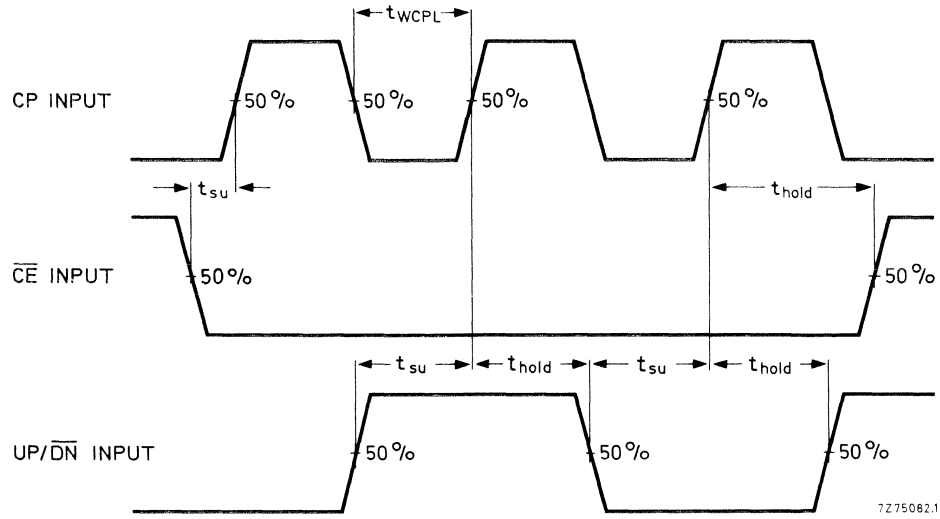


Fig. 5 Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP.

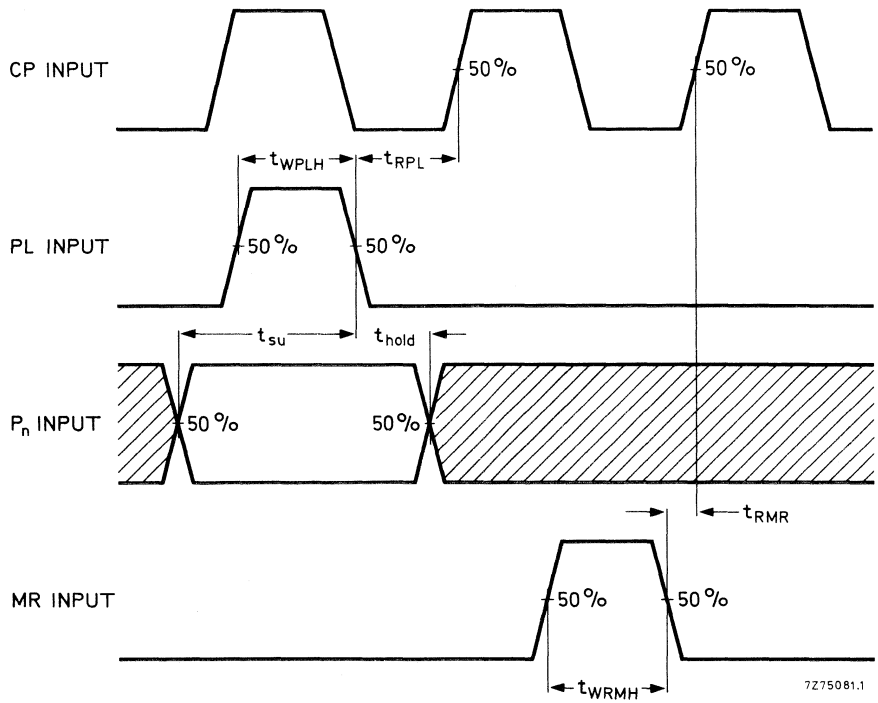


Fig. 6 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

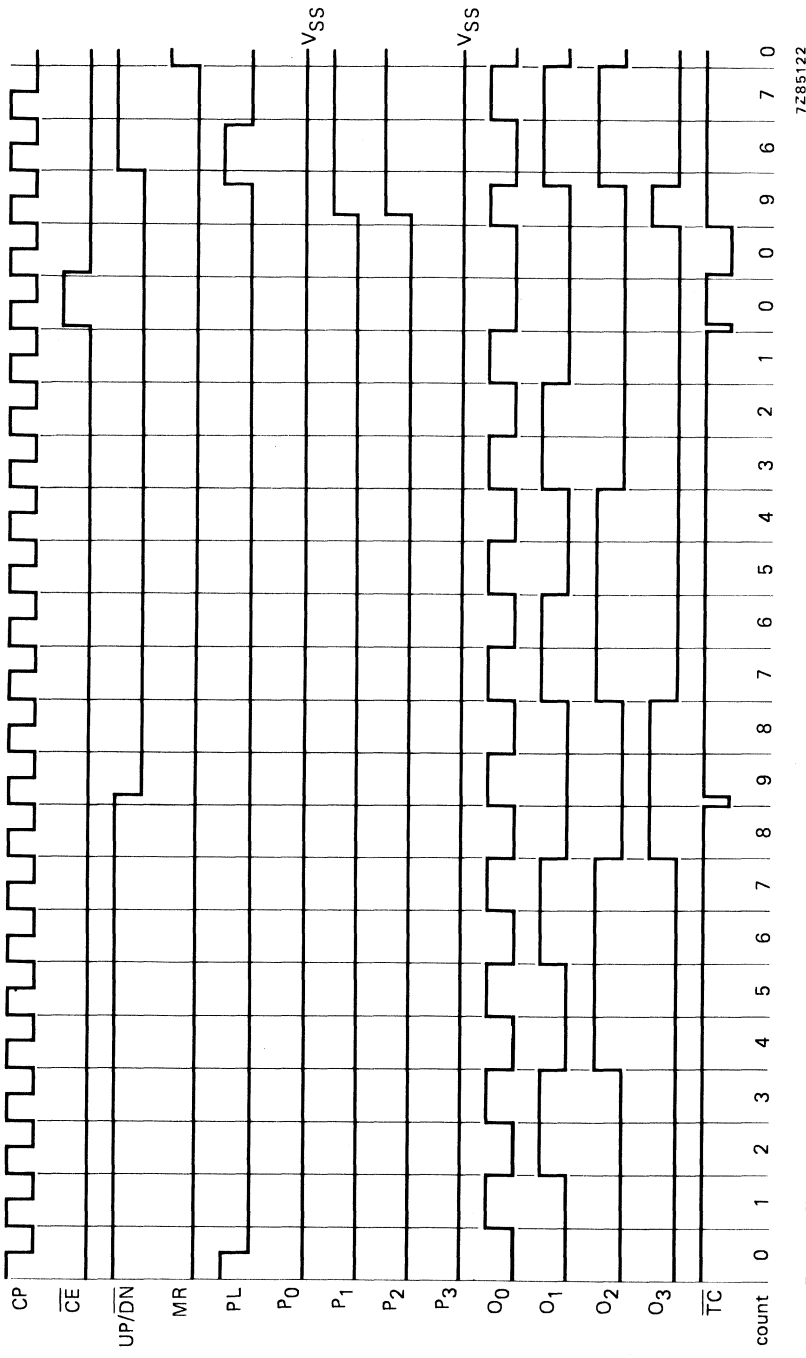


Fig. 7 Timing diagram.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

The HEF4511B is a BCD to 7-segment latch/decoder/driver with four address inputs (D_A to D_D), an active LOW latch enable input ($\overline{EL}$), an active LOW ripple blanking input ($\overline{BI}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH n-p-n bipolar transistor segment outputs (O_a to O_g).

When $\overline{EL}$ is LOW, the state of the segment outputs (O_a to O_g) is determined by the data on D_A to D_D. When $\overline{EL}$ goes HIGH, the last data present on D_A to D_D are stored in the latches and the segment outputs remain stable. When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.

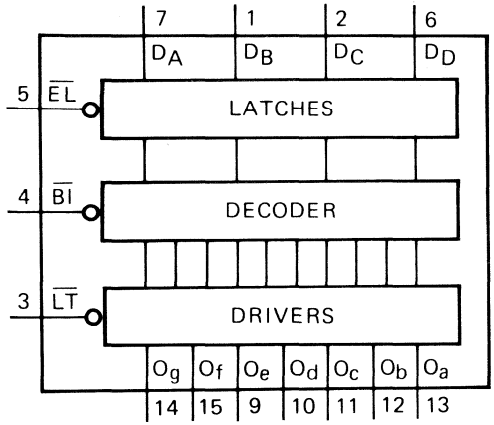


Fig. 1 Functional diagram.

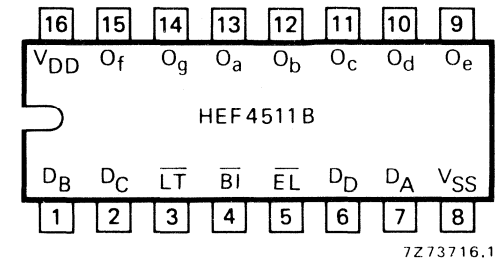


Fig. 2 Pinning diagram.

HEF4511BP : 16-lead DIL; plastic (SOT-38Z).
HEF4511BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4511BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_A to D_D	address (data) inputs
$\overline{EL}$	latch enable input (active LOW)
$\overline{BI}$	ripple blanking input (active LOW)
$\overline{LT}$	lamp test input (active LOW)
O_a to O_g	segment outputs

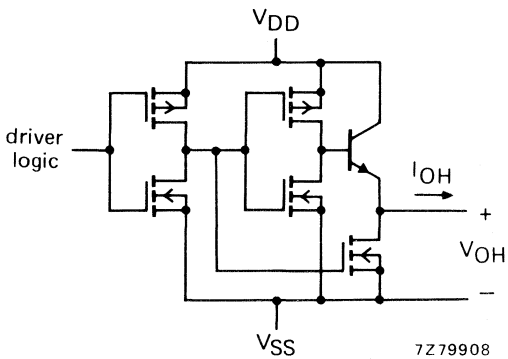


Fig. 3 Schematic diagram of output stage.

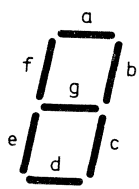


Fig. 4 Segment designation.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

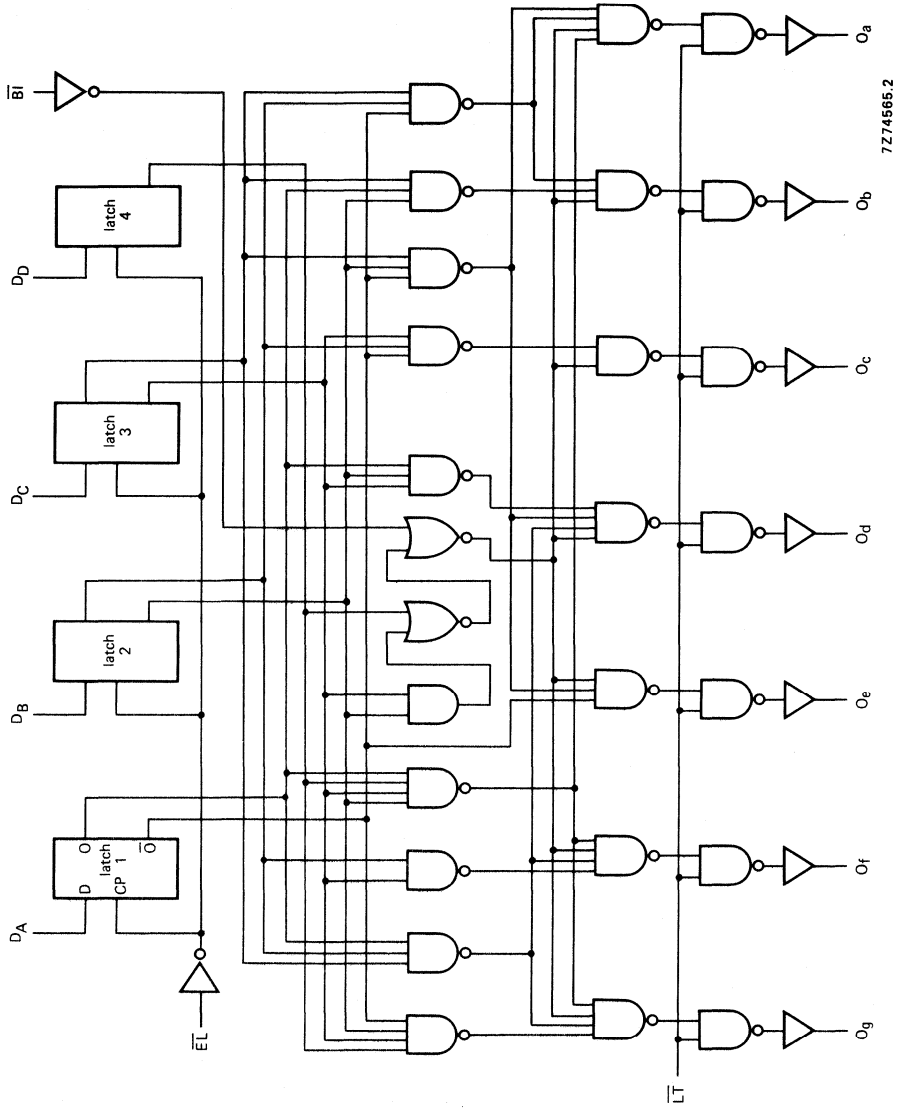


Fig. 5 Logic diagram; for one latch see Fig. 6.

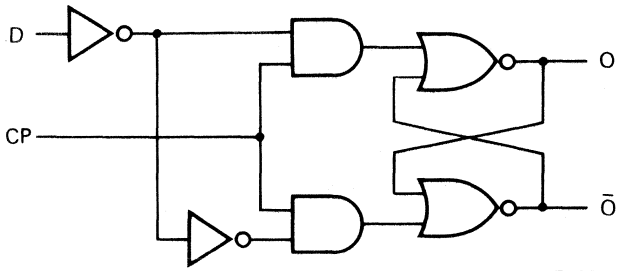


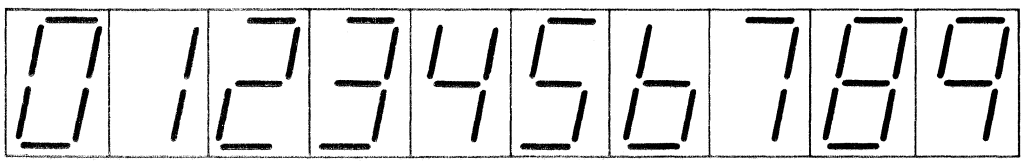
Fig. 6 Logic diagram (one latch); see also Fig. 5. 7Z79901

FUNCTION TABLE

inputs							outputs							
$\overline{EL}$	$\overline{BI}$	$\overline{LT}$	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X				*				*

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* Depends upon the BCD code applied during the LOW to HIGH transition of $\overline{EL}$.



7Z72856

Fig. 7 Display.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Output (source) current HIGH $-I_{OH}$ max. 25 mA

For other RATINGS see Family Specifications.

Note

A destructive high current mode may occur if V_I and V_O are not constrained to the range $V_{SS} \leqslant V_I$ or $V_O \leqslant V_{DD}$.

D.C. CHARACTERISTICS

V_{SS} = 0 V

HEF	V_{DD} V	I_{OH} mA	symbol	T_{amb} (°C) −40 min.	−40 max.	+ 25 min.	+ 25 typ.	+ 85 min.	+ 85 max.	
Output voltage HIGH	5	0	V_{OH}	4,10		4,10	4,40	4,10		V
	10	0		9,10		9,10	9,40	9,10		V
	15	0		14,10		14,10	14,40	14,10		V
Output voltage HIGH	5	5	V_{OH}				4,20			V
	10	5					9,20			V
	15	5					14,20			V
Output voltage HIGH	5	10	V_{OH}	3,60		3,60	4,05	3,30		V
	10	10		8,75		8,75	9,10	8,45		V
	15	10		13,75		13,75	14,10	13,45		V
Output voltage HIGH	5	15	V_{OH}				4,00			V
	10	15					9,00			V
	15	15					14,00			V
Output voltage HIGH	5	20	V_{OH}	2,80		2,80	3,80	2,50		V
	10	20		8,10		8,10	9,00	7,80		V
	15	20		13,10		13,10	14,00	12,80		V
Output voltage HIGH	5	25	V_{OH}				3,70			V
	10	25					8,90			V
	15	25					14,00			V

HEC	V_{DD} V	I_{OH} mA	symbol	T_{amb} (°C) −55 min.	−55 max.	+ 25 min.	+ 25 typ.	+ 125 min.	+ 125 max.	
Output voltage HIGH	5	0	V_{OH}	4,10		4,10	4,40	4,10		V
	10	0		9,10		9,10	9,90	9,10		V
	15	0		14,10		14,10	14,40	14,40		V
Output voltage HIGH	5	5	V_{OH}				4,30			V
	10	5					9,30			V
	15	5					14,30			V
Output voltage HIGH	5	10	V_{OH}	3,60		3,60	4,25	3,20		V
	10	10		8,75		8,75	9,25	8,35		V
	15	10		13,75		13,75	14,25	13,35		V

D.C. CHARACTERISTICS (continued)

HEC	V_{DD} V	I_{OH} mA	symbol	T_{amb} (°C) −55 min.	−55 max.	+ 25 min.	+ 25 typ.	+125 min.	+125 max.	
Output voltage HIGH	5	15	V_{OH}				4,20			V
	10	15					9,20			V
	15	15					14,20			V
Output voltage HIGH	5	20	V_{OH}	2,80		2,80	4,20	2,30		V
	10	20		8,10		8,10	9,20	7,60		V
	15	20		13,10		13,10	14,20	12,60		V
Output voltage HIGH	5	25	V_{OH}				4,15			V
	10	25					9,20			V
	15	25					14,20			V

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
$D_n \rightarrow O_n$	5			155	310 ns	128 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			135	270 ns	108 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
$\overline{EL} \rightarrow O_n$	5			160	320 ns	133 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
	5			160	320 ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
$\overline{BI} \rightarrow O_n$	5			120	240 ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS (continued)

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays (cont.)							
$\overline{BI} \rightarrow O_n$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{LT} \rightarrow O_n$	5			80	160	ns	52 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
	5			60	120	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			25	50	ns	20 ns + (0,1 na/Pf) C_L
LOW to HIGH	10	t_{TLH}		16	32	ns	13 ns + (0,06 ns/pF) C_L
	15			13	26	ns	10 ns + (0,06 ns/pF) C_L
Minimum $\overline{EL}$	5		80	40		ns	
pulse width; LOW	10	t_{WELL}	40	20		ns	
	15		35	17		ns	
Set-up time	5		50	25		ns	
$D_n \rightarrow \overline{EL}$	10	t_{su}	25	12		ns	see also waveforms Fig. 8
	15		20	9		ns	
Hold-time	5		60	30		ns	
$D_n \rightarrow \overline{EL}$	10	t_{hold}	30	15		ns	
	15		25	12		ns	

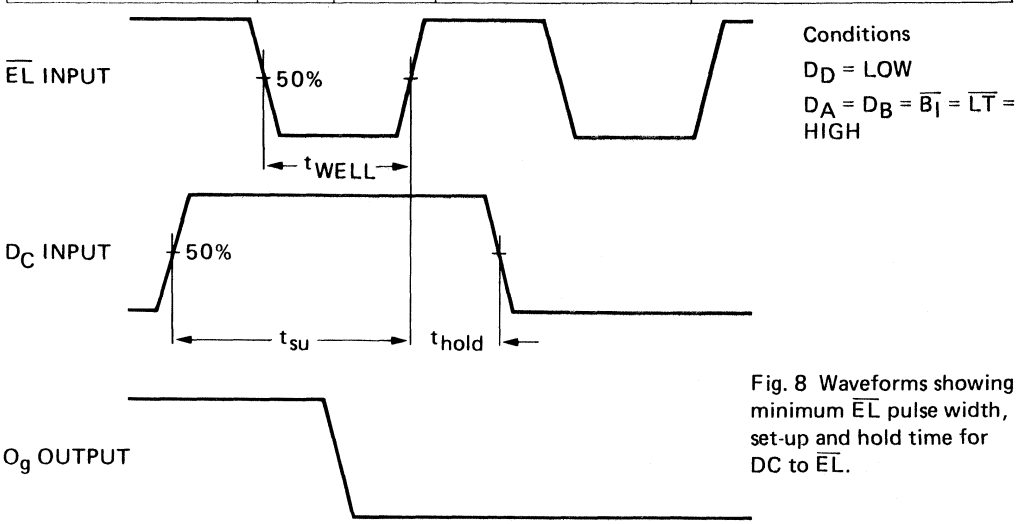


Fig. 8 Waveforms showing minimum $\overline{EL}$ pulse width, set-up and hold time for DC to $\overline{EL}$.

APPLICATION INFORMATION

Some examples of applications for the HEF4511B are:

- Driving LED displays.
- Driving incandescent displays.
- Driving fluorescent displays.
- Driving LCD displays.
- Driving gas discharge displays.

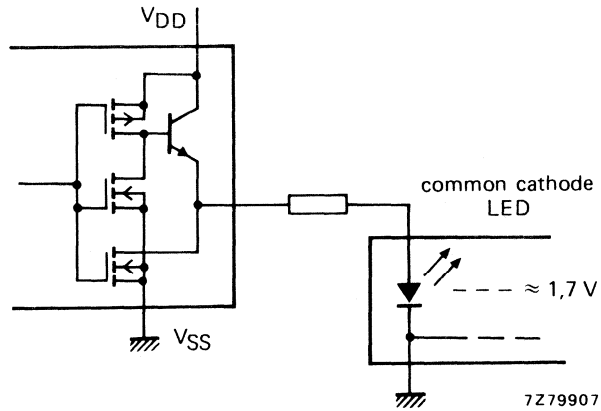


Fig. 9 Connection to common cathode LED display readout.

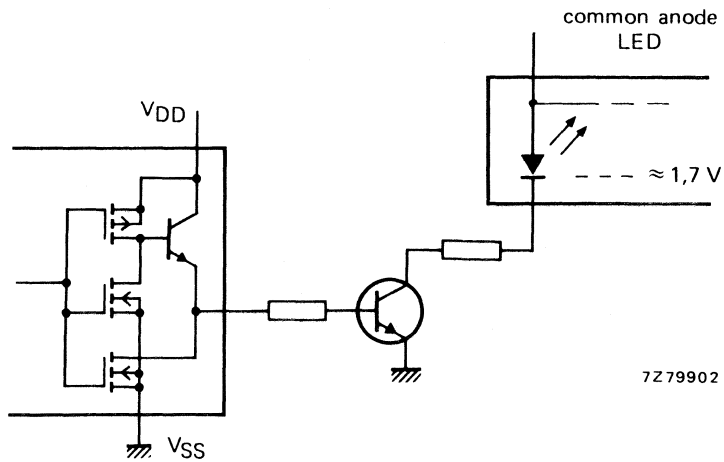
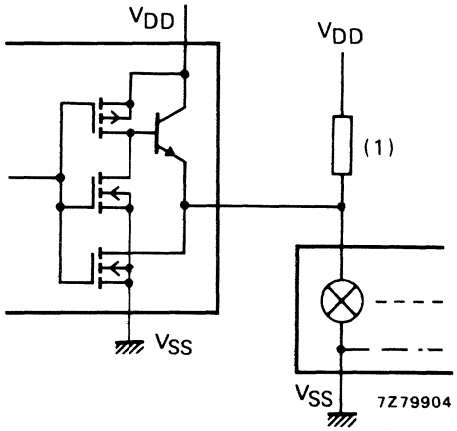


Fig. 10 Connection to common anode LED display readout.



(1) A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Fig. 11 Connection to incandescent display readout.

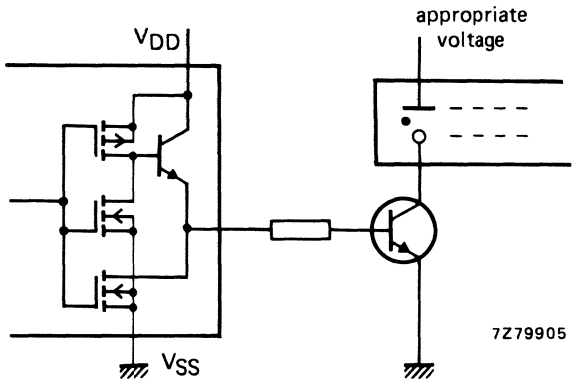


Fig. 13 Connection to gas discharge display readout.

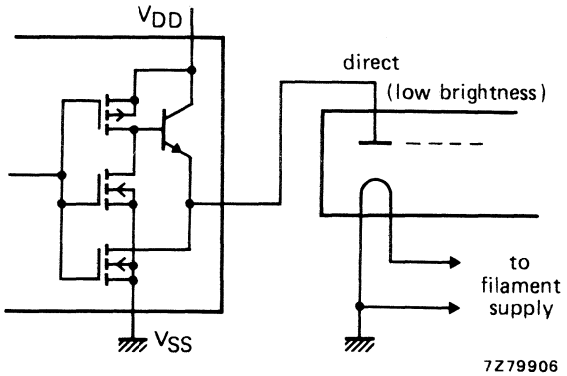


Fig. 12 Connection to fluorescent display readout.

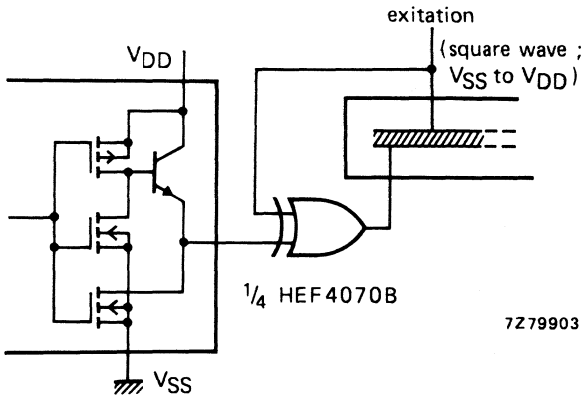


Fig. 14 Connection to liquid crystal (LCD) display readout.
Direct d.c. drive of LCDs not recommended for life of LCD readouts.

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUT

The HEF4512B is an 8-input multiplexer with 8 binary inputs (I_0 to I_7), an enable input ($\overline{E}$) and an output enable input ($\overline{EO}$). One of eight binary inputs is selected by select inputs S_0, S_1 and S_2, and is routed to the output O. A HIGH on $\overline{EO}$ causes O to assume a high impedance OFF-state, regardless of other input conditions. This allows the output to interface directly with bus oriented systems (3-state). When the active LOW enable ($\overline{E}$) is HIGH, it forces the output LOW provided $\overline{EO}$ is LOW. By proper manipulation of the inputs, the device can provide any logic functions of four variables. It cannot be used to multiplex analogue signals.

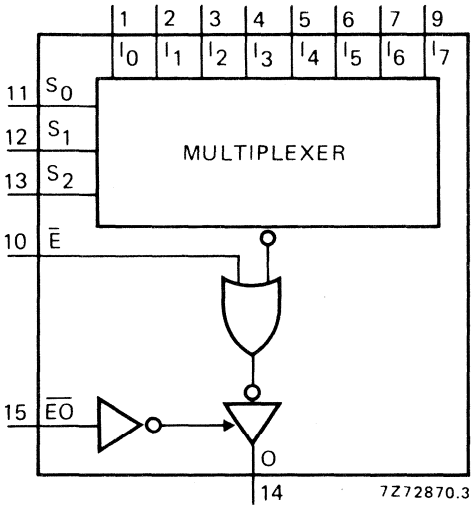


Fig. 1 Functional diagram.

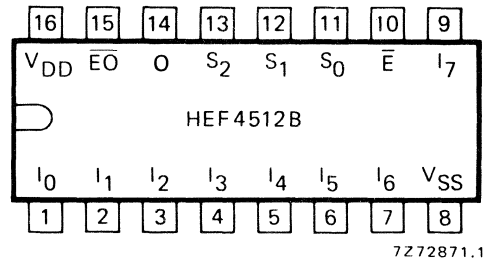


Fig. 2 Pinning diagram.

HEF4512BP : 16-lead DIL; plastic (SOT-38Z).
HEF4512BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4512BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

S_0, S_1, S_2	select inputs
$\overline{EO}$	output enable (active LOW)
$\overline{E}$	enable (active LOW)
I_0 to I_7	multiplexer inputs
O	multiplexer output

FAMILY DATA

I_{DD} LIMITS category MSI | see Family Specifications

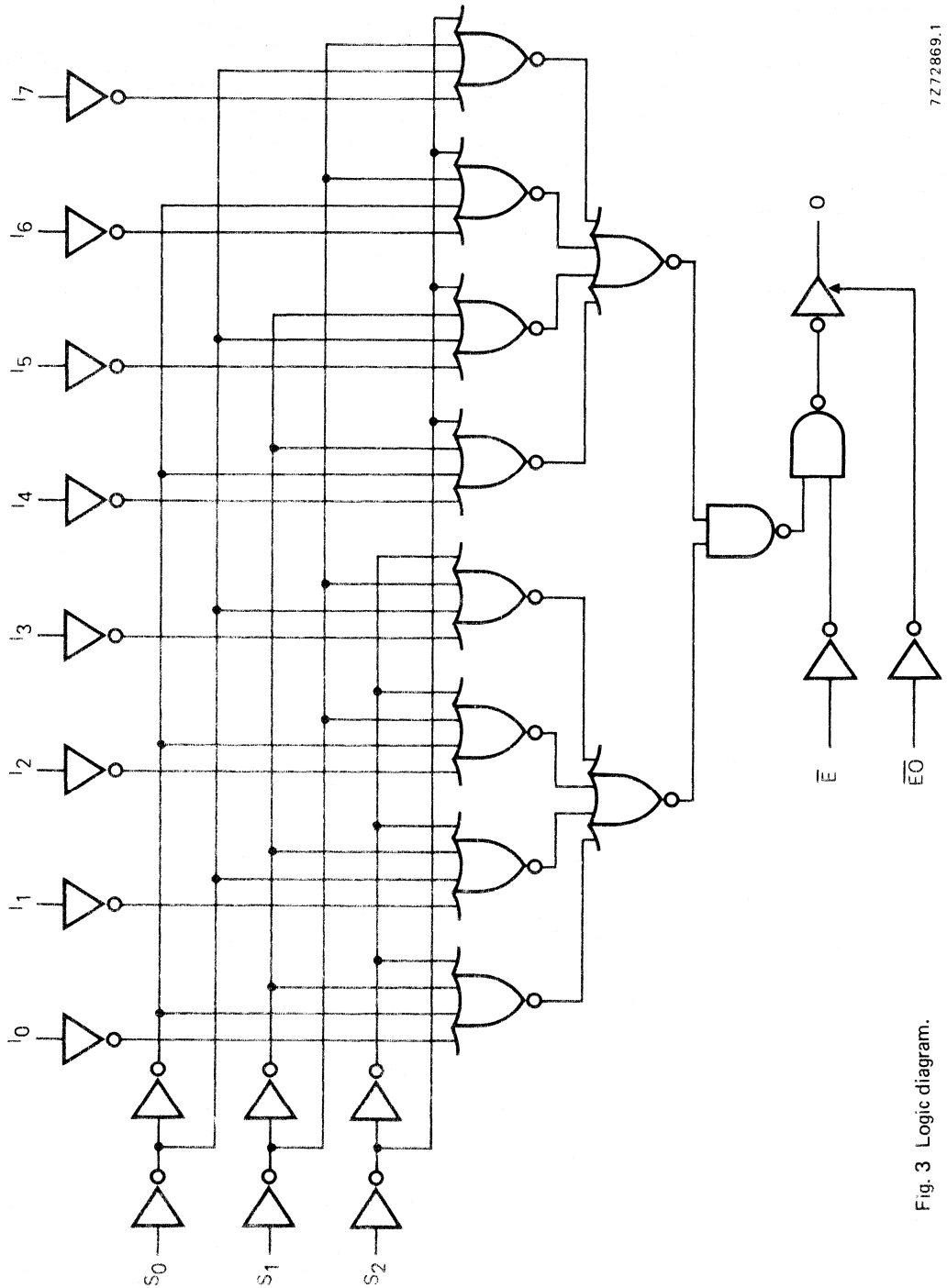


Fig. 3 Logic diagram.

TRUTH TABLE

inputs													output
$\overline{EO}$	$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	O
L	H	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	L	L	H	X	L	X	X	X	X	X	X	L
L	L	L	L	H	X	H	X	X	X	X	X	X	H
L	L	L	H	L	X	X	L	X	X	X	X	X	L
L	L	L	H	L	X	X	H	X	X	X	X	X	H
L	L	L	H	H	X	X	X	L	X	X	X	X	L
L	L	L	H	H	X	X	X	H	X	X	X	X	H
L	L	H	L	L	X	X	X	X	L	X	X	X	L
L	L	H	L	L	X	X	X	X	H	X	X	X	H
L	L	H	L	H	X	X	X	X	X	L	X	X	L
L	L	H	L	H	X	X	X	X	X	H	X	X	H
L	L	H	H	L	X	X	X	X	X	X	L	X	L
L	L	H	H	L	X	X	X	X	X	X	H	X	H
L	L	H	H	H	X	X	X	X	X	X	X	L	L
L	L	H	H	H	X	X	X	X	X	X	X	H	H
H	X	X	X	X	X	X	X	X	X	X	X	X	Z

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance OFF-state

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$5800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

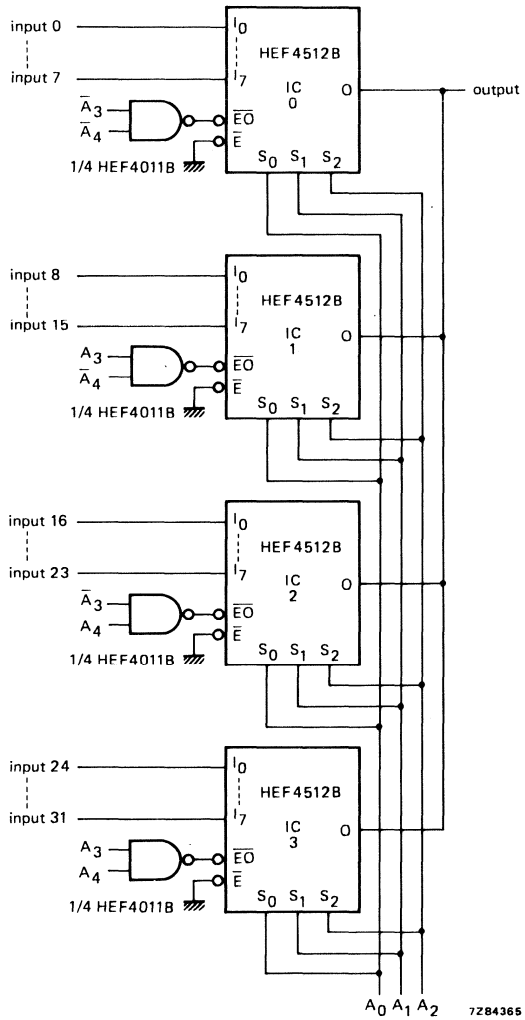
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
I_n → O	5		100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		100	200	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
S_n → O	5		140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	55	110	ns	44 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
	5		150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	60	120	ns	49 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{E}$ → O	5		60	120	ns	33 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		55	110	ns	28 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays						
Output disable times						
$\overline{EO}$ → O	5		35	70	ns	
HIGH	10	t_{PHZ}	20	40	ns	
	15		15	30	ns	
	5		35	70	ns	
LOW	10	t_{PLZ}	15	30	ns	
	15		10	20	ns	
Output enable times						
$\overline{EO}$ → O	5		35	70	ns	
HIGH	10	t_{PZH}	15	30	ns	
	15		10	20	ns	
	5		35	70	ns	
LOW	10	t_{PZL}	20	40	ns	
	15		15	30	ns	

APPLICATION INFORMATION

Some examples of applications for the HEF4512B are:

- Signal gating
- Digital multiplexing
- Number sequence generation



TRUTH TABLE for Fig. 4

A_4	A_3	A_2	A_1	A_0	input conn. to output	
L	L	L	L	L	0	via IC 0
L	L	L	L	H	1	
L	L	L	H	L	2	
L	L	L	H	H	3	
L	L	H	L	L	4	
L	L	H	L	H	5	
L	L	H	H	L	6	
L	L	H	H	H	7	
L	H	L	L	L	8	via IC 1
L	H	L	L	H	9	
L	H	L	H	L	10	
L	H	L	H	H	11	
L	H	H	L	L	12	
L	H	H	L	H	13	
L	H	H	H	L	14	
L	H	H	H	H	15	
H	L	L	L	L	16	via IC 2
H	L	L	L	H	17	
H	L	L	H	L	18	
H	L	L	H	H	19	
H	L	H	L	L	20	
H	L	H	L	H	21	
H	L	H	H	L	22	
H	L	H	H	H	23	
H	H	L	L	L	24	via IC 3
H	H	L	L	H	25	
H	H	L	H	L	26	
H	H	L	H	H	27	
H	H	H	L	L	28	
H	H	H	L	H	29	
H	H	H	H	L	30	
H	H	H	H	H	31	

Fig. 4 32-input multiplexer using 4 x HEF4512B and 1 x HEF4011B. The input is selected by 5-bit address (A_4 to A_0) and presented at the output.

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCHES

The HEF4514B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input ($\overline{E}$). The 16 outputs (O_0 to O_{15}) are mutually exclusive active HIGH. When EL is HIGH, the selected output is determined by the data on A_n. When EL goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input ($\overline{E}$) does not affect the state of the latch. When the HEF4514B is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

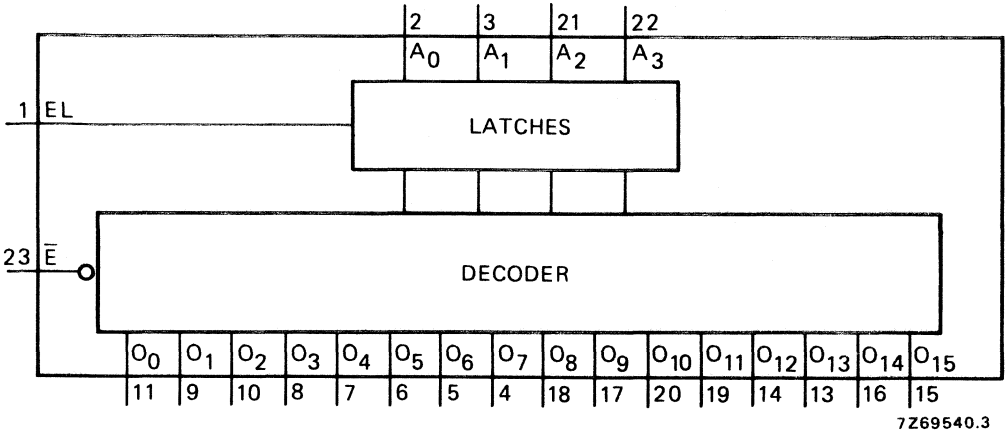


Fig. 1 Functional diagram.

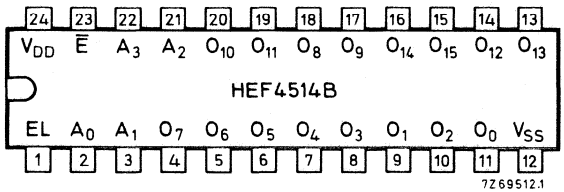


Fig. 2 Pinning diagram.

PINNING

A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
EL	latch enable input
O_0 to O_{15}	outputs (active HIGH)

HEF4514BP : 24-lead DIL; plastic (SOT-101A).
HEF4514BD: 24-lead DIL; ceramic (cerdip) (SOT-94).
HEF4514BT : 24-lead mini-pack; plastic (SO-24; SOT-137A).

APPLICATION INFORMATION

Some examples of applications for the HEF4514B are:

- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

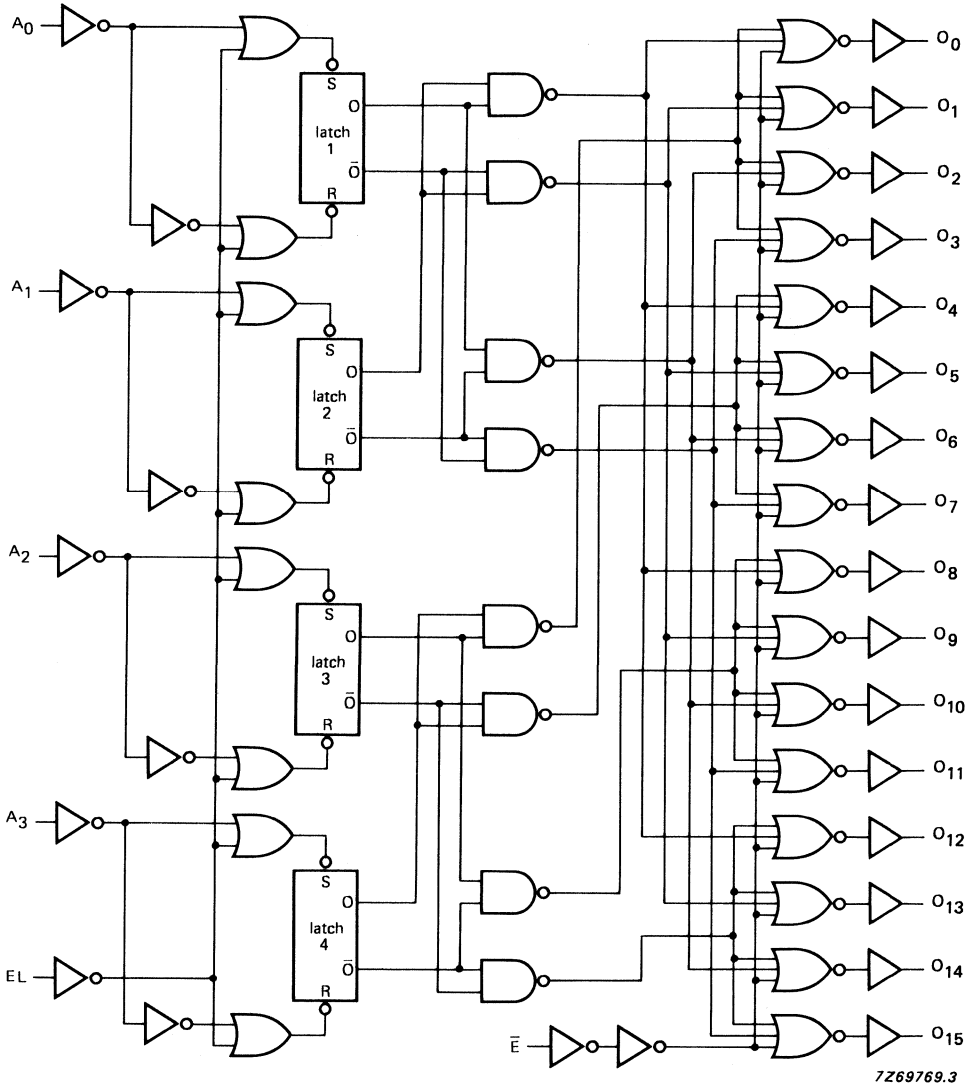


Fig. 3 Logic diagram.

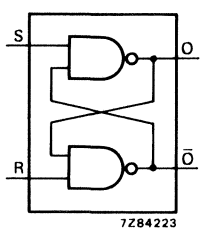


Fig. 4 Logic diagram (one latch).

TRUTH TABLE

inputs					outputs													
$\overline{E}$	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

EL = HIGH
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
A_n, EL → O_n	5		260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		270	550	ns	243 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
$\overline{E}$ → O_n	5		175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		200	400	ns	173 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times	5			90	180	ns	40 ns + (1,0 ns/pF) C_L
	10	t_{THL}		35	65	ns	14 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
	5			85	170	ns	35 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		35	70	ns	14 ns + (0,42 ns/pF) C_L
	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
Set-up time	5		120	60		ns	see also waveforms Fig. 5
A_n → EL	10	t_{su}	40	20		ns	
	15		30	15		ns	
Hold time	5		0	60		ns	
A_n → EL	10	t_{hold}	0	20		ns	
	15		0	15		ns	
Minimum EL pulse width; HIGH	5		120	60		ns	
	10	t_{WELH}	40	20		ns	
	15		30	15		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5500 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	16 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

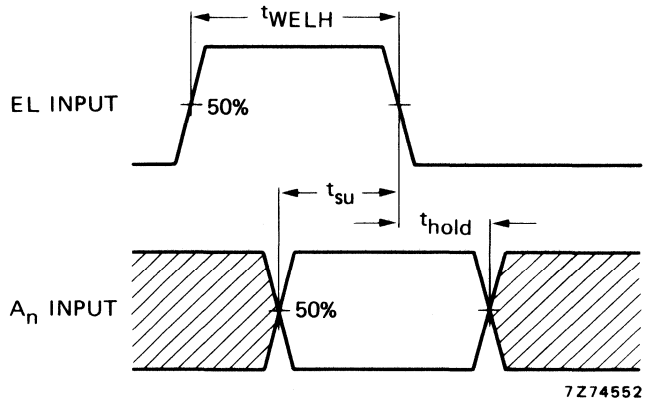


Fig. 5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL.
Set-up and hold times are shown as positive values but may be specified as negative values.

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCHES

The HEF4515B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input ($\overline{E}$). The 16 outputs ($\overline{O}_0$ to $\overline{O}_{15}$) are mutually exclusive active LOW. When EL is HIGH, the selected output is determined by the data on A_n. When EL goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is LOW. At $\overline{E}$ HIGH, all outputs are HIGH. The enable input ($\overline{E}$) does not affect the state of the latch. When the HEF 4515B is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

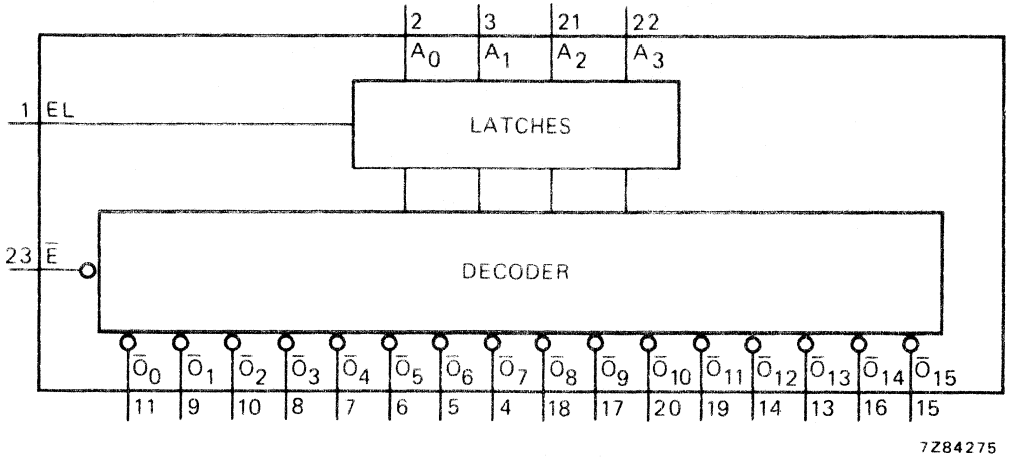
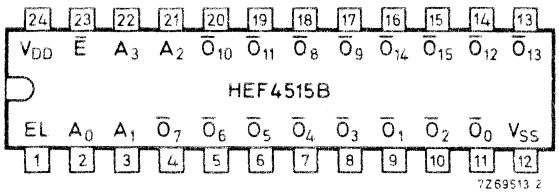


Fig. 1 Functional diagram.



PINNING

A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
EL	latch enable input
$\overline{O}_0$ to $\overline{O}_{15}$	outputs (active LOW)

Fig. 2 Pinning diagram.

HEF4515BP : 24-lead DIL; plastic (SOT-101A).
HEF4515BD: 24-lead DIL; ceramic (cerdip) (SOT-94).
HEF4515BT : 24-lead mini-pack; plastic (SO-24; SOT-137A).

APPLICATION INFORMATION

Some examples of applications for the HEF4515B are:

- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

FAMILY DATA

I_{DD} LIMITS category MSI | see Family Specifications

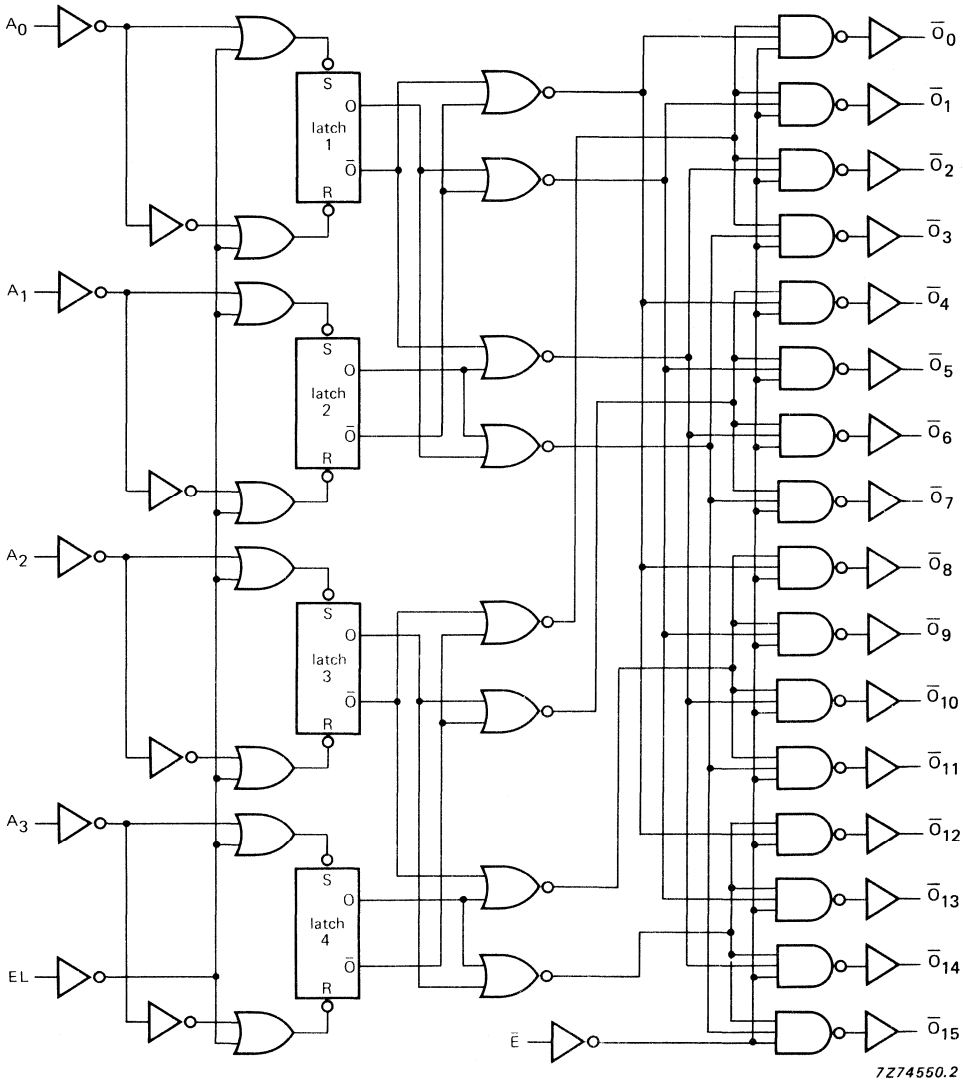


Fig. 3 Logic diagram.

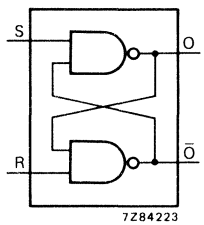


Fig. 4 Logic diagram (one latch).

TRUTH TABLE

inputs					outputs													
$\overline{E}$	A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$	$\overline{O}_{10}$	$\overline{O}_{11}$	$\overline{O}_{12}$	$\overline{O}_{13}$	$\overline{O}_{14}$	$\overline{O}_{15}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

EL = HIGH
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
A_n, EL → $\overline{O}_n$	5		260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		270	550	ns	243 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
$\overline{E}$ → $\overline{O}_n$	5		175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		200	400	ns	173 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times	5			90	180	ns	40 ns + (1,0 ns/pF) C_L
	10	t_{THL}		35	65	ns	14 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
	5			85	170	ns	35 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		35	70	ns	14 ns + (0,42 ns/pF) C_L
	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
Set-up time	5		120	60		ns	see also waveforms Fig. 5
A_n → EL	10	t_{su}	40	20		ns	
	15		30	15		ns	
Hold time	5		0	60		ns	
A_n → EL	10	t_{hold}	0	20		ns	
	15		0	15		ns	
Minimum EL pulse width; HIGH	5		120	60		ns	
	10	t_{WELH}	40	20		ns	
	15		30	15		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + Σ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5500 f_i + Σ($f_o C_L$) × V_{DD}^2	
	15	16 000 f_i + Σ($f_o C_L$) × V_{DD}^2	

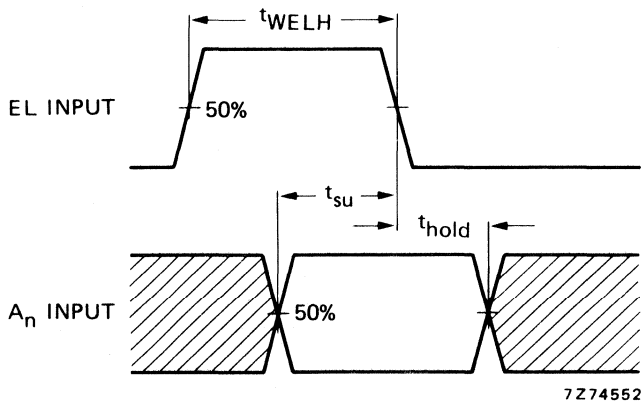


Fig. 5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as negative values.

BINARY UP/DOWN COUNTER

The HEF4516B is an edge-triggered synchronous up/down 4-bit binary counter with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR which must be LOW. When PL and $\overline{CE}$ are LOW, the counter changes on the LOW to HIGH transition of CP. Input UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when O_0 to O_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when O_0 to O_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of all other input conditions.

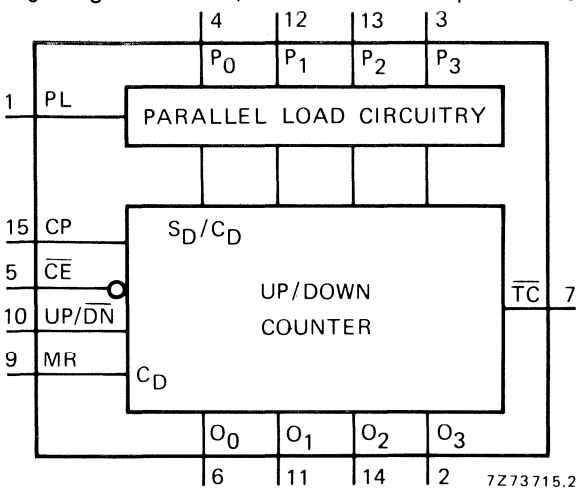


Fig. 1 Functional diagram.

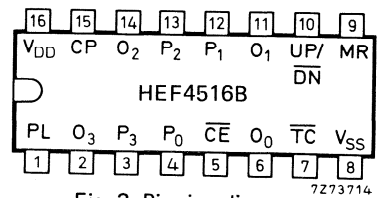


Fig. 2 Pinning diagram.

HEF4516BP : 16-lead DIL; plastic (SOT-38Z).
HEF4516BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4516BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

PL	parallel load input (active HIGH)	UP/$\overline{DN}$	up/down count control input
P_0 to P_3	parallel inputs	MR	master reset input
$\overline{CE}$	count enable input (active LOW)	$\overline{TC}$	terminal count output (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)	O_0 to O_3	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Products approved to CECC 90 104-069.

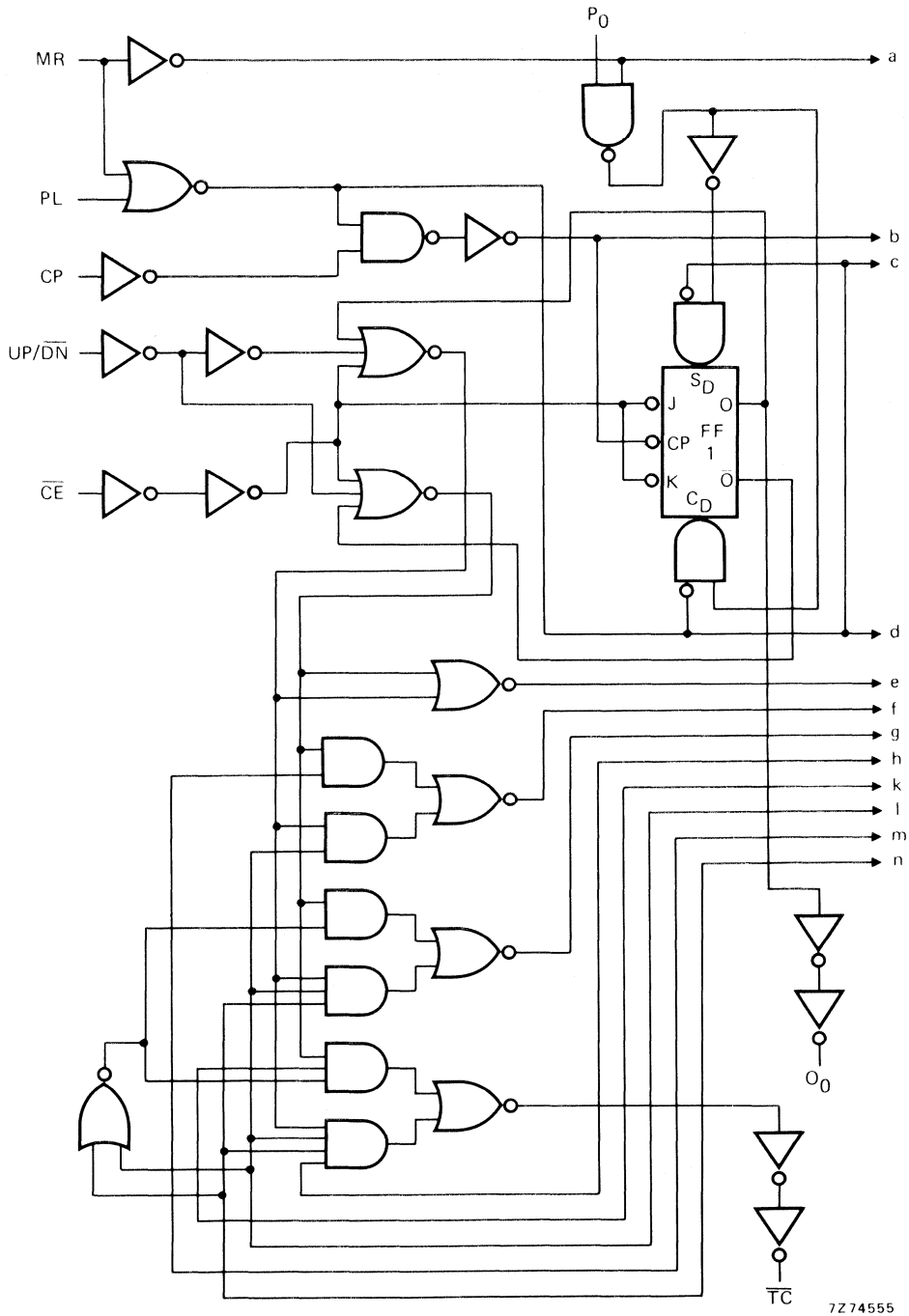


Fig. 3a Logic diagram (continued in Fig. 3b).

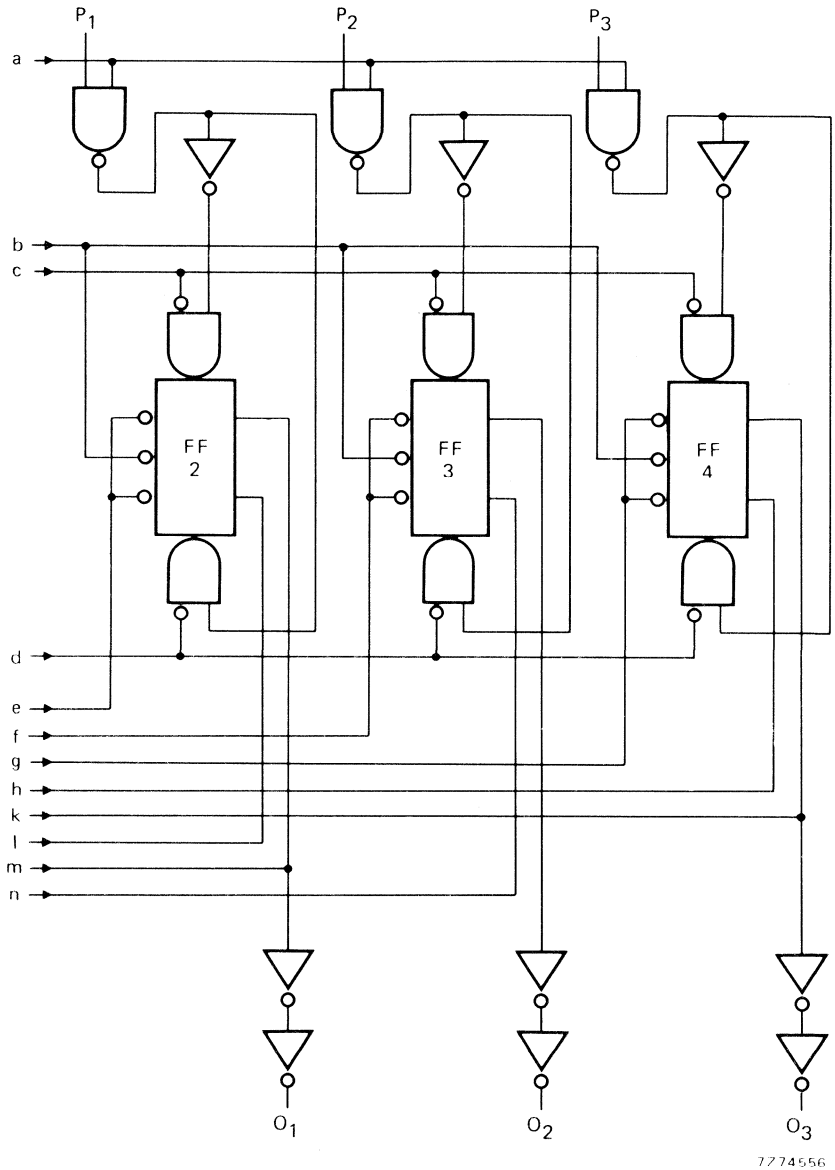


Fig. 3b Logic diagram (continued from Fig. 3a).

FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	∫	count down
L	L	H	L	∫	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition

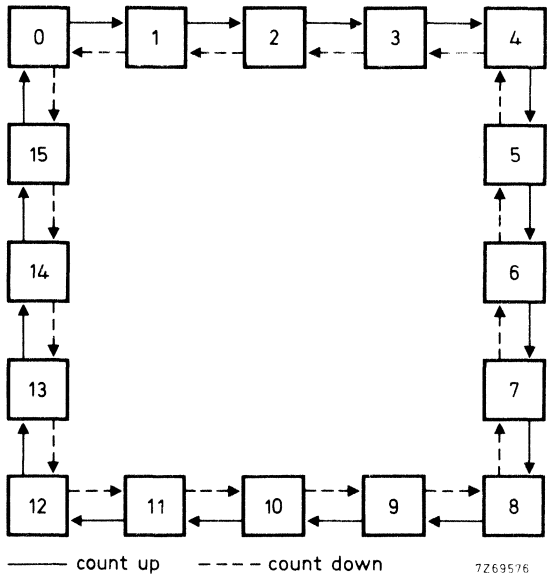


Fig. 4 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE}} \cdot \{(UP/\overline{DN}) \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3 + \overline{(UP/\overline{DN})} \cdot \overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3\}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1000 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	4500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	11 200 f_i + Σ($f_o C_L$) x V_{DD}^2	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP → O_n	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
	5			155	310 ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
CP → $\overline{TC}$	5			260	525 ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		105	210 ns	94 ns + (0,23 ns/pF) C_L
	15			75	150 ns	67 ns + (0,16 ns/pF) C_L
	5			180	360 ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			55	115 ns	47 ns + (0,16 ns/pF) C_L
PL → O_n	5			125	255 ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	85 ns	32 ns + (0,16 ns/pF) C_L
	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	105 ns	42 ns + (0,16 ns/pF) C_L
PL → $\overline{TC}$	5			250	500 ns	223 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		110	220 ns	99 ns + (0,23 ns/pF) C_L
	15			80	160 ns	72 ns + (0,16 ns/pF) C_L
	5			250	500 ns	223 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		110	220 ns	99 ns + (0,23 ns/pF) C_L
	15			80	160 ns	72 ns + (0,16 ns/pF) C_L
$\overline{CE}$ → $\overline{TC}$	5			165	330 ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	135 ns	54 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	125 ns	49 ns + (0,23 ns/pF) C_L
	15			45	95 ns	37 ns + (0,16 ns/pF) C_L
MR → O_n, $\overline{TC}$	5			205	405 ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	85 ns	37 ns + (0,16 ns/pF) C_L
MR → $\overline{TC}$	5			225	450 ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum clock pulse width; LOW	5		95	45		ns	
	10	t_{WCPL}	35	20		ns	
	15		25	15		ns	
Minimum PL pulse width; HIGH	5		105	55		ns	
	10	t_{WPLH}	45	25		ns	
	15		35	15		ns	
Minimum MR pulse width; HIGH	5		120	60		ns	
	10	t_{WMRH}	50	25		ns	
	15		40	20		ns	
Recovery time for MR	5		130	65		ns	
	10	t_{RMR}	45	20		ns	
	15		30	15		ns	
Recovery time for PL	5		150	75		ns	
	10	t_{RPL}	50	25		ns	
	15		30	15		ns	
Set-up times $P_n \longrightarrow$ PL	5		100	50		ns	
	10	t_{su}	50	25		ns	
	15		40	20		ns	see also waveforms Figs 5 and 6
	5		250	125		ns	
UP/$\overline{DN}$ $\longrightarrow$ CP	10	t_{su}	100	50		ns	
	15		75	35		ns	
	5		120	60		ns	
$\overline{CE}$ $\longrightarrow$ CP	10	t_{su}	40	20		ns	
	15		25	10		ns	
Hold times $P_n \longrightarrow$ PL	5		10	−40		ns	
	10	t_{hold}	5	−20		ns	
	15		0	−20		ns	
	5		35	−90		ns	
UP/$\overline{DN}$ $\longrightarrow$ CP	10	t_{hold}	15	−35		ns	
	15		15	−25		ns	
	5		20	−40		ns	
$\overline{CE}$ $\longrightarrow$ CP	10	t_{hold}	5	−15		ns	
	15		5	−10		ns	
Maximum clock pulse frequency	5		3	6		MHz	
	10	f_{max}	7	14		MHz	
	15		9	18		MHz	

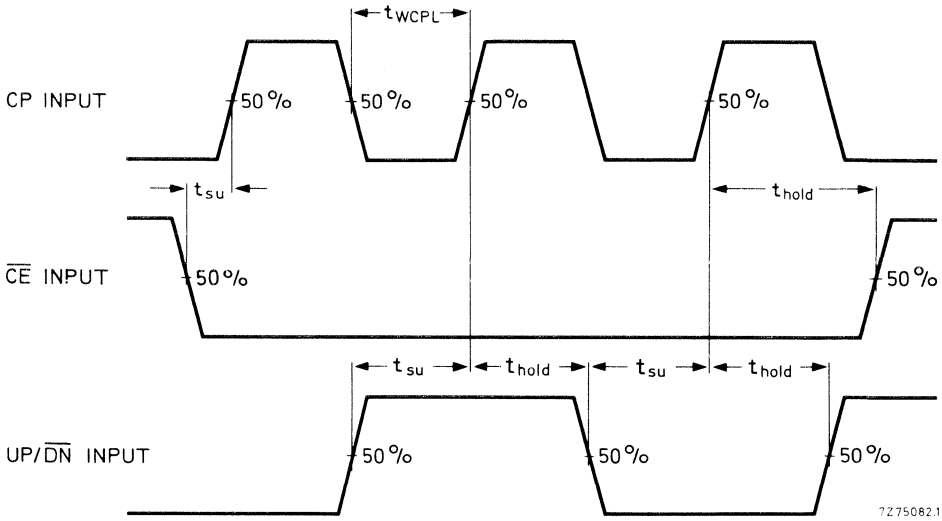


Fig. 5 Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP.

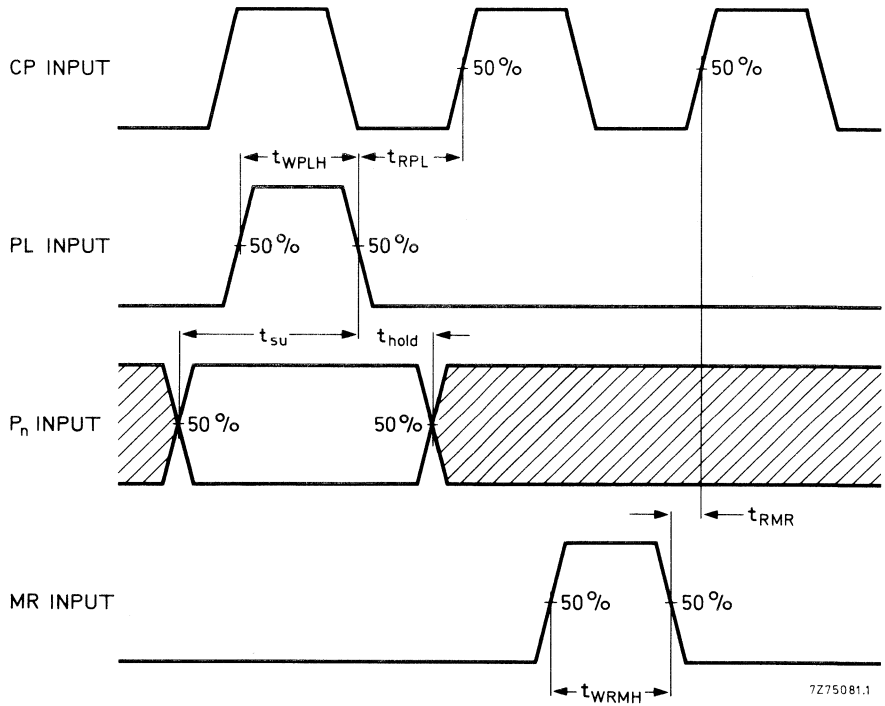


Fig. 6 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

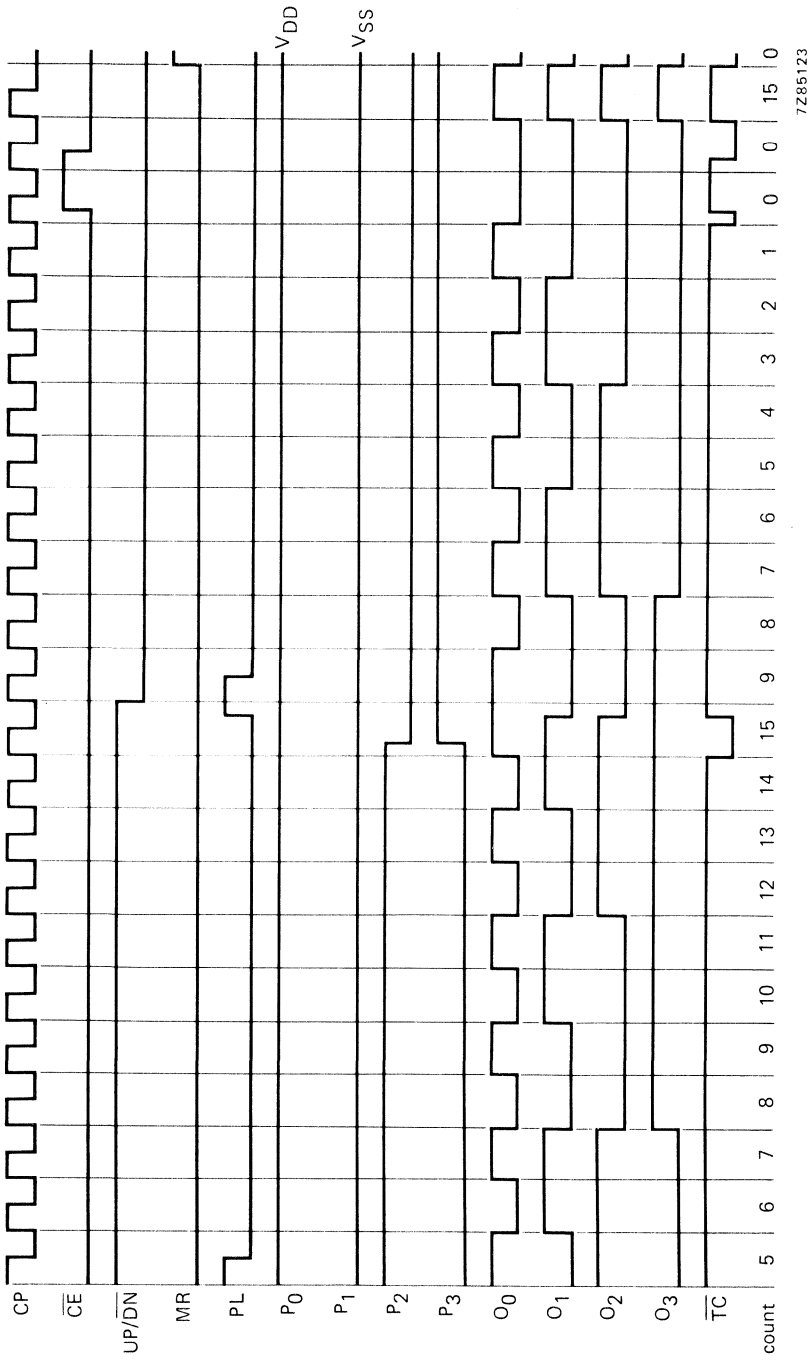


Fig. 7 Timing diagram.

DUAL 64-BIT STATIC SHIFT REGISTER

The HEF4517B consists of two identical, independent 64-bit static shift registers. Each register has separate clock (CP), data input (D), parallel input-enable/output-enable (PE/$\overline{EO}$) and four 3-state outputs of the 16th, 32nd, 48th and 64th bit positions (O_{16} to O_{64}). Data at the D input is entered into the first bit on the LOW to HIGH transition of the clock, regardless of the state of PE/$\overline{EO}$.

When PE/$\overline{EO}$ is LOW the outputs are enabled and the device is in the 64-bit serial mode.

When PE/$\overline{EO}$ is HIGH the outputs are disabled (high impedance OFF-state), the 64-bit shift register is divided into four 16-bit shift registers with D, O_{16}, O_{32} and O_{48} as data inputs of the 1st, 17th, 33rd, and 49th bit respectively. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

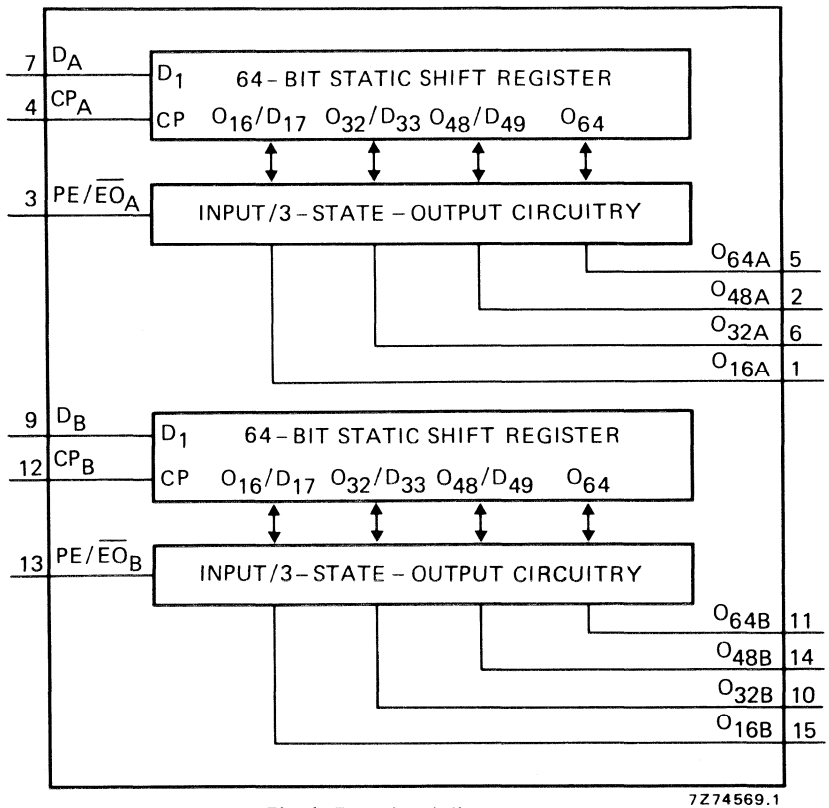


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

Products approved to CECC 90 104-070.

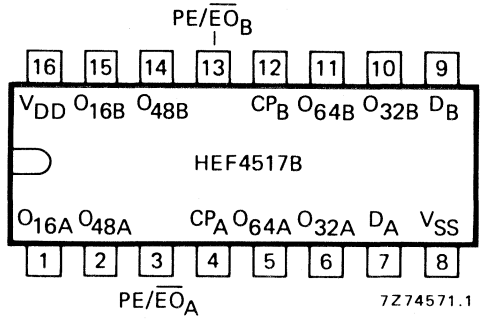


Fig. 2 Pinning diagram.

HEF4517BP : 16-lead DIL; plastic (SOT-38Z).
HEF4517BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4517BT : 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

CP_A, CP_B	clock inputs
PE/$\overline{EO}_A$, PE/$\overline{EO}_B$	parallel input-enable/output-enable inputs
D_A, D_B	data inputs
O_{16A}, O_{32A}, O_{48A}	3-state outputs/inputs
O_{16B}, O_{32B}, O_{48B}	3-state outputs/inputs
O_{64A}, O_{64B}	3-state outputs

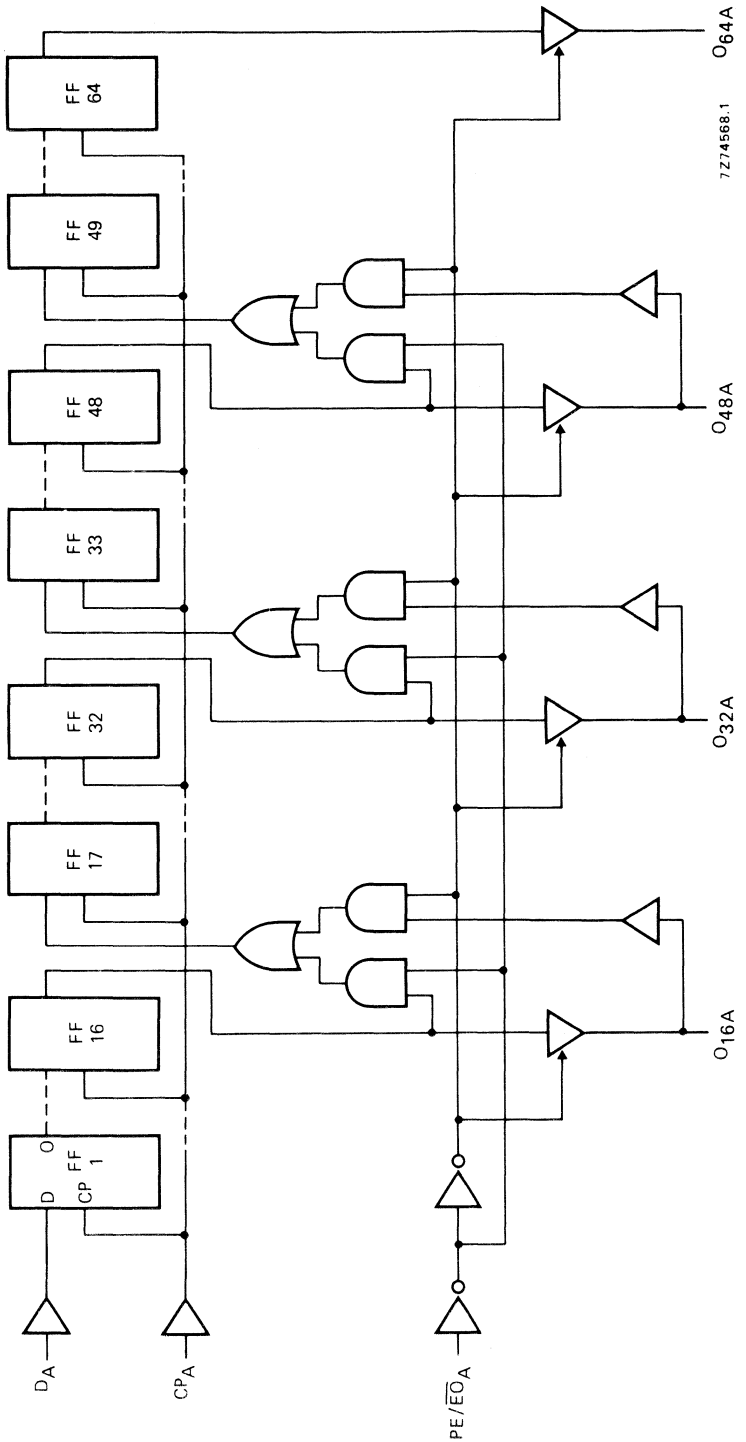


Fig. 3 Logic diagram (one shift register).

FUNCTION TABLE

inputs			inputs/outputs				mode
CP	D	PE/$\overline{EO}$	O_{16}	O_{32}	O_{48}	O_{64}	
∫	data entered into 1st bit	L	content of 16th bit displayed	content of 32nd bit displayed	content of 48th bit displayed	content of 64th bit displayed	One 64-bit shift register. The content of the shift register is shifted over one stage
∫	data entered into 1st bit	H	data at O_{16} entered into 17th bit	data at O_{32} entered into 33rd bit	data at O_{48} entered into 49th bit	remains in 'Z' state	Four 16-bit shift register. The content of the shift registers is shifted over one stage.
⎽\	X	L	no change	no change	no change	no change	no change
⎽\	X	H	Z	Z	Z	Z	no change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance state
∫ = positive-going transition
⎽\ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$7\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$28\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$70\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			220	440	ns	193 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			190	380	ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; LOW	5	t_{WCPL}		95	190	ns	see also waveforms Fig. 4.
	10			40	80	ns	
	15			30	60	ns	
Set-up times O_n, D ⟶ CP	5	t_{su}	30	10		ns	
	10		25	5		ns	
	15		20	5		ns	
Hold time O_n, D ⟶ CP	5	t_{hold}	45	15		ns	
	10		30	10		ns	
	15		25	10		ns	
3-state propagation delays							
Output disable times							
PE/$\overline{EO}$ ⟶ O_n HIGH	5	t_{PHZ}		40	80	ns	
	10			30	60	ns	
	15			25	50	ns	
LOW	5	t_{PLZ}		50	100	ns	
	10			30	60	ns	
	15			25	50	ns	
Output enable times							
PE/$\overline{EO}$ ⟶ O_n HIGH	5	t_{PZH}		45	90	ns	
	10			25	50	ns	
	15			20	40	ns	
LOW	5	t_{PZL}		60	120	ns	
	10			30	60	ns	
	15			25	50	ns	
Maximum clock pulse frequency	5	f_{max}	2	5		MHz	
	10		6	12		MHz	
	15		8	16		MHz	

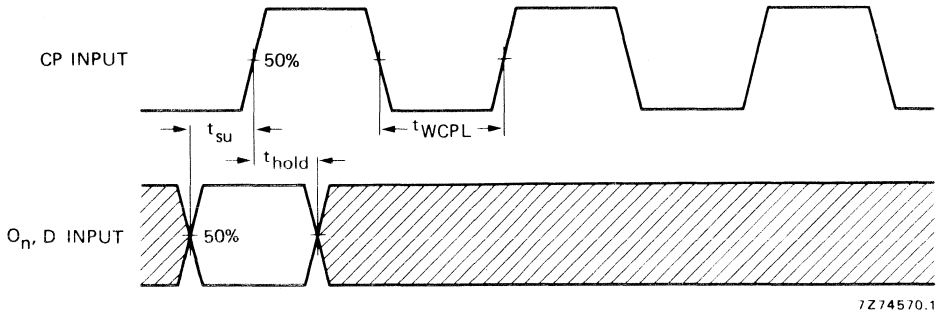


Fig. 4 Waveforms showing minimum clock pulse width, set-up and hold times for O_n (as data input) and D to CP.

DUAL BCD COUNTER

The HEF4518B is a dual 4-bit internally synchronous BCD counter. The counter has an active HIGH clock input (CP_0) and an active LOW clock input ($\overline{CP}_1$), buffered outputs from all four bit positions (O_0 to O_3) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP_0 input if $\overline{CP}_1$ is HIGH or the HIGH to LOW transition of the $\overline{CP}_1$ input if CP_0 is LOW. Either CP_0 or $\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of CP_0, $\overline{CP}_1$.
Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

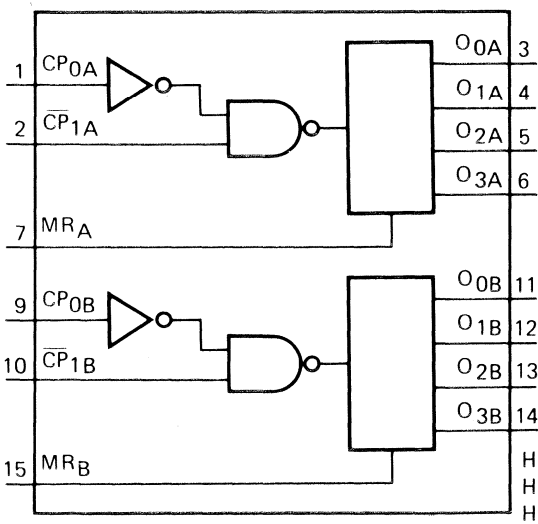


Fig. 1 Functional diagram.

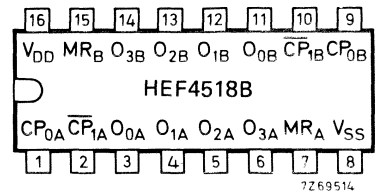


Fig. 2 Pinning diagram.

HEF4518BP : 16-lead DIL; plastic (SOT-38Z).
HEF4518BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4518BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

CP_{0A}, CP_{0B}	clock inputs (L to H triggered)
$\overline{CP}_{1A}$, $\overline{CP}_{1B}$	clock inputs (H to L triggered)
MR_A, MR_B	master reset inputs
O_{0A} to O_{3A}	outputs
O_{0B} to O_{3B}	outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4518B are:

- Multistage synchronous counting.
- Multistage asynchronous counting.
- Frequency dividers.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

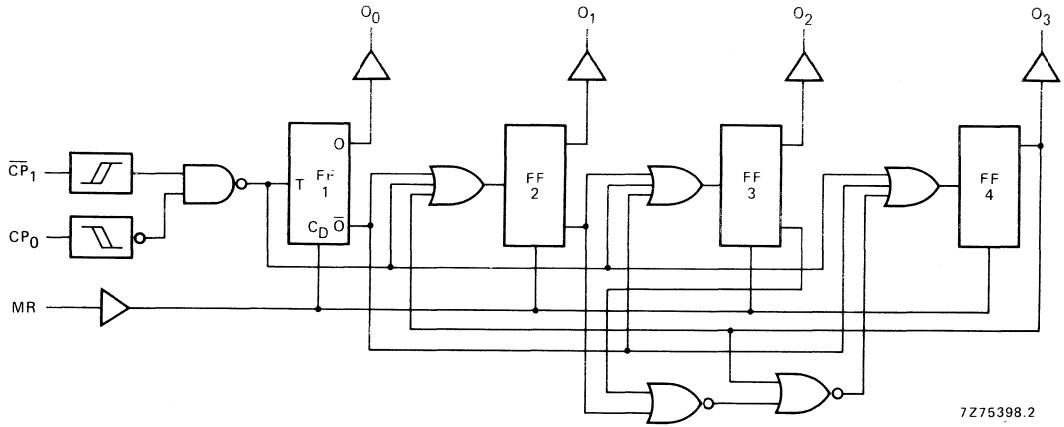


Fig. 3 Logic diagram (one counter).

FUNCTION TABLE

CP_0	$\overline{CP}_1$	MR	mode
∫	H	L	counter advances
L	⟍	L	counter advances
⟍	X	L	no change
X	∫	L	no change
∫	L	L	no change
H	⟍	L	no change
X	X	H	O_0 to O_3 = LOW

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⟍ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP_0, $\overline{CP}_1$ → O_n	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
MR → O_n	5			75	150	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum CP_0	5		60	30		ns	
pulse width; LOW	10	t_{WCPL}	30	15		ns	
	15		20	10		ns	
Minimum $\overline{CP}_1$	5		60	30		ns	
pulse width; HIGH	10	t_{WCPH}	30	15		ns	
	15		20	10		ns	
Minimum MR	5		30	15		ns	
pulse width; HIGH	10	t_{WMRH}	20	10		ns	
	15		16	8		ns	
Recovery time	5		50	25		ns	
for MR	10	t_{RMR}	30	15		ns	see also waveforms Figs 4 and 5
	15		20	10		ns	
Set-up times	5		50	25		ns	
CP_0 → $\overline{CP}_1$	10	t_{su}	30	15		ns	
	15		20	10		ns	
	5		50	25		ns	
$\overline{CP}_1$ → CP_0	10	t_{su}	30	15		ns	
	15		20	10		ns	
Maximum clock	5		8	16		MHz	
pulse frequency	10	f_{max}	15	30		MHz	
	15		20	40		MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$750\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$8000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

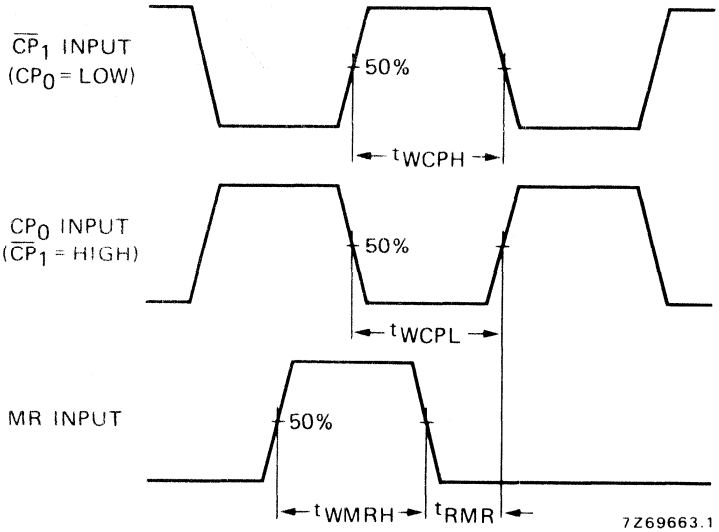


Fig. 4 Waveforms showing recovery time for MR; minimum CP_0, $\overline{CP}_1$ and MR pulse widths.

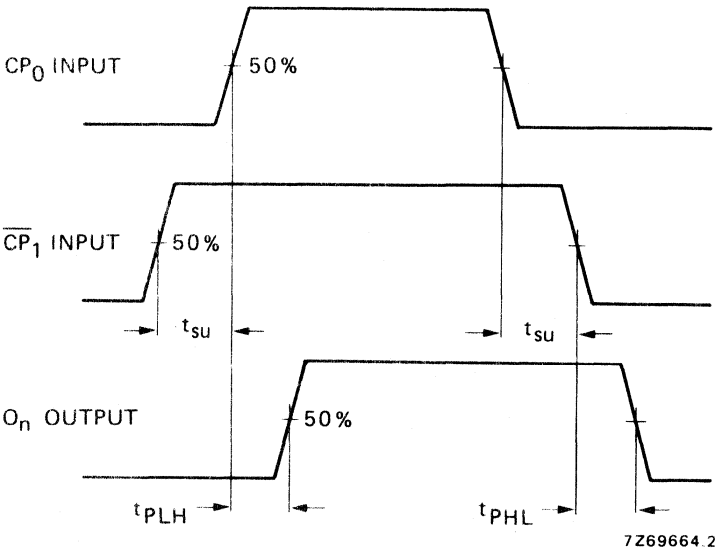


Fig. 5 Waveforms showing set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0, and propagation delays.

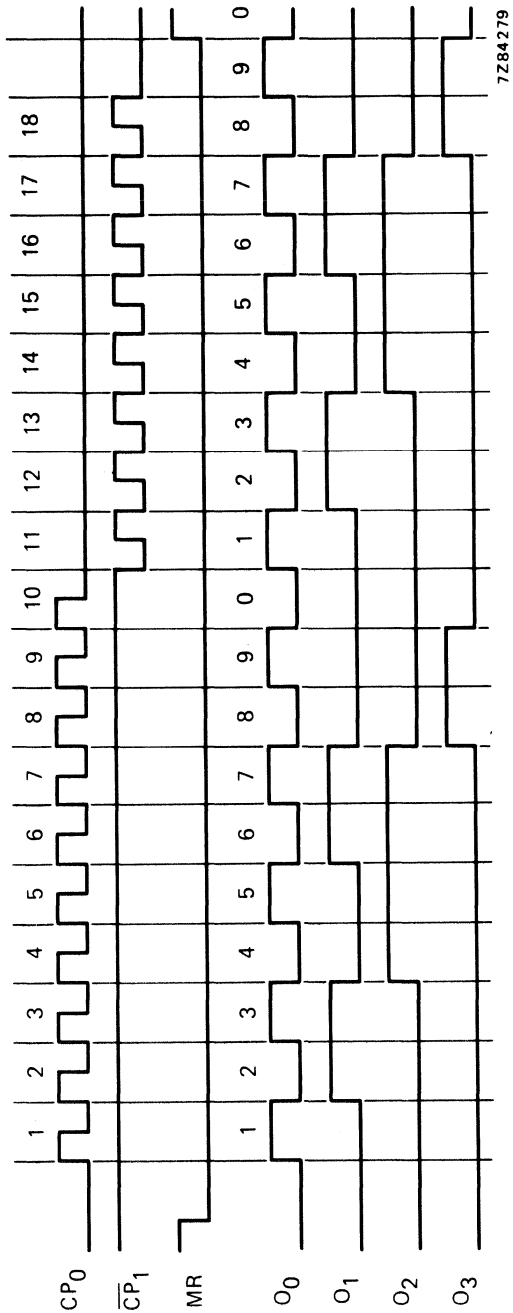


Fig. 6 Timing diagram.

QUADRUPLE 2-INPUT MULTIPLEXER

The HEF4519B provides four multiplexing circuits with common select inputs (S_A, S_B); each circuit contains two inputs (A_n, B_n) and one output (O_n). It may be used to select four bits of information from one of two sources.

The 'A' inputs are selected when S_A is HIGH, the 'B' inputs when S_B is HIGH. When S_A and S_B are HIGH, the output (O_n) is the logical EXCLUSIVE-NOR of the A_n and B_n inputs ($O_n = A_n \odot B_n$).

When S_A and S_B are LOW, the output (O_n) is LOW, independent of the multiplexer inputs (A_n and B_n).

The HEF4519B cannot be used to multiplex analogue signals. The outputs utilize standard buffers for best performance.

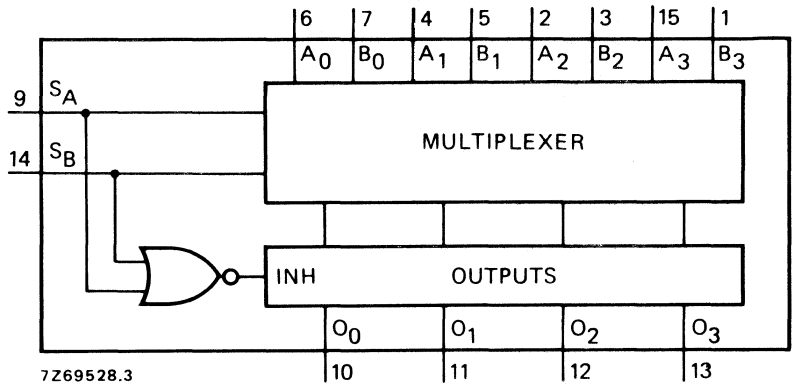


Fig. 1 Functional diagram.

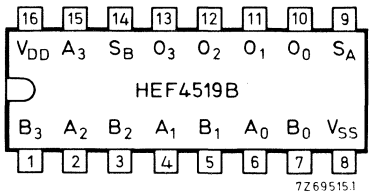


Fig. 2 Pinning diagram.

HEF4519BP : 16-lead DIL; plastic (SOT-38Z).
HEF4519BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4519BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

S_A, S_B	selects inputs (active HIGH)
A_0 to A_3	multiplexer inputs
B_0 to B_3	multiplexer inputs
O_0 to O_3	multiplexer outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

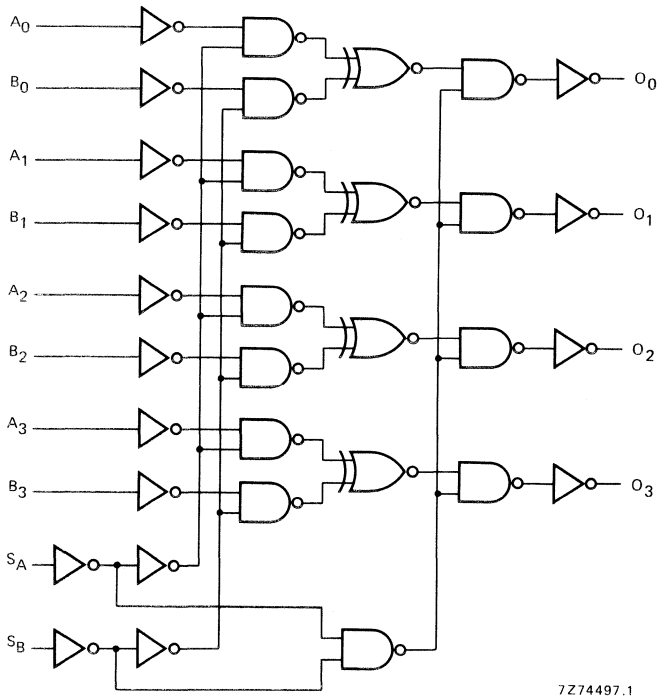


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs				output
S_A	S_B	A_n	B_n	O_n
L	L	X	X	L
H	L	A_n	X	A_n
L	H	X	B_n	B_n
H	H	L	L	H
H	H	H	L	L
H	H	L	H	L
H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
A_n, B_n → O_n	5		95	190	ns	68 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF)C_L
	15		30	60	ns	22 ns + (0,16 ns/pF)C_L
	5		80	160	ns	53 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF)C_L
	15		30	60	ns	22 ns + (0,16 ns/pF)C_L
S_A, S_B → O_n	5		95	190	ns	68 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF)C_L
	15		30	55	ns	22 ns + (0,16 ns/pF)C_L
	5		85	165	ns	58 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF)C_L
	15		30	60	ns	22 ns + (0,16 ns/pF)C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1000 f_i + $\Sigma(f_oC_L)$ × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	6000 f_i + $\Sigma(f_oC_L)$ × V_{DD}^2	
	15	17 000 f_i + $\Sigma(f_oC_L)$ × V_{DD}^2	

APPLICATION INFORMATION

Some examples of applications for the HEF4519B are:

- 2-input multiplexers.
- True/complement selectors.

DUAL BINARY COUNTER

The HEF4520B is a dual 4-bit internally synchronous binary counter. The counter has an active HIGH clock input (CP_0) and an active LOW clock input ($\overline{CP}_1$), buffered outputs from all four bit positions (O_0 to O_3) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP_0 input if $\overline{CP}_1$ is HIGH or the HIGH to LOW transition of the $\overline{CP}_1$ input if CP_0 is LOW. Either CP_0 or $\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of CP_0, $\overline{CP}_1$.
Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

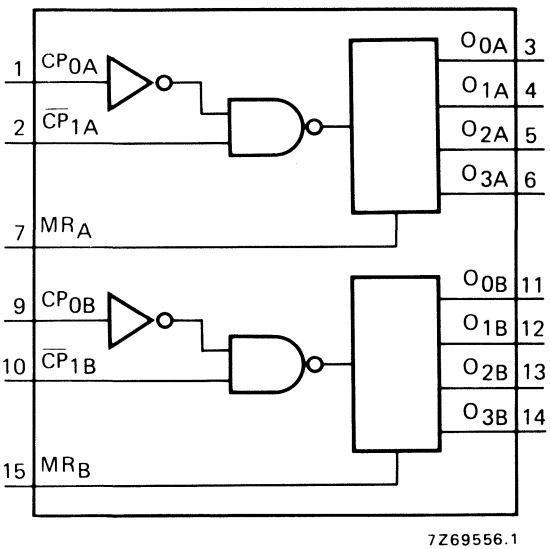


Fig. 1 Functional diagram.

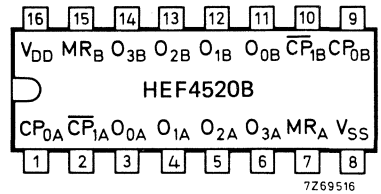


Fig. 2 Pinning diagram.

HEF4520BP : 16-lead DIL; plastic (SOT-38Z).
HEF4520BD: 16-lead DIL; ceramic (cerdip) SOT-74)
HEF4520BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

CP_{0A}, CP_{0B}	clock inputs (L to H triggered)
$\overline{CP}_{1A}$, $\overline{CP}_{1B}$	clock inputs (H to L triggered)
MR_A, MR_B	master reset inputs
O_{0A} to O_{3A}	outputs
O_{0B} to O_{3B}	outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

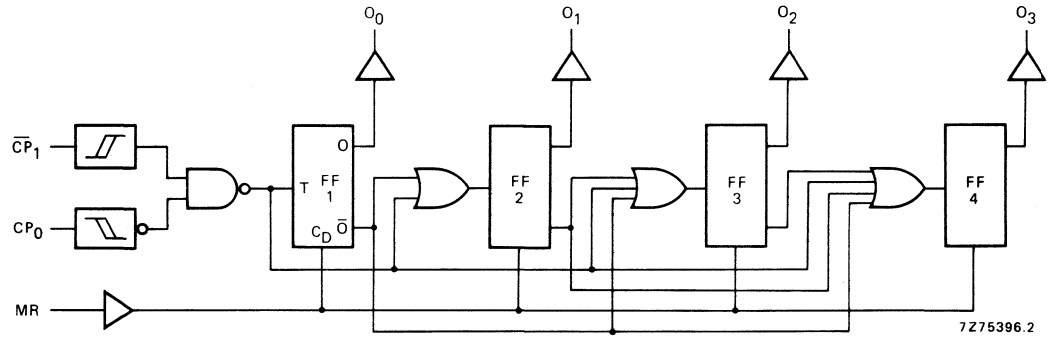


Fig. 3 Logic diagram (one counter).

FUNCTION TABLE

CP_0	$\overline{CP}_1$	MR	mode
∫	H	L	counter advances
L	⟍	L	counter advances
⟍	X	L	no change
X	∫	L	no change
∫	L	L	no change
H	⟍	L	no change
X	X	H	O_0 to O_3 = LOW

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⟍ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP_0, $\overline{CP}_1$ → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
MR → O_n	5			75	150	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum CP_0	5		60	30		ns	
pulse width; LOW	10	t_{WCPL}	30	15		ns	
	15		20	10		ns	
Minimum $\overline{CP}_1$	5		60	30		ns	
pulse width; HIGH	10	t_{WCPH}	30	15		ns	
	15		20	10		ns	
Minimum MR	5		30	15		ns	
pulse width; HIGH	10	t_{WMRH}	20	10		ns	
	15		16	8		ns	
Recovery time	5		50	25		ns	
for MR	10	t_{RMR}	30	15		ns	see also waveforms Figs 4 and 5
	15		20	10		ns	
Set-up times	5		50	25		ns	
CP_0 → $\overline{CP}_1$	10	t_{su}	30	15		ns	
	15		20	10		ns	
	5		50	25		ns	
$\overline{CP}_1$ → CP_0	10	t_{su}	30	15		ns	
	15		20	10		ns	
Maximum clock	5		8	16		MHz	
pulse frequency	10	f_{max}	15	30		MHz	
	15		20	40		MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$850f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3\,800f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$10\,200f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

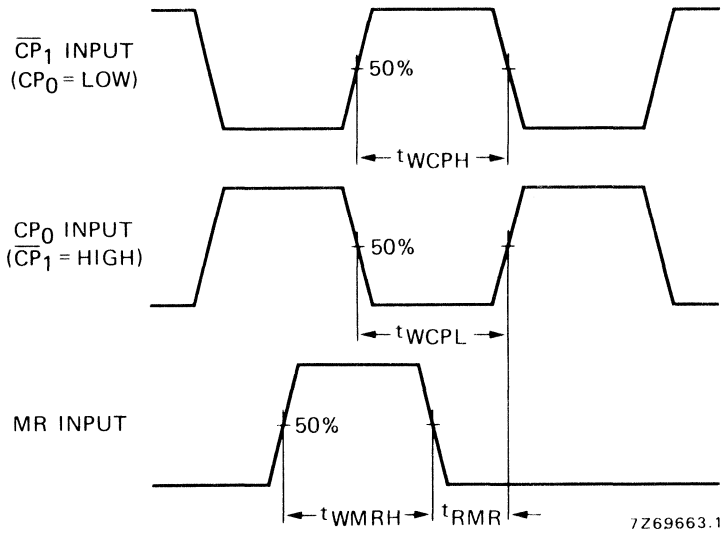


Fig. 4 Waveforms showing recovery time for MR; minimum CP_0, $\overline{CP}_1$ and MR pulse widths.

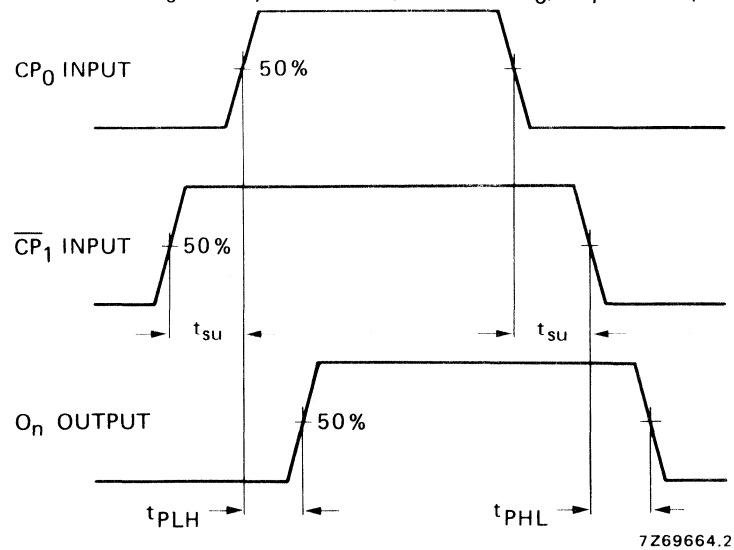


Fig. 5 Waveforms showing set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0, and propagation delays.

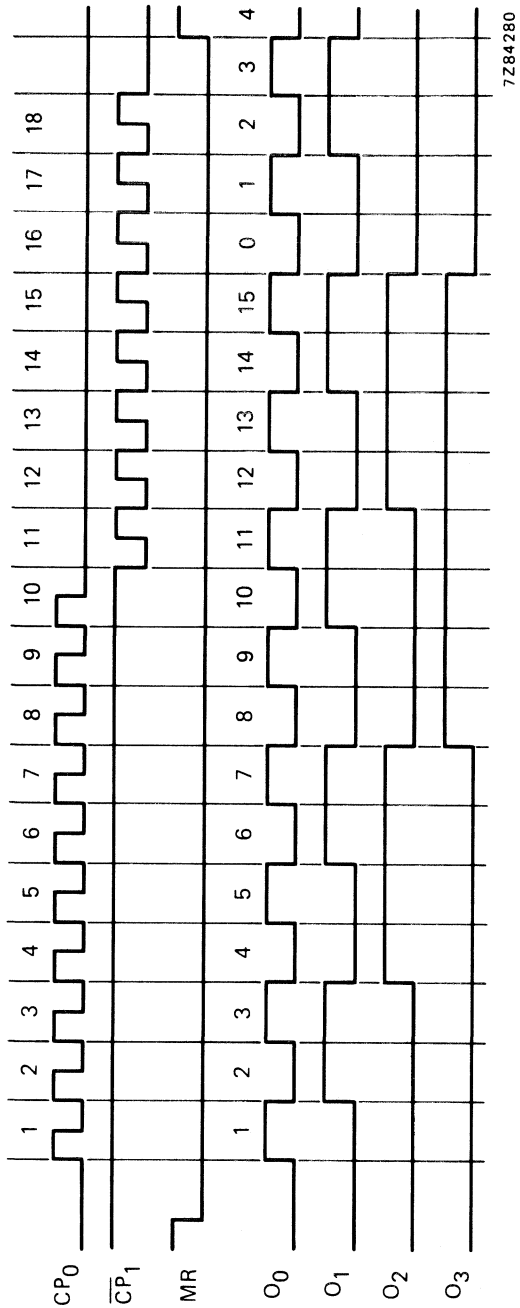


Fig. 6 Timing diagram.

24-STAGE FREQUENCY DIVIDER

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage (I_2/O_2) will function as a crystal oscillator, or in combination with I_1 as an RC oscillator, or as an input buffer for an external oscillator. Low-power operation as a crystal oscillator is enabled by connecting external resistors to pins 3 (V_{SS}') and 5 (V_{DD}').
Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B will count up to $2^{24} = 16777216$. The counting advances on the HIGH to LOW transition of the clock (I_2). The outputs of the last seven stages are available for additional flexibility.

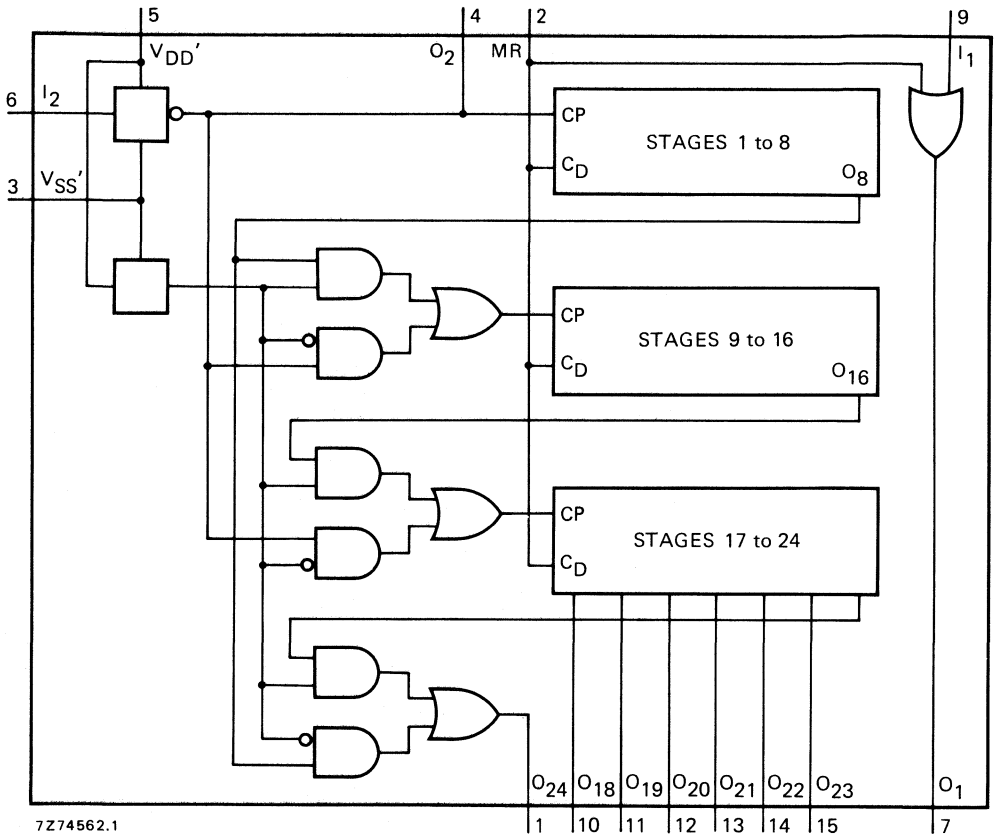


Fig. 1 Functional diagram.

FAMILY DATA
I_{DD} LIMITS category MSI } see Family Specifications

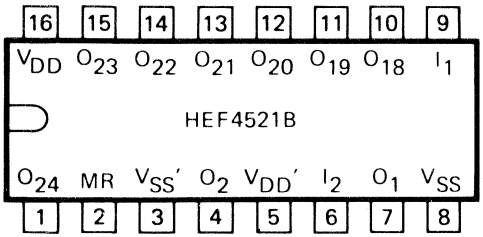


Fig. 2 Pinning diagram.

HEF4521BP : 16-lead DIL; plastic (SOT-38Z).
HEF4521BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4521BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

COUNT CAPACITY

output	count capacity
O_{18}	2^{18} = 262 144
O_{19}	2^{19} = 524 288
O_{20}	2^{20} = 1 048 576
O_{21}	2^{21} = 2 097 152
O_{22}	2^{22} = 4 194 304
O_{23}	2^{23} = 8 388 608
O_{24}	2^{24} = 16 777 216

FUNCTIONAL TEST SEQUENCE

inputs		control terminals			outputs	remarks
MR	I_2	O_2	V_{SS}'	V_{DD}'	O_{18} to O_{24}	
H	L	L	V_{DD}	V_{SS}	L	counter is in three 8-stage sections in parallel mode; I_2 and O_2 are interconnected (O_2 is now input); counter is reset by MR
L	⎍	⎍	V_{DD}	V_{SS}	H	255 pulses are clocked into I_2, O_2 (the counter advances on the LOW to HIGH transition)
L	L	L	V_{SS}	V_{SS}	H	V_{SS}' is connected to V_{SS}
L	H	L	V_{SS}	V_{SS}	H	the input I_2 is made HIGH
L	H	L	V_{SS}	V_{DD}	H	V_{DD}' is connected to V_{DD}; O_2 is now made floating and becomes an output; the device is now in the 2^{24} mode
L	⎺⎺_		V_{SS}	V_{DD}	L	counter ripples from an all HIGH state to an all LOW state

A test function has been included for the reduction of the test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting V_{SS}' to V_{DD} and V_{DD}' to V_{SS}. Via I_2 (connected to O_2) 255 counts are loaded into each of the 8-stage sections in parallel. All flip-flops are now at a HIGH state. The counter is now returned to the normal 24-stage in series configuration by connecting V_{SS}' to V_{SS} and V_{DD}' to V_{DD}. One more pulse is entered into input I_2, which will cause the counter to ripple from an all HIGH state to an all LOW state.

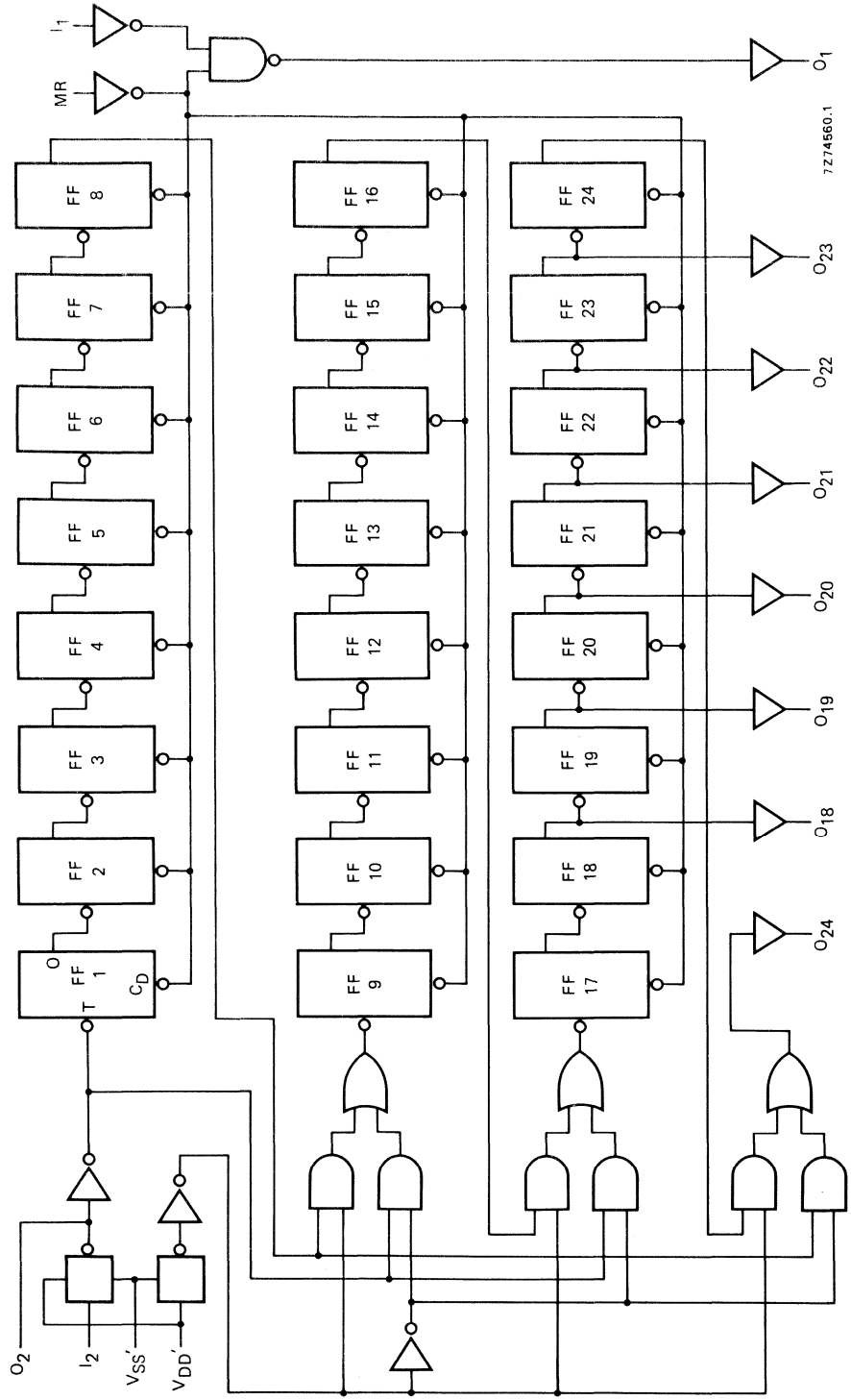


Fig. 3 Logic diagram; for schematic diagram of clock circuit see Fig. 4.

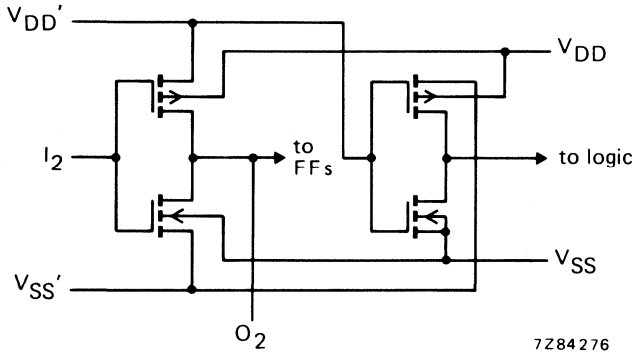


Fig. 4 Schematic diagram of clock input circuitry.

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
$I_2 \rightarrow O_{18}$	5			950	1900 ns	923 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		350	700 ns	339 ns + (0,23 ns/pF) C_L
	15			220	440 ns	212 ns + (0,16 ns/pF) C_L
	5			950	1900 ns	923 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		350	700 ns	339 ns + (0,23 ns/pF) C_L
	15			220	440 ns	212 ns + (0,16 ns/pF) C_L
$O_n \rightarrow O_{n+1}$	5			40	80 ns	13 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		15	30 ns	4 ns + (0,23 ns/pF) C_L
	15			10	20 ns	2 ns + (0,16 ns/pF) C_L
	5			40	80 ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		15	30 ns	4 ns + (0,23 ns/pF) C_L
	15			10	20 ns	2 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			120	240 ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
$I_1 \rightarrow O_1$	5			90	180 ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70 ns	24 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
	5			60	120 ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60 ns	19 ns + (0,23 ns/pF) C_L
	15			20	40 ns	12 ns + (0,16 ns/pF) C_L
Output transition times						
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	
Minimum I_2 pulse width; HIGH	5	t_{WI2H}	80	40	ns	see also waveforms Fig. 5
	10		40	20	ns	
	15		30	15	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	70	35	ns	
	10		40	20	ns	
	15		30	15	ns	
Recovery time for MR	5	t_{RMR}	20	−10	ns	
	10		15	−5	ns	
	15		15	0	ns	
Maximum clock pulse frequency	5	f_{max}	6	12	MHz	
	10		12	25	MHz	
	15		17	35	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\,050\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

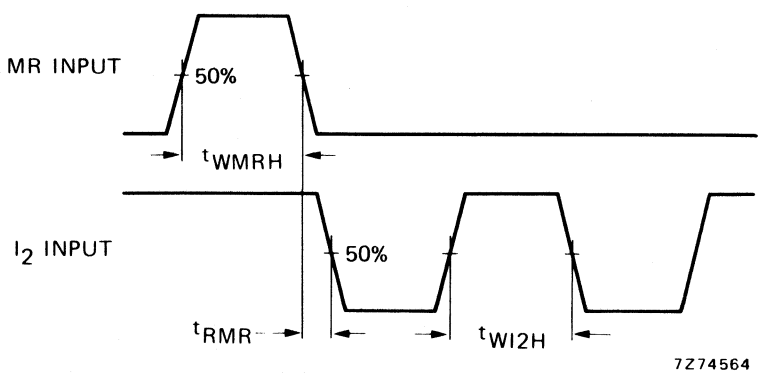
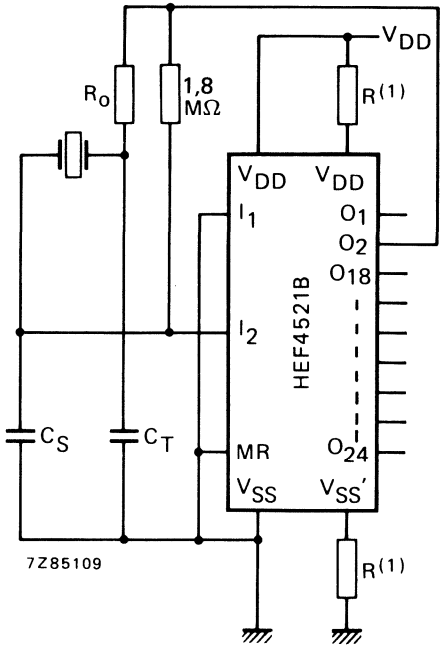


Fig. 5 Waveforms showing minimum pulse widths for MR and I_2, recovery time for MR.

APPLICATION INFORMATION



(1) Optional for low power operation.

Fig. 6 Crystal oscillator circuit.

Typical characteristics for crystal oscillator circuit (Fig. 6):

	500 kHz circuit	50 kHz circuit	unit
Crystal characteristics			
resonance frequency	500	50	kHz
crystal cut	S	N	—
equivalent resistance; R_S	1	6,2	kΩ
External resistor/capacitor values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF

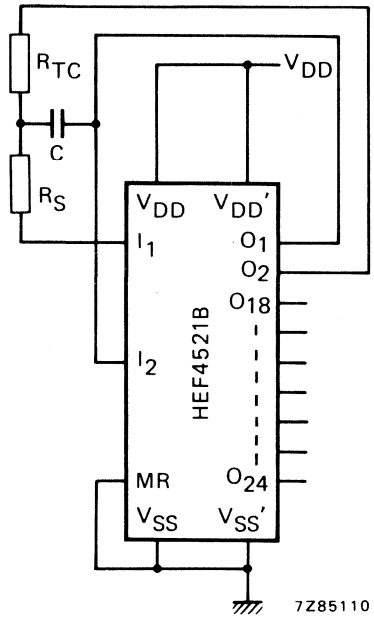
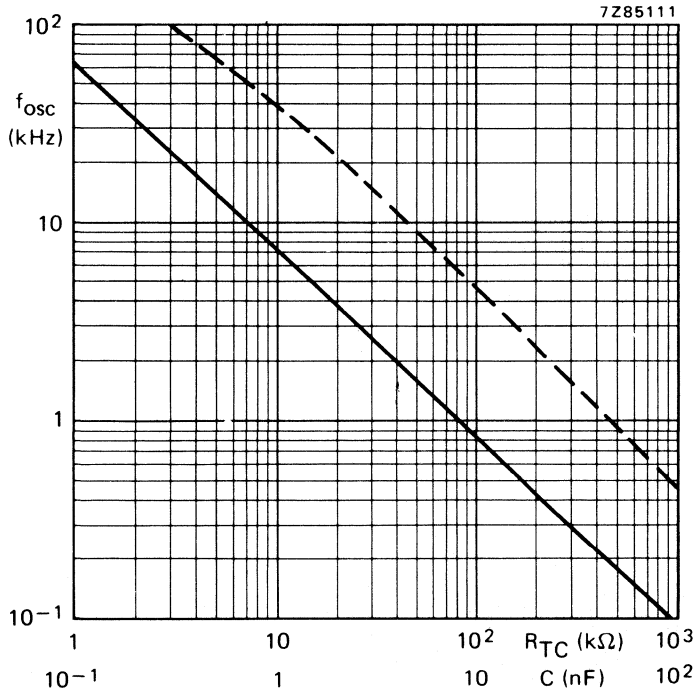


Fig. 7 RC oscillator circuit;
$f \approx \frac{1}{2{,}3 \times R_{TC} \times C}$; $R_S \geqslant 2\ R_{TC}$, in which:
f in Hz, R in Ω, C in F.



— — — R_{TC}; C = 1 nF; $R_S \approx 2\ R_{TC}$
———— C; R_{TC} = 56 kΩ; R_S = 120 kΩ

Fig. 8 Oscillator frequency as a function of R_{TC} and C; V_{DD} = 10 V; test circuit is Fig. 7.

APPLICATION INFORMATION (continued)

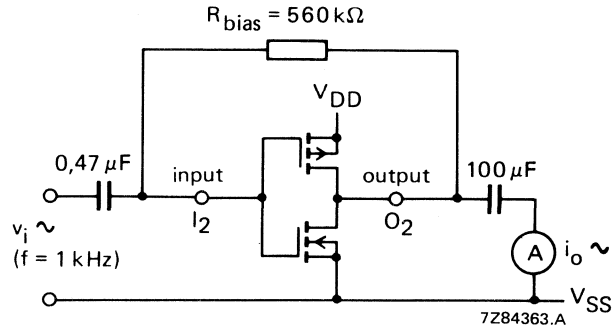
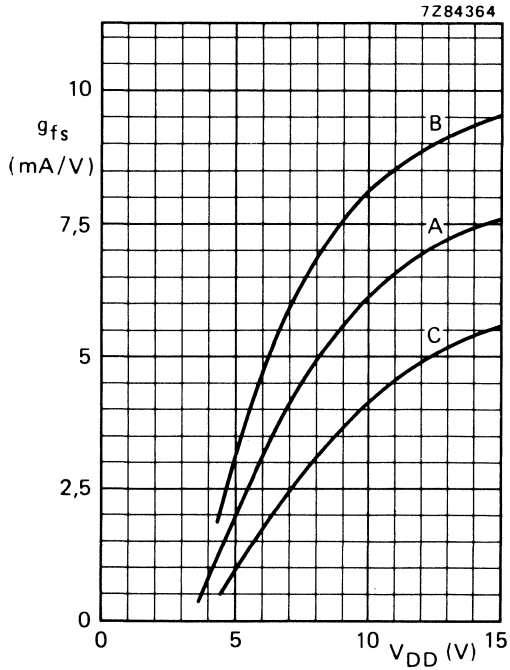


Fig. 9 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 10).



Curves in Fig. 10:

A: average,
B: average + 2 s,
C: average −2 s, in which:
's' is the observed standard deviation.

Fig. 10 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

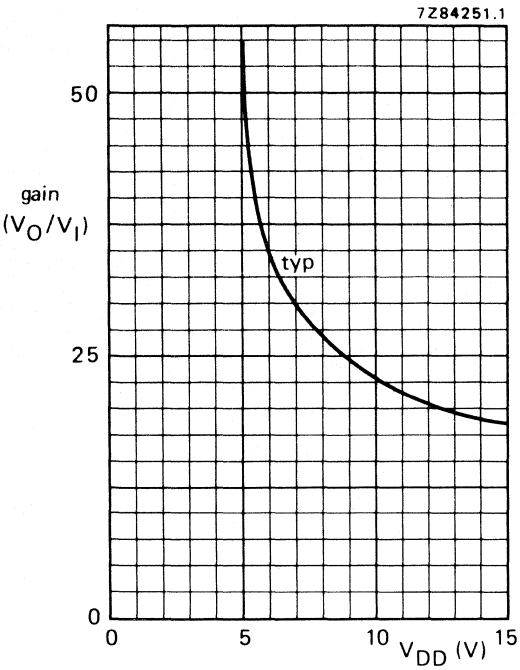


Fig. 11 Voltage gain (V_O/V_I as a function of supply voltage.

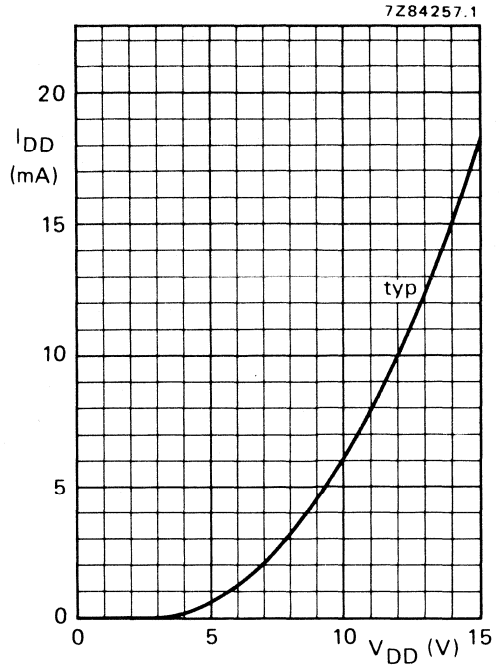


Fig. 12 Supply current as a function of supply voltage.

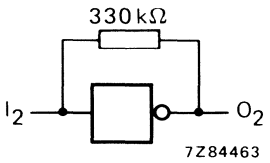


Fig. 13 Test set-up for measuring graphs of Figs 11 and 12.

PROGRAMMABLE 4-BIT BCD DOWN COUNTER

The HEF4522B is a synchronous programmable 4-bit BCD down counter with an active HIGH and an active LOW clock input (CP_0, $\overline{CP}_1$), an asynchronous parallel load input (PL), four parallel inputs (P_0 to P_3), a cascade feedback input (CF), four buffered parallel outputs (O_0 to O_3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

This device is a programmable, cascadable down counter with a decoded TC output for divide-by-n applications. In single stage applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR, which must be LOW. When PL and $\overline{CP}_1$ are LOW, the counter advances on a LOW to HIGH transition of CP_0. When PL is LOW and CP_0 is HIGH, the counter advances on a HIGH to LOW transition of $\overline{CP}_1$. TC is HIGH when the counter is in the zero state ($O_0 = O_1 = O_2 = O_3$ = LOW) and CF is HIGH and PL is LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

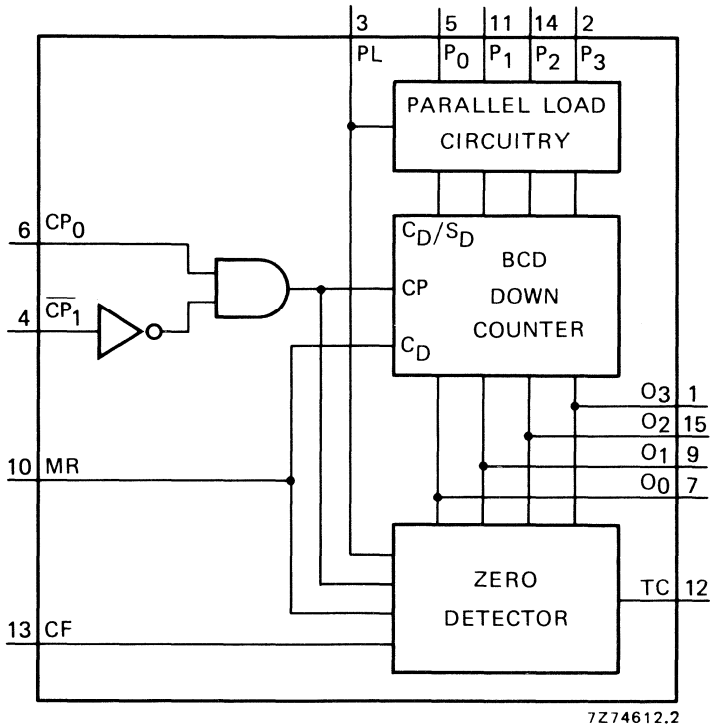
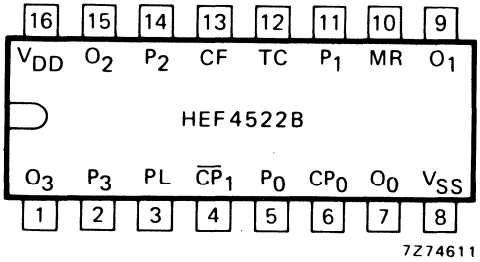


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications



HEF4522BP : 16-lead DIL; plastic (SOT-38Z).
HEF4522BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4522BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

PINNING

PL	parallel load input
P_0 to P_3	parallel inputs
CF	cascade feedback input
CP_0	clock input (LOW to HIGH, triggered)
$\overline{CP}_1$	clock input (HIGH to LOW, triggered)
MR	asynchronous master reset input
TC	terminal count output
O_0 to O_3	buffered parallel outputs

COUNTING MODE

CF = HIGH; PL = LOW; MR = LOW

count	outputs			
	O_3	O_2	O_1	O_0
9	H	L	L	H
8	H	L	L	L
7	L	H	H	H
6	L	H	H	L
5	L	H	L	H
4	L	H	L	L
3	L	L	H	H
2	L	L	H	L
1	L	L	L	H
0	L	L	L	L

FUNCTION TABLE

MR	PL	CP_0	$\overline{CP}_1$	mode
H	X	X	X	reset (asynchronous)
L	H	X	X	preset (asynchronous)
L	L	∫	H	no change
L	L	L	\	no change
L	L	\	X	no change
L	L	X	∫	no change
L	L	∫	L	counter advances
L	L	H	\	counter advances

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
\ = negative-going transition

SINGLE STAGE OPERATION

Divide-by-n; MR = LOW; CF = HIGH; $\overline{CP}_1$ = LOW

PL	P_3	P_2	P_1	P_0	divide by	TC output pulse width
L	X	X	X	X	10	one clock period
TC	H	H	H	H	15	clock pulse HIGH
TC	H	H	H	L	14	
TC	H	H	L	H	13	
TC	H	H	L	L	12	
TC	H	L	H	H	11	
TC	H	L	H	L	10	
TC	H	L	L	H	9	
TC	H	L	L	L	8	
TC	L	H	H	H	7	
TC	L	H	H	L	6	
TC	L	H	L	H	5	
TC	L	H	L	L	4	
TC	L	L	H	H	3	
TC	L	L	H	L	2	
TC	L	L	L	H	1	
TC	L	L	L	L	no operation	

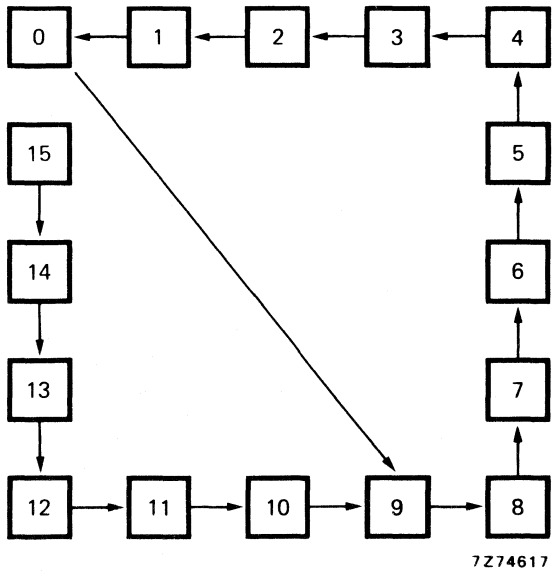


Fig. 3 State diagram.

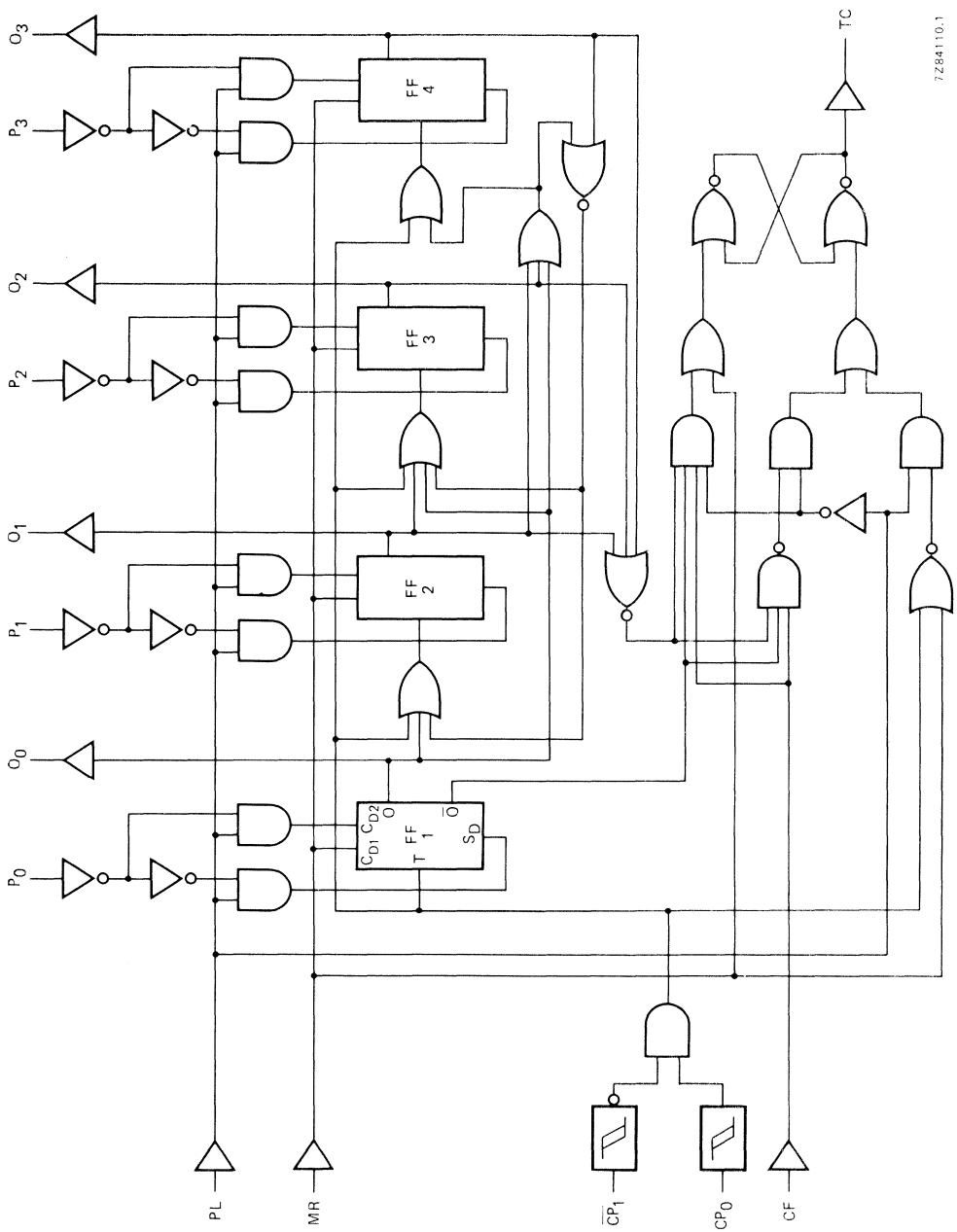


Fig. 4 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1000 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4000 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	10 000 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP_0, $\overline{CP}_1$ → O_n	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CP_0, $\overline{CP}_1$ → TC	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
PL → O_n	5			200	400	ns	173 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
MR → O_n	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; CP_0 LOW	5	t_{WCPL}	80	40		ns	see also waveforms Figs 5 and 6
	10		40	20		ns	
	15		30	15		ns	
Minimum clock pulse width; $\overline{CP}_1$ HIGH	5	t_{WCPH}	80	40		ns	
	10		40	20		ns	
	15		30	15		ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	100	50		ns	
	10		40	20		ns	
	15		32	16		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	130	65		ns	
	10		50	25		ns	
	15		40	20		ns	
Hold time $P_n \longrightarrow$ PL	5	t_{hold}	30	5		ns	
	10		20	5		ns	
	15		15	5		ns	
Set-up time $P_n \longrightarrow$ PL	5	t_{su}	30	0		ns	
	10		20	0		ns	
	15		15	0		ns	
Maximum clock pulse frequency PL = LOW	5	f_{max}	6	12		MHz	see note
	10		12	25		MHz	
	15		16	32		MHz	

Note

In the divide-by-n mode (PL connected to TC), one has to observe the maximum HIGH to LOW propagation delay for CP to TC, before applying the next clock pulse.

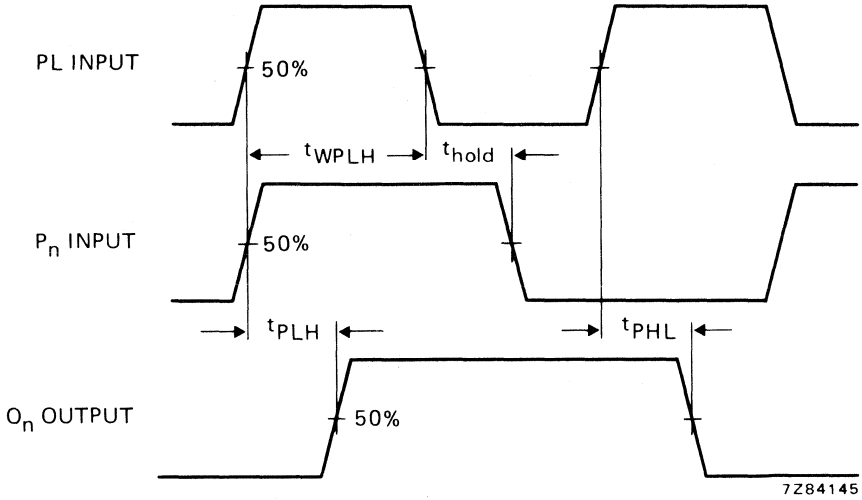


Fig. 5 Waveforms showing minimum PL pulse width, propagation delays for PL, P_n to O_n and hold time for PL to P_n.

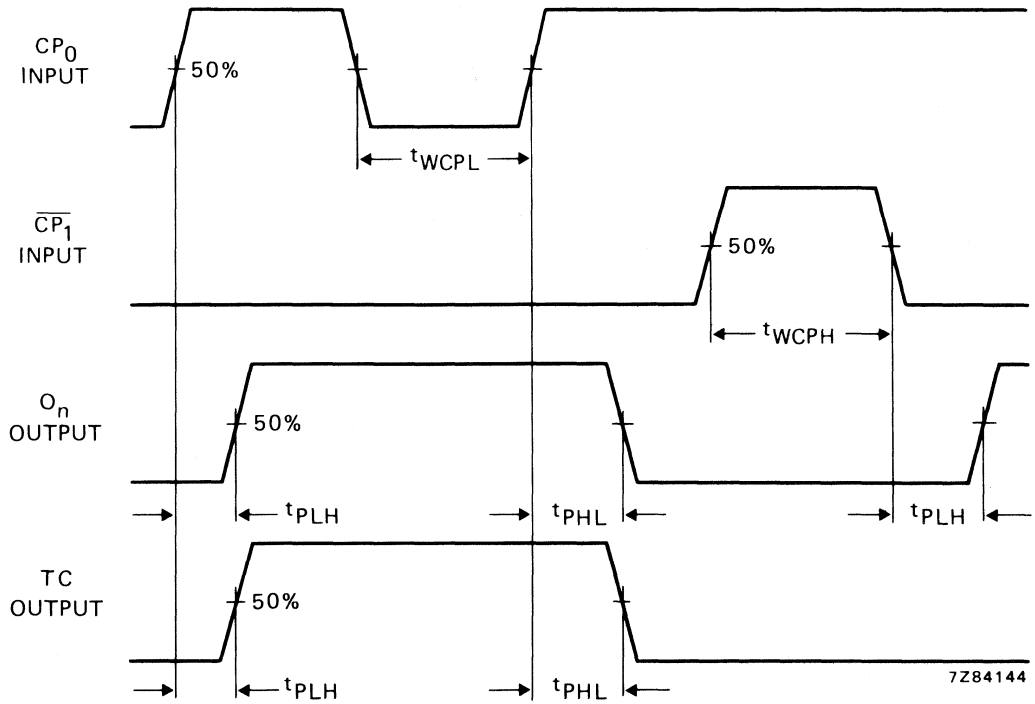


Fig. 6 Waveforms showing minimum CP_0 and $\overline{CP}_1$ pulse widths, propagation delays for CP_0, $\overline{CP}_1$ to O_n and TC.

APPLICATION INFORMATION

Some examples of applications for the HEF4522B are:

- Divide-by-n counter
- Programmable frequency divider

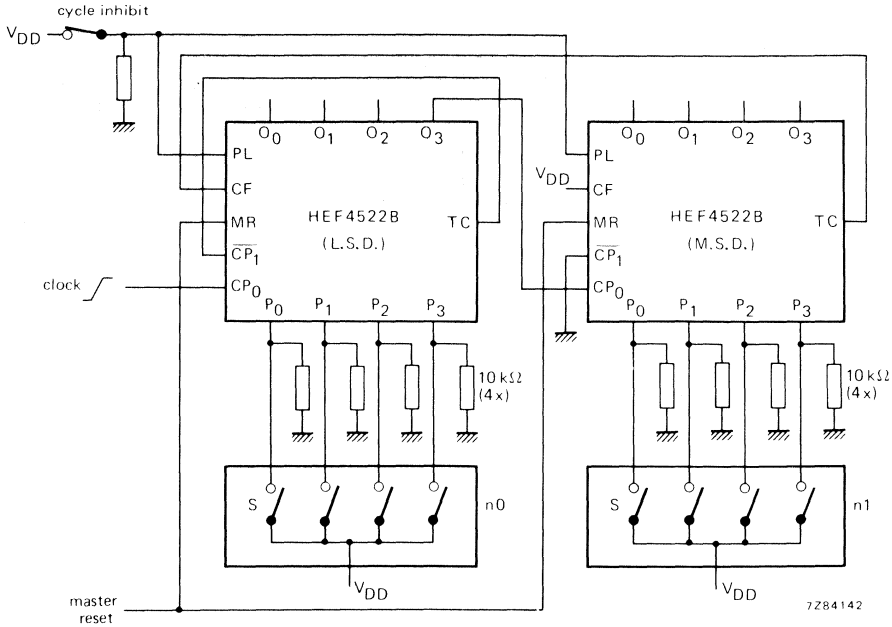
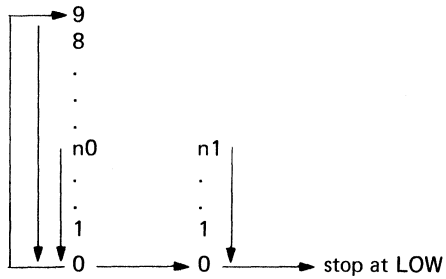


Fig. 7 Typical application of two HEF4522B circuits in a 2-stage programmable down counter (one cycle). S are thumbwheel switches; when open: LOW state.

Counting cycle:



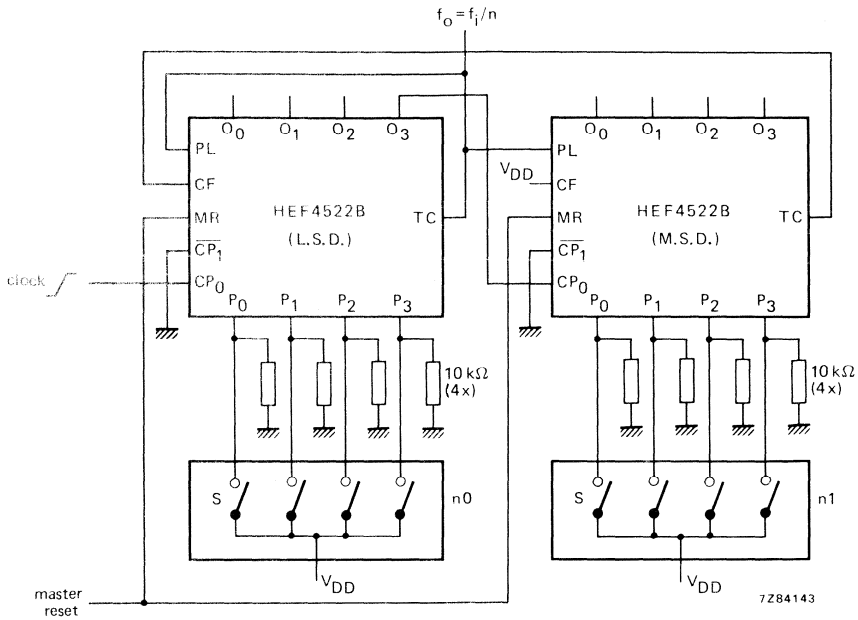
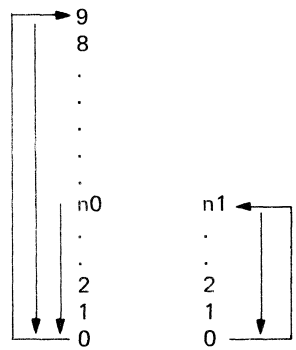


Fig. 8 Typical application of two HEF4522B circuits in a 2-stage programmable frequency divider. S are thumbwheel switches; when open: LOW state.

Counting cycle:



L.S.D. counter M.S.D. counter

PROGRAMMABLE 4-BIT BINARY DOWN COUNTER

The HEF4526B is a synchronous programmable 4-bit binary down counter with an active HIGH and an active LOW clock input (CP_0, $\overline{CP_1}$), an asynchronous parallel load input (PL), four parallel inputs (P_0 to P_3), a cascade feedback input (CF), four buffered parallel outputs (O_0 to O_3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

This device is a programmable, cascadable down counter with a decoded TC output for divide-by-n applications. In single stage applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR, which must be LOW. When PL and $\overline{CP_1}$ are LOW, the counter advances on a LOW to HIGH transition of CP_0. When PL is LOW and CP_0 is HIGH, the counter advances on a HIGH to LOW transition of $\overline{CP_1}$. TC is HIGH when the counter is in the zero state ($O_0 = O_1 = O_2 = O_3$ = LOW) and CF is HIGH and PL is LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

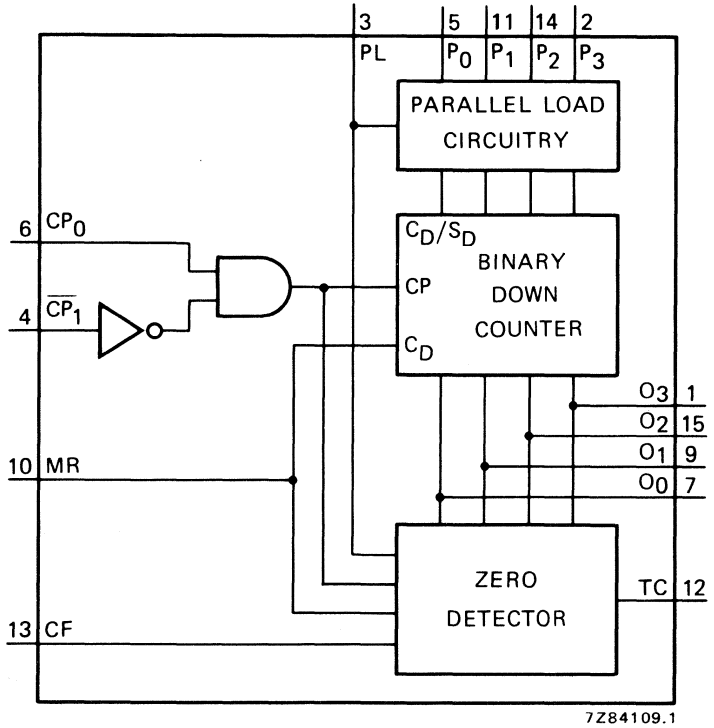
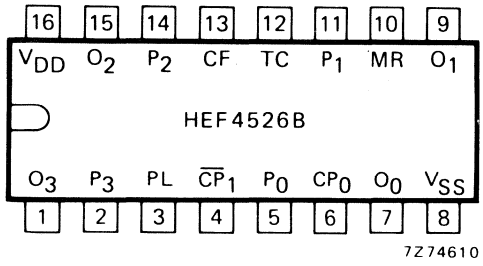


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



HEF4526BP : 16-lead DIL; plastic (SOT-38Z).
HEF4526BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4526BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

PINNING

PL	parallel load input
P_0 to P_3	parallel inputs
CF	cascade feedback input
CP_0	clock input (LOW to HIGH, triggered)
$\overline{CP}_1$	clock input (HIGH to LOW, triggered)
MR	asynchronous master reset input
TC	terminal count output
O_0 to O_3	buffered parallel outputs

COUNTING MODE

CF = HIGH; PL = LOW; MR = LOW

count	outputs			
	O_3	O_2	O_1	O_0
15	H	H	H	H
14	H	H	H	L
13	H	H	L	H
12	H	H	L	L
11	H	L	H	H
10	H	L	H	L
9	H	L	L	H
8	H	L	L	L
7	L	H	H	H
6	L	H	H	L
5	L	H	L	H
4	L	H	L	L
3	L	L	H	H
2	L	L	H	L
1	L	L	L	H
0	L	L	L	L

FUNCTION TABLE

MR	PL	CP_0	$\overline{CP}_1$	mode
H	X	X	X	reset (asynchronous)
L	H	X	X	preset (asynchronous)
L	L	∫	H	no change
L	L	L	∖	no change
L	L	∖	X	no change
L	L	X	∫	no change
L	L	∫	L	counter advances
L	L	H	∖	counter advances

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
∖ = negative-going transition

SINGLE STAGE OPERATION

Divide-by-n; MR = LOW; CF = HIGH; $\overline{CP}_1$ = LOW

PL	P_3	P_2	P_1	P_0	divide by	TC output pulse width
L	X	X	X	X	16	one clock period
TC	H	H	H	H	15	clock pulse HIGH
TC	H	H	H	L	14	
TC	H	H	L	H	13	
TC	H	H	L	L	12	
TC	H	L	H	H	11	
TC	H	L	H	L	10	
TC	H	L	L	H	9	
TC	H	L	L	L	8	
TC	L	H	H	H	7	
TC	L	H	H	L	6	
TC	L	H	L	H	5	
TC	L	H	L	L	4	
TC	L	L	H	H	3	
TC	L	L	H	L	2	
TC	L	L	L	H	1	
TC	L	L	L	L	no operation	

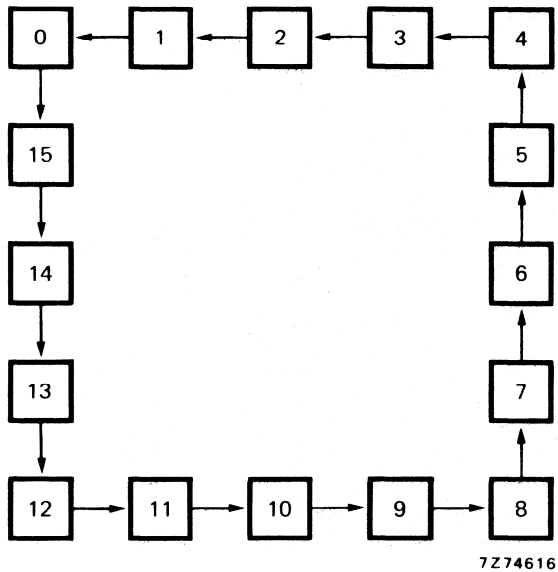


Fig. 3 State diagram.

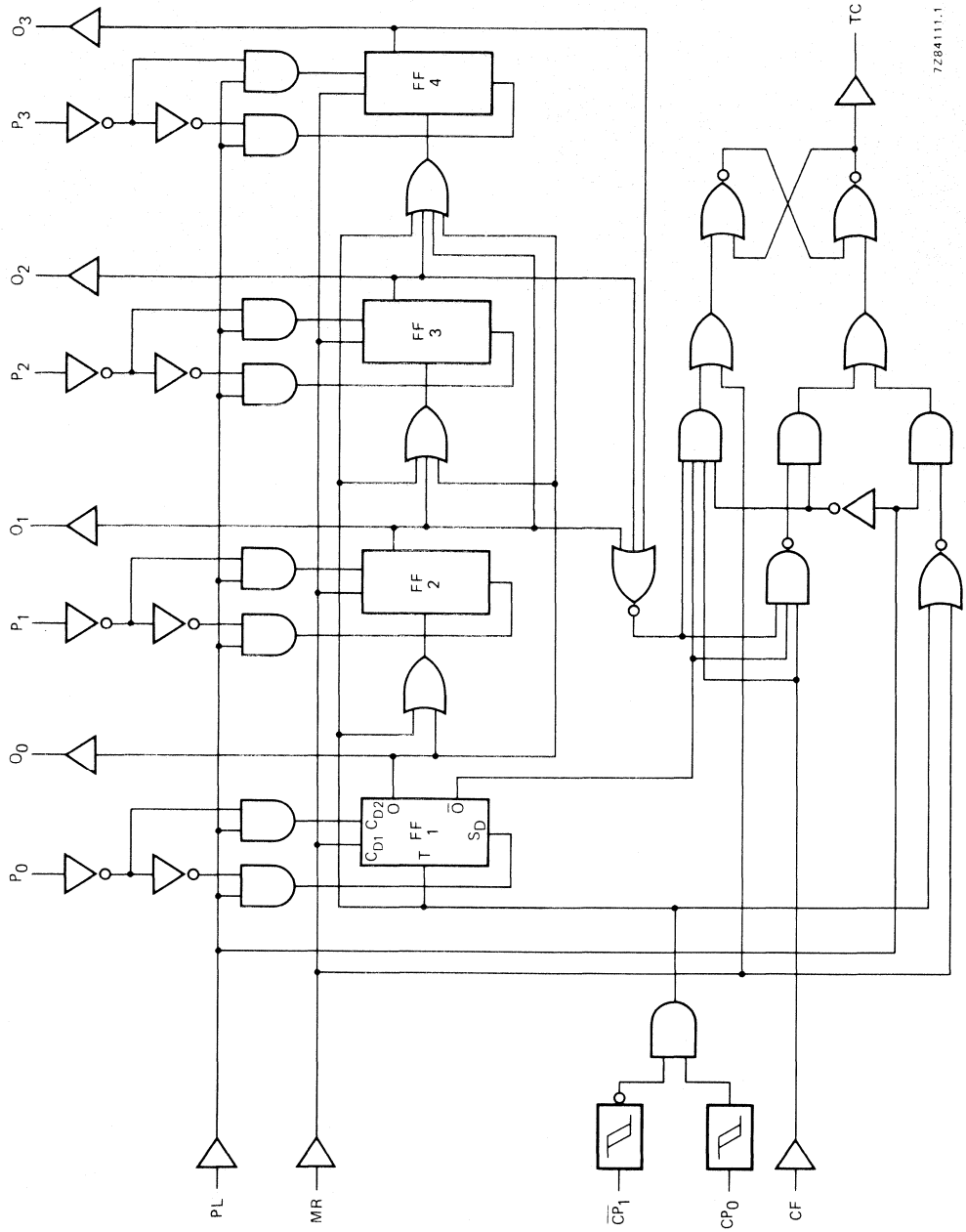


Fig. 4 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1000 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	4000 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	10 000 f_i + Σ($f_o C_L$) x V_{DD}^2	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP_0, $\overline{CP}_1$ → O_n	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CP_0, $\overline{CP}_1$ → TC	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
PL → O_n	5			200	400	ns	173 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
MR → O_n	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width CP_0 LOW	5	t_{WCPL}	80	40		ns	see also waveforms Figs 5 and 6
	10		40	20		ns	
	15		30	15		ns	
Minimum clock pulse width $\overline{CP}_1$ HIGH	5	t_{WCPH}	80	40		ns	
	10		40	20		ns	
	15		30	15		ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	100	50		ns	
	10		40	20		ns	
	15		32	16		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	130	65		ns	
	10		50	25		ns	
	15		40	20		ns	
Hold time $P_n \longrightarrow PL$	5	t_{hold}	30	5		ns	
	10		20	5		ns	
	15		15	5		ns	
Set-up time $P_n \longrightarrow PL$	5	t_{su}	30	0		ns	
	10		20	0		ns	
	15		15	0		ns	
Maximum clock pulse frequency PL = LOW	5	f_{max}	6	12		MHz	see note
	10		12	25		MHz	
	15		16	32		MHz	

Note

In the divide-by-n mode (PL connected to TC), one has to observe the maximum HIGH to LOW propagation delay for CP to TC, before applying the next clock pulse.

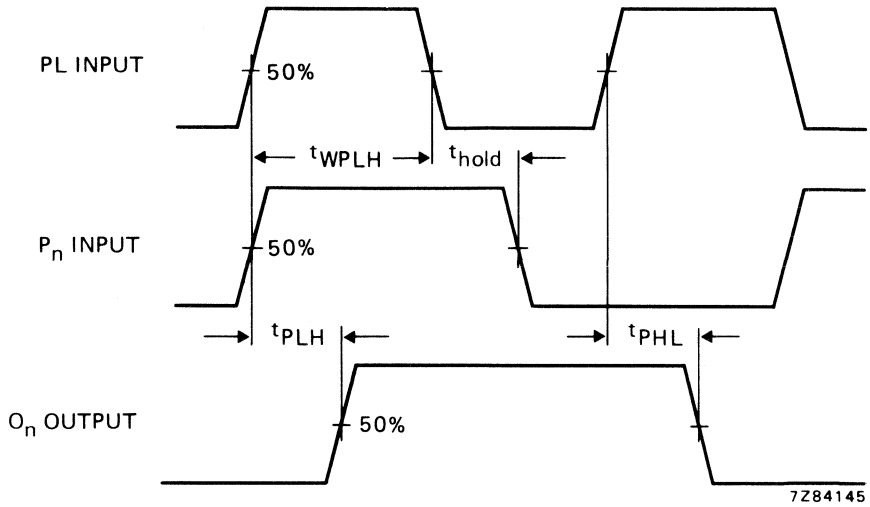


Fig. 5 Waveforms showing minimum PL pulse width, propagation delays for PL, P_n to O_n and hold time for PL to P_n.

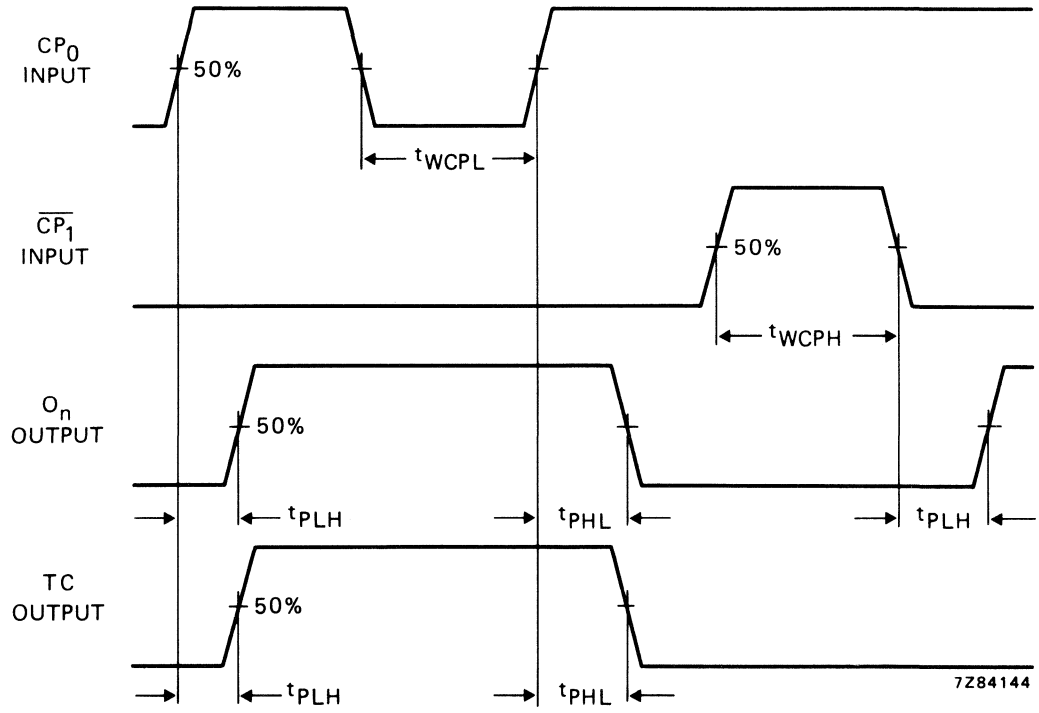


Fig. 6 Waveforms showing minimum CP_0 and $\overline{CP}_1$ pulse widths, propagation delays for CP_0, $\overline{CP}_1$ to O_n and TC.

APPLICATION INFORMATION

Some examples of applications for the HEF4526B are:

- Divide-by-n counter
- Programmable frequency divider

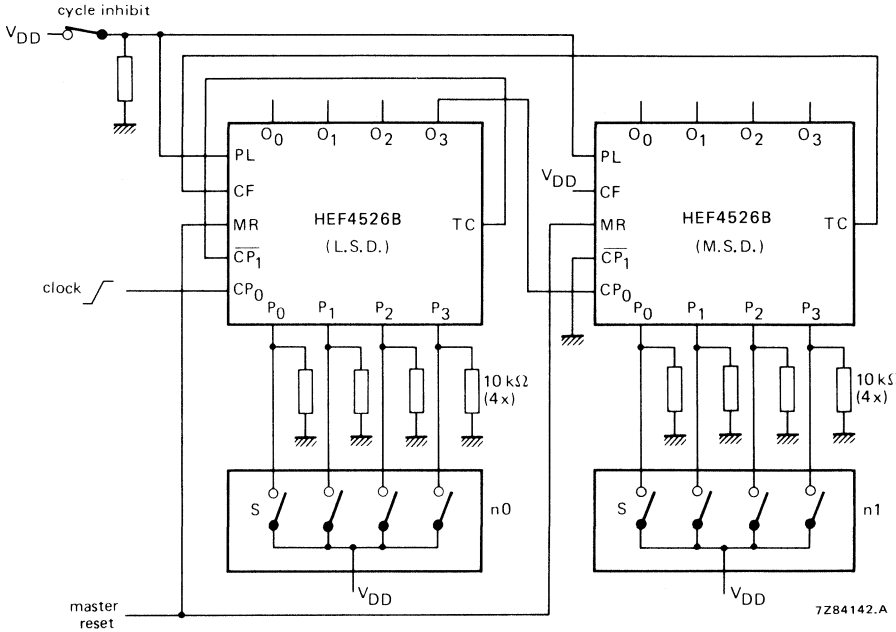
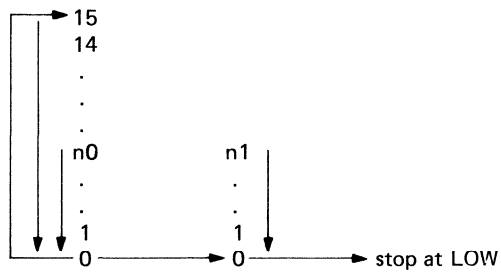


Fig. 7 Typical application of two HEF4526B circuits in a 2-stage programmable down counter (one cycle). S are thumbwheel switches; when open: LOW state.

Counting cycle:



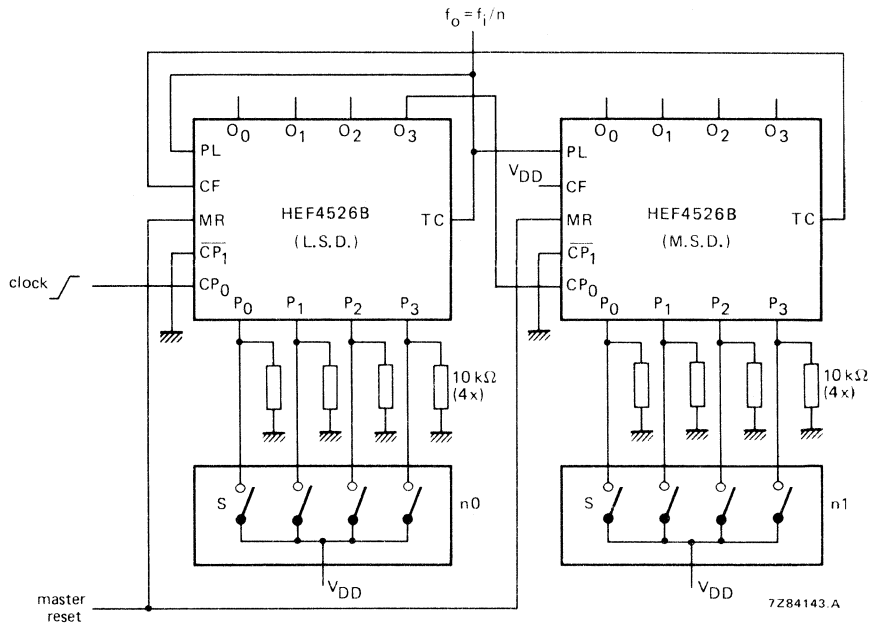
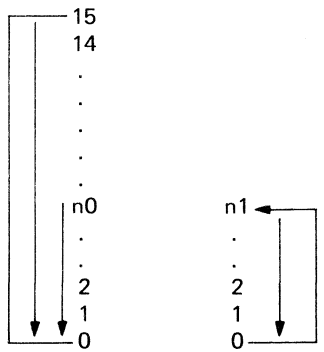


Fig. 8 Typical application of two HEF4526B circuits in a 2-stage programmable frequency divider. S are thumbwheel switches; when open: LOW state.

Counting cycle:



BCD RATE MULTIPLIER

The HEF4527B is a BCD rate multiplier with two buffered rate outputs (O_1 and $\overline{O}_1$), two buffered terminal count outputs (TC and $\overline{TC}$), four BCD rate select inputs (S_A, S_B, S_C, S_D), a common clock input (CP), a preset input (PL), an overriding asynchronous clear input (CL), a strobe input (STR), a cascade input (CAS) and an active LOW count enable input ($\overline{CE}$).

The BCD rate multiplier provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD number, there will be six output pulses for every ten clock input pulses. The output is clocked on the negative-going transition of the clock.

When $\overline{CE}$, STR, CAS, CL and PL are LOW, the rate pulses are available at the outputs O_1 and $\overline{O}_1$, the terminal count pulses at TC and $\overline{TC}$.

A HIGH on CL resets the counter, independent of all other input conditions and a rate of 10 pulses is available at O_1 and $\overline{O}_1$ when S_D is HIGH. When $\overline{CE}$ is HIGH, the counter is disabled, the state of the outputs (O_1, $\overline{O}_1$) depend on the content of the counter.

A HIGH on PL sets the counter in the '9' state and TC becomes HIGH.

A HIGH on STR inhibits the outputs O_1 and $\overline{O}_1$. A HIGH on CAS forces the output O_1 to HIGH, while the state of $\overline{O}_1$ depends on the inputs S_A to S_D (see lines 1 to 16 of function table).

This device may be used to perform arithmetic operations. For the add mode and multiply mode see Figs 5 and 6.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

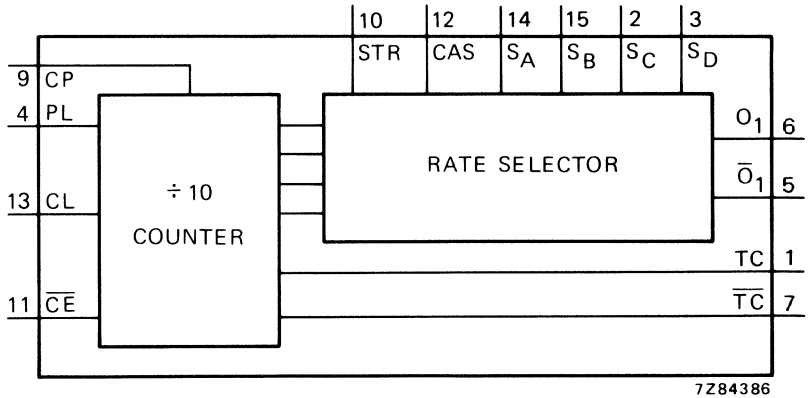
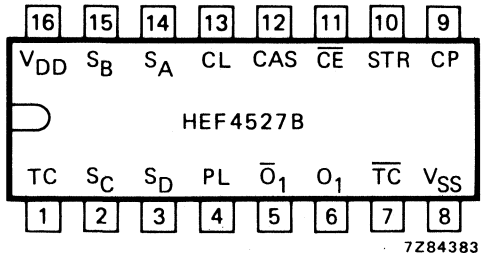


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS catagory MSI

see Family Specifications



HEF4527BP : 16-lead DIL; plastic (SOT-38Z).
HEF4527BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4527BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

PINNING

CP	clock input
PL	preset to '9' input
CL	counter clear input
$\overline{CE}$	count enable input (active LOW)
STR	strobe input
CAS	cascade input
S_A to S_D	rate select inputs
O_1 to $\overline{O}_1$	rate outputs
TC	terminal count output (active HIGH)
$\overline{TC}$	terminal count output (active LOW)

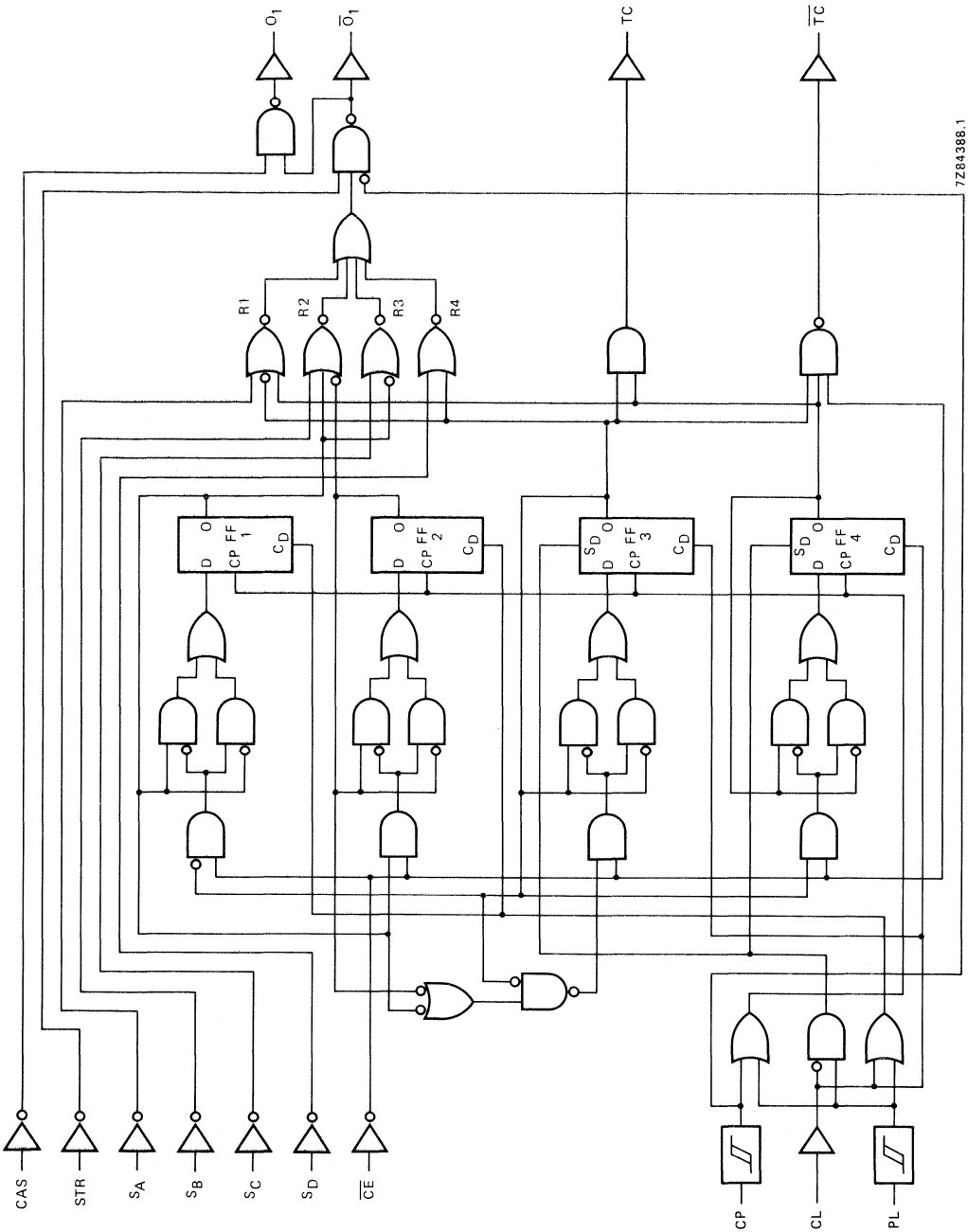


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs										outputs				mode of operation
number of pulses or logic level										number of pulses or logic level				
S_D	S_C	S_B	S_A	CP	$\overline{CE}$	STR	CAS	CL	PL	O_1	$\overline{O}_1$	$\overline{TC}$	TC	
L	L	L	L	10	L	L	L	L	L	L	H	1	1	
L	L	L	H	10	L	L	L	L	L	1	1	1	1	
L	L	H	L	10	L	L	L	L	L	2	2	1	1	
L	L	H	H	10	L	L	L	L	L	3	3	1	1	
L	H	L	L	10	L	L	L	L	L	4	4	1	1	
L	H	L	H	10	L	L	L	L	L	5	5	1	1	rate pulses at
L	H	H	L	10	L	L	L	L	L	6	6	1	1	the outputs
L	H	H	H	10	L	L	L	L	L	7	7	1	1	depend on the
H	L	L	L	10	L	L	L	L	L	8	8	1	1	BCD input
H	L	L	H	10	L	L	L	L	L	9	9	1	1	number at
H	L	H	L	10	L	L	L	L	L	8	8	1	1	S_A to S_D
H	L	H	H	10	L	L	L	L	L	9	9	1	1	
H	H	L	L	10	L	L	L	L	L	8	8	1	1	
H	H	L	H	10	L	L	L	L	L	9	9	1	1	
H	H	H	L	10	L	L	L	L	L	8	8	1	1	
H	H	H	H	10	L	L	L	L	L	9	9	1	1	
X	X	X	X	X	H	L	L	L	L	▲	▲	H	▲	$\overline{CE}$ = H; counter disabled
X	X	X	X	10	L	H	L	L	L	L	H	1	1	outputs O_1 and O_2 disabled
X	X	X	X	10	L	L	H	L	L	H	*	1	1	output O_1 disabled
H	X	X	X	10	L	L	L	H	X	10	10	H	L	CL = H
L	X	X	X	X	L	L	L	H	X	L	H	H	L	counter reset
X	X	X	X	X	L	L	L	L	H	L	H	L	H	PL = H; preset to '9'

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* Same output as the first 16 lines of this function table (depends on the values of S_A to S_D).
▲ Depends on internal state of the counter.

A.C. CHARACTERISTICS $V_{SS} = 0$ V; $T_{amb} = 25\ ^{o}C$; $C_L = 50$ pF; input transition times $\leqslant 20$ ns.

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	typical extrapolation formula
Propagation delays							
CP → O_1, $\overline{O}_1$	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	50	ns	39 ns + (0,23 ns/pF) C_L
	15			35	35	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			160	320	ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
CP → $\overline{TC}$	5			175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
CAS → O_1	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
	5			70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
STR → O_1, $\overline{O}_1$	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$\overline{CE}$ → $\overline{TC}$	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
	5			65	130	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
CL → O_1	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CL → $\overline{O}_1$	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns.

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	typical extrapolation formula
Propagation delays							
PL → O_1, $\overline{O}_1$	5			260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		100	200	ns	89 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			235	470	ns	208 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
Minimum clock	5			45	90	ns	
pulse width	10	t_{WCPH}		18	36	ns	
HIGH	15			12	24	ns	
Minimum CL	5			20	40	ns	
pulse width; HIGH	10	t_{WCLH}		12	24	ns	
	15			10	20	ns	
Minimum PL	5			50	100	ns	
pulse width; HIGH	10	t_{WPLH}		20	40	ns	
	15			15	30	ns	
Set-up times	5		30	15		ns	
$\overline{CE}$ → CP	10	t_{su}	20	10		ns	
	15		12	5		ns	
Recovery times	5		20	10		ns	
CL → CP	10	t_{RCL}	16	8		ns	
	15		10	5		ns	
	5		80	40		ns	
PL → CP	10	t_{RPL}	36	18		ns	
	15		25	10		ns	
Maximum clock	5		4,5	9		MHz	
pulse frequency	10	f_{max}	11	22		MHz	
	15		16	32		MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 050 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	4 500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	10 500 f_i + Σ($f_o C_L$) x V_{DD}^2	

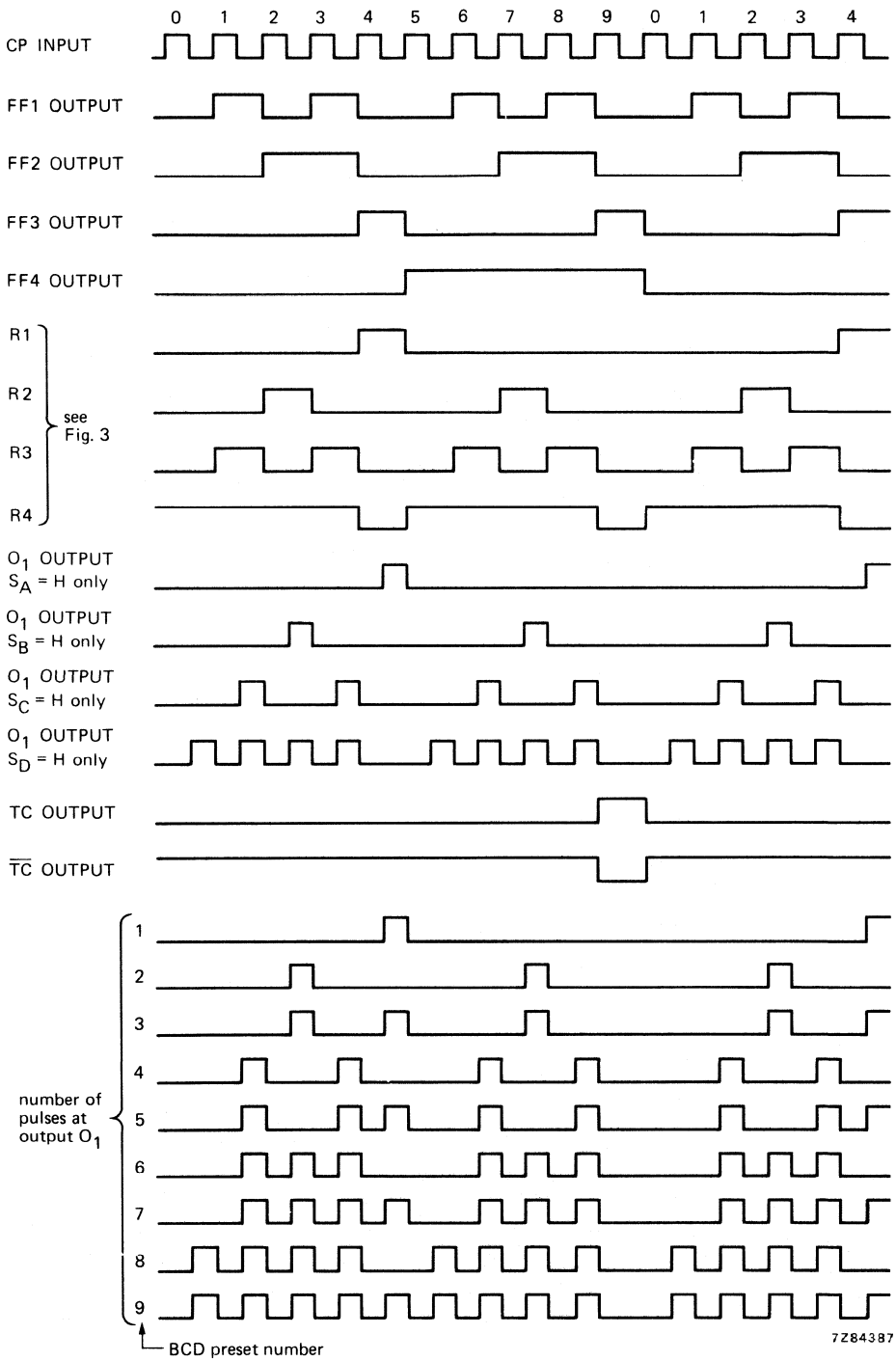


Fig. 4 Timing diagram.

APPLICATION INFORMATION

Add mode

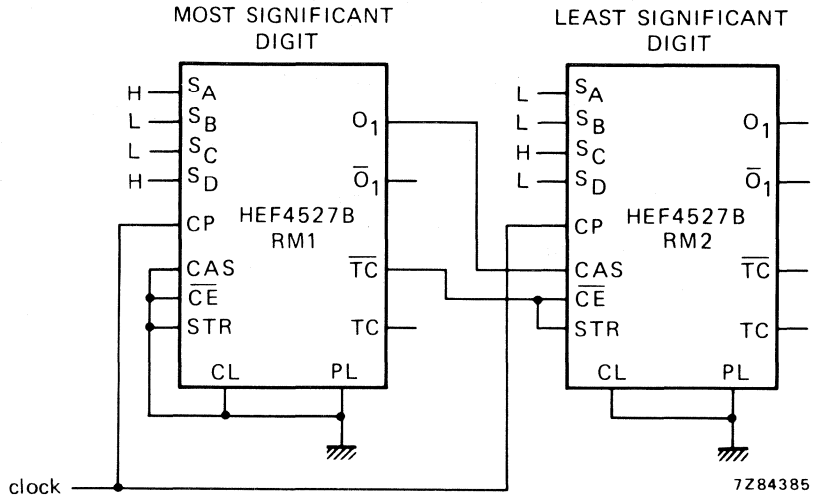


Fig. 5 Two HEF4527B cascaded in the add mode.
Output rate = 10^n (0,1 BCD_1 + 0,01 BCD_2 + 0,01 BCD_3 + ...), in where n = number of cascaded RMs. Example: RM1 preset to 9 and RM2 preset to 4, output rate is 10^2 (0,1 x 9 x 0,01 x 4) = 94.

Multiply mode

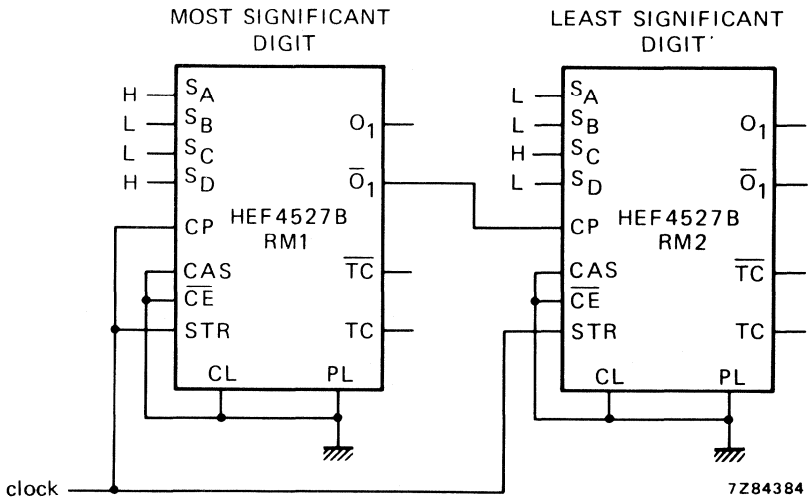


Fig. 6 Two HEF4527B cascaded in the multiply mode.
Output rate = 10^n (0,1 BCD_1 x 0,1 BCD_2 x 0,1 BCD_3 x .....), in where n = number of cascaded RMs.
Example: RM1 preset to 9 and RM2 preset to 4, output rate is 10^2 (0,1 x 9 x 0,1 x 4) = 36.

DUAL MONOSTABLE MULTIVIBRATOR

The HEF4528B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW input ($\overline{I}_0$), and active HIGH input (I_1), an active LOW clear direct input ($\overline{C}_D$), an output (O) and its complement ($\overline{O}$), and two pins for connecting the external timing components (C_{TC},* RC_{TC}).

An external timing capacitor (C_t) must be connected between C_{TC} and RC_{TC} and an external resistor (R_t) must be connected between RC_{TC} and V_{DD}. The duration of the output pulse is determined by the external timing components C_t and R_t.

A HIGH to LOW transition on $\overline{I}_0$ when I_1 is LOW or a LOW to HIGH transition on I_1 when $\overline{I}_0$ is HIGH produces a positive pulse (LOW-HIGH-LOW) on O and a negative pulse (HIGH-LOW-HIGH) on $\overline{O}$ if the $\overline{C}_D$ is HIGH. A LOW on $\overline{C}_D$ forces O LOW, $\overline{O}$ HIGH and inhibits any further pulses until $\overline{C}_D$ is HIGH.

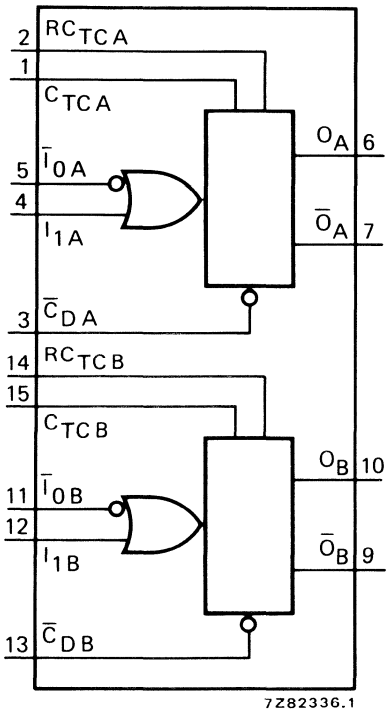


Fig. 1 Functional diagram.

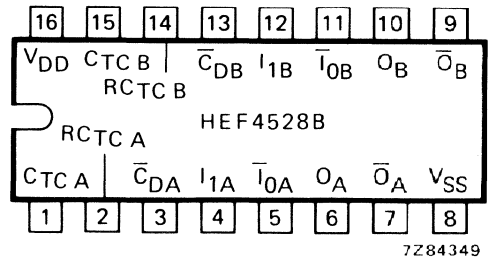


Fig. 2 Pinning diagram.

HEF4528BP : 16-lead DIL; plastic (SOT-38Z).
HEF4528BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4528BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{I}_{0A}$, $\overline{I}_{0B}$	input (HIGH to LOW triggered)
I_{1A}, I_{1B}	input (LOW to HIGH triggered)
$\overline{C}_{DA}$, $\overline{C}_{DB}$	clear direct input (active LOW)
O_A, O_B	output
$\overline{O}_A$, $\overline{O}_B$	complementary output (active LOW)
$C_{TC\,A}$, $C_{TC\,B}$	external capacitor connections*
$RC_{TC\,A}$, $RC_{TC\,B}$	external capacitor/ resistor connections

* Always connected to ground.

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

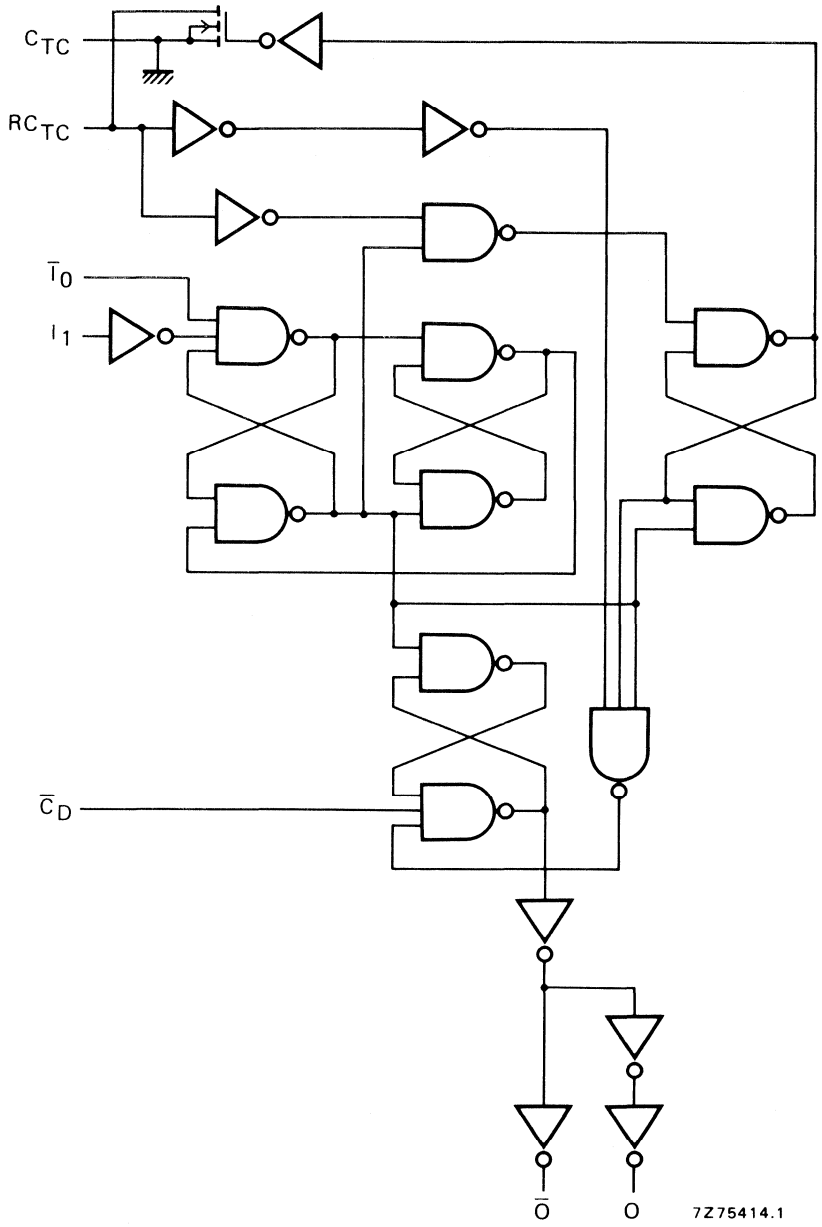


Fig. 3 Logic diagram (one monostable multivibrator).

FUNCTION TABLE

inputs			outputs	
$\overline{I}_0$	I_1	$\overline{C}_D$	O	$\overline{O}$
↘	L	H	⎍	⎎
H	↗	H	⎍	⎎
X	X	L	L	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition
⎍⎎ = positive or negative output pulse; width is determined by C_t and R_t

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{I}_0, I_1 \rightarrow \overline{O}$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{I}_0, I_1 \rightarrow O$	5			155	305	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{C}_D \rightarrow O$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{C}_D \rightarrow \overline{O}$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns; R_t = 5 kΩ; C_t = 15 pF

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$4000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$20\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$59\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 5.

	V_{DD} V	symbol	min.	typ.	max.		
Recovery time for $\overline{C}_D$	5	t_{RCD}	0	−75		ns	
	10		0	−30		ns	
	15		0	−25		ns	
Minimum $\overline{I}_0$ pulse width; LOW	5	t_{WI0L}	50	25		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum I_1 pulse width; HIGH	5	t_{WI1H}	50	25		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum $\overline{C}_D$ pulse width; LOW	5	t_{WCDL}	60	30		ns	
	10		35	15		ns	
	15		25	10		ns	
Set-up time $\overline{C}_D \longrightarrow \overline{I}_0$ or I_1	5	t_{su}	0	−105		ns	to avoid change in output
	10		0	−40		ns	
	15		0	−25		ns	
Output O pulse width; HIGH	5	t_{WOH}	−	235		ns	note 1
	10		−	155		ns	
	15		−	140		ns	
Output O pulse width; HIGH	5	t_{WOH}	−	5,45		μs	note 2
	10		−	4,95		μs	
	15		−	4,85		μs	
Change in output O pulse width over temperature	5	Δt_{WO}	−	±3		%	note 3
	10		−	±2		%	
	15		−	±2		%	
Change in output O pulse width over V_{DD}	5	Δt_{WO}	−	±2		%	V_{DD} ± 5%
	10		−	±1		%	
	15		−	±1		%	
External timing resistor	5	R_t	5	−	2000	kΩ	
	10		5	−	2000	kΩ	
	15		5	−	2000	kΩ	
External timing capacitor	5	C_t	no limits				
	10		no limits				
	15		no limits				

Notes

1. R_t = 5 kΩ; C_t = 15 pF; for other R_t, C_t combinations and $C_t < 0{,}01$ μF see graph Fig. 4.
2. R_t = 10 kΩ; C_t = 1000 pF; for other R_t, C_t combinations and $C_t > 0{,}01$ μF use formula $t_{WO} = K.R_t.C_t$.

   where: t_{WO} = output pulse width (s)
   R_t = external timing resistor (Ω)
   C_t = external timing capacitor (F)

   K = 0,42 for V_{DD} = 5 V
   K = 0,32 for V_{DD} = 10 V
   K = 0,30 for V_{DD} = 15 V
3. T_{amb} = −40 to +85 °C; Δt_{WO} is referenced to t_{WO} at T_{amb} = 25 °C.

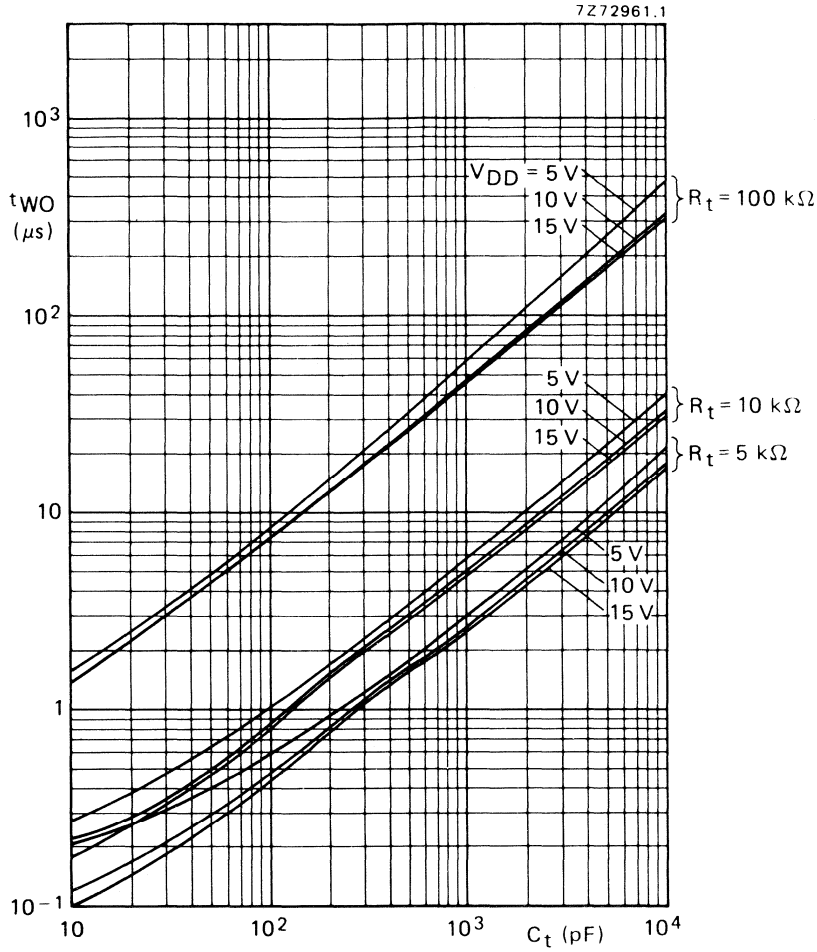


Fig. 4 Output pulse width (t_{WO}) as a function of external timing capacitor (C_t).

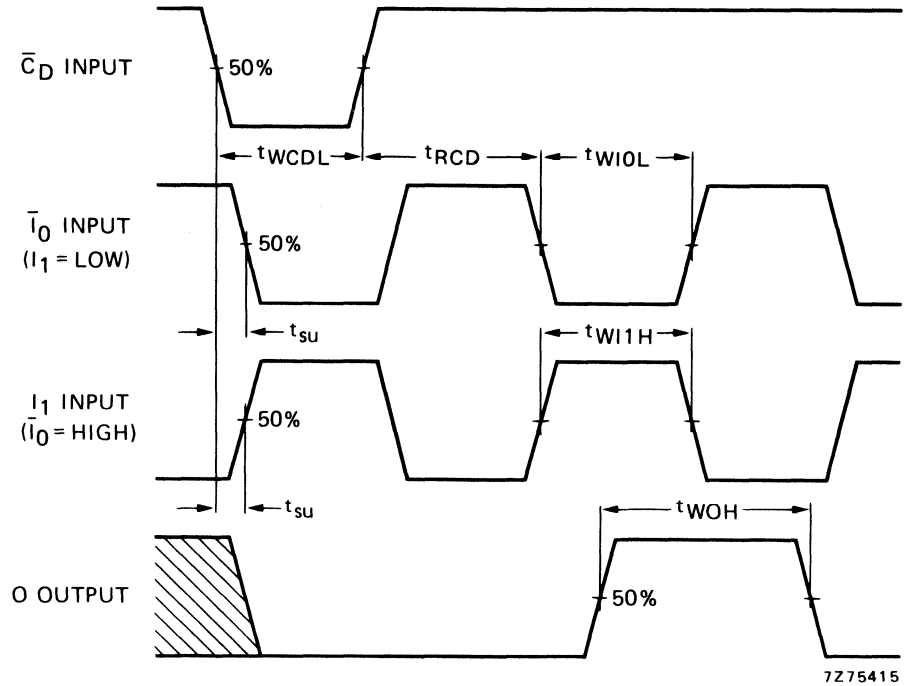


Fig. 5 Waveforms showing minimum $\overline{I}_0$, I_1 and O pulse widths, set-up and recovery times. Set-up and recovery times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

An example of an application for the HEF4528B is:

- Non-retriggerable monostable multivibrator

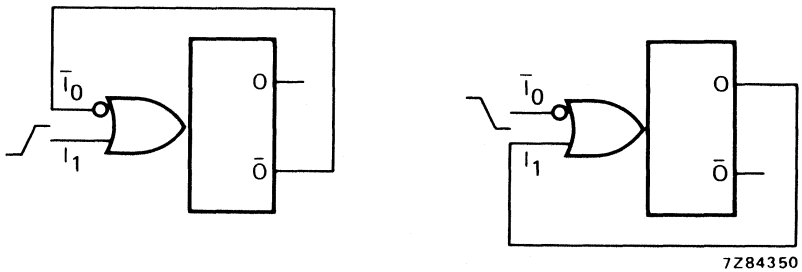


Fig. 6 Two examples for a non-retriggerable monostable multivibrator using half of HEF4528B (LOW to HIGH and HIGH to LOW triggered).

13-INPUT PARITY CHECKER/GENERATOR

The HEF4531B is a parity checker/generator with 13 parity inputs (I_0 to I_{12}) and a parity output (O). When the number of parity inputs that are HIGH is even, the output is LOW. When the number of parity inputs that are HIGH is odd, the output is HIGH. For words of 12 bits or less, the output can be used to generate either odd or even parity by appropriate termination of the unused parity input(s). For words of 14 or more bits, the devices can be cascaded by connecting the output of one device to any parity input of another device. When cascading devices, it is recommended that the output of one device be connected to the I_{12} input of the other device since there is less delay to the output from the I_{12} input than from any other input (I_0 to I_{11}).

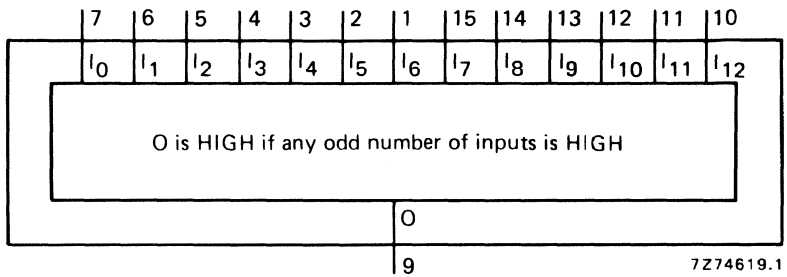


Fig. 1 Functional diagram.

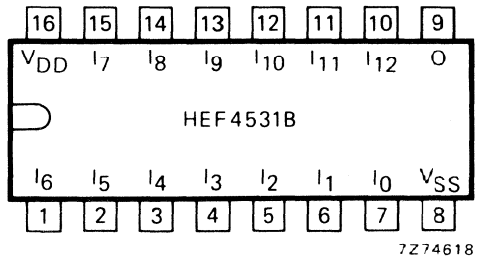


Fig. 2 Pinning diagram.

HEF4531BP : 16-lead DIL; plastic (SOT-38Z).
HEF4531BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4531BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

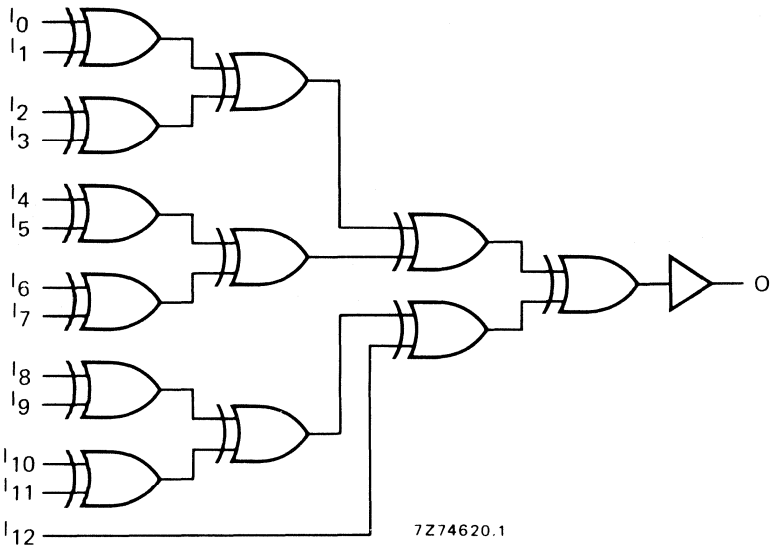


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs													output
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	O
L	L	L	L	L	L	L	L	L	L	L	L	L	L
			any odd number of inputs HIGH										H
			any even number of inputs HIGH										L
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	425 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	2 400 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	7 700 f_i + Σ($f_o C_L$) x V_{DD}^2	

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
I_0 to I_{11} → O	5		145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	60	120	ns	49 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		135	270	ns	108 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	55	110	ns	44 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
I_{12} → O	5		105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	45	90	ns	34 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
	5		85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

8-INPUT PRIORITY ENCODER

The HEF4532B is an 8-input priority encoder with eight active HIGH priority inputs (I_0 to I_7), three active HIGH outputs (O_0 to O_2), an active HIGH enable input (E_{in}), an active HIGH enable output (E_{out}) and an active HIGH group select output (GS).
Data is accepted on inputs I_0 to I_7. The binary code corresponding to the highest priority input (I_0 to I_7) which is HIGH, is generated on O_0 to O_2 if E_{in} is HIGH. Input I_7 is assigned the highest priority. GS is HIGH when one or more priority inputs and E_{in} are HIGH. E_{out} is HIGH when I_0 to I_7 are LOW and E_{in} is HIGH. E_{in}, when LOW, forces all outputs (O_0 to O_2, GS, E_{out}) LOW.

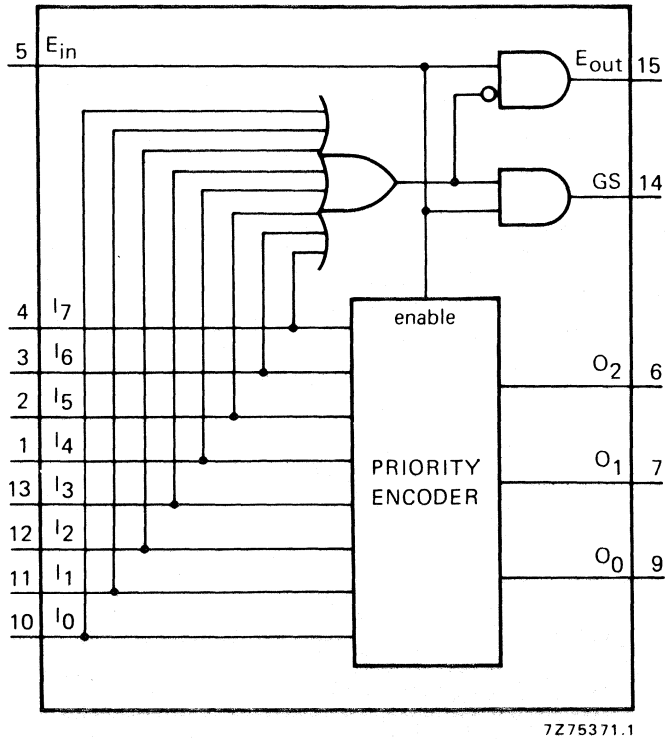


Fig. 1 Functional diagram.

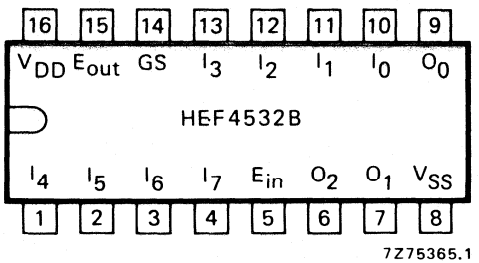


Fig. 2 Pinning diagram.

HEF4532BP : 16-lead DIL; plastic (SOT-38Z).
HEF4532BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4532BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

I_0 to I_7	priority inputs
E_{in}	enable input
E_{out}	enable output
GS	group select output
O_0 to O_2	outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

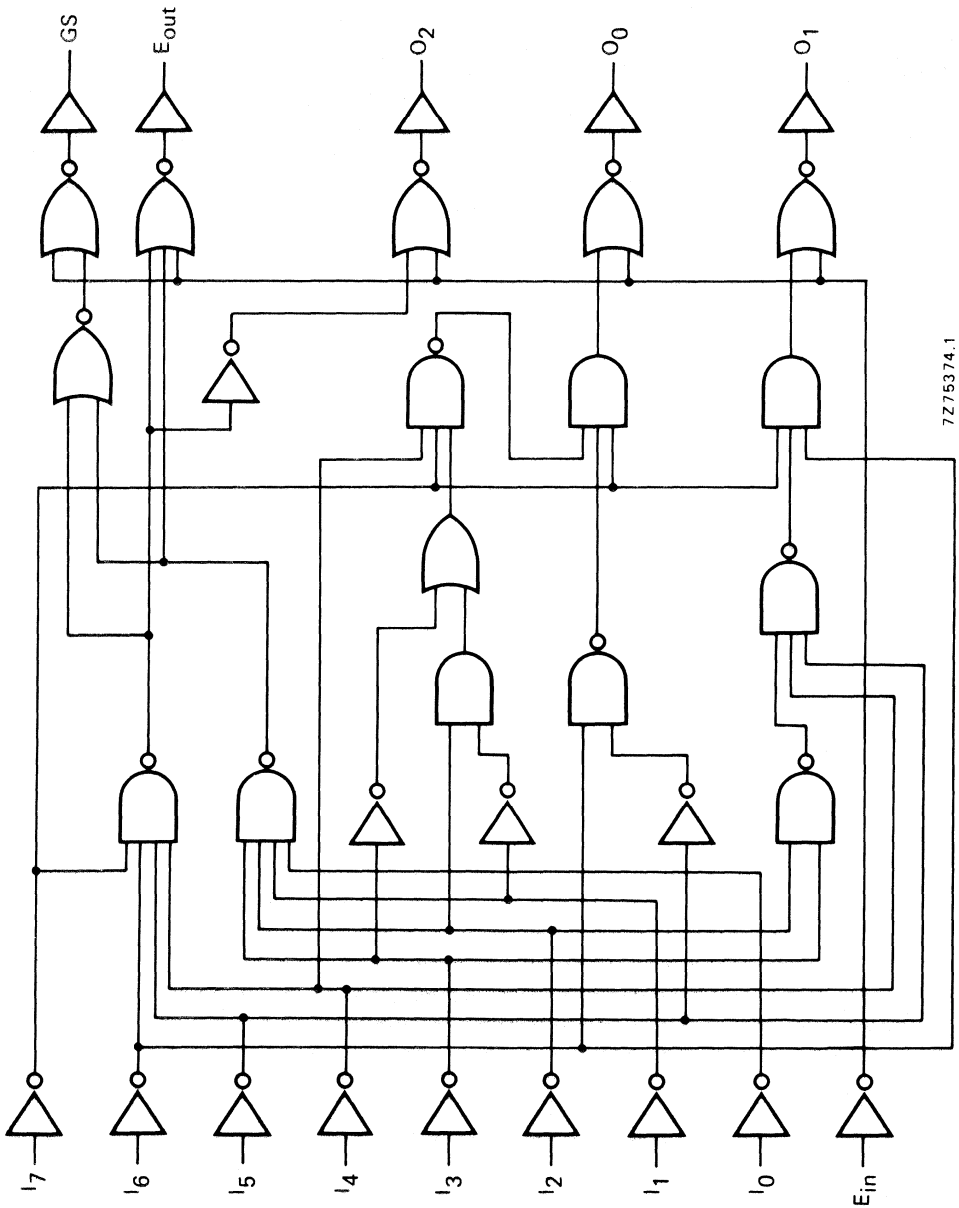


Fig. 3 Logic diagram.

TRUTH TABLE

inputs									outputs				
E_{in}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	O_2	O_1	O_0	E_{out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

LOGIC EQUATIONS

$O_2 = E_{in} \cdot (I_4 + I_5 + I_6 + I_7)$

$O_1 = E_{in} \cdot (I_2 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_6 + I_7)$

$O_0 = E_{in} \cdot (I_1 \cdot \bar{I}_2 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_5 \cdot \bar{I}_6 + I_7)$

$E_{out} = E_{in} \cdot \bar{I}_0 \cdot \bar{I}_1 \cdot \bar{I}_2 \cdot \bar{I}_3 \cdot \bar{I}_4 \cdot \bar{I}_5 \cdot \bar{I}_6 \cdot \bar{I}_7$

$GS = E_{in} \cdot (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7)$

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times $\leqslant 20$ ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,620\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,970\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
E_{in} → E_{out}	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
E_{in} → GS	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
E_{in} → O_n	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
I_n → O_n	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
I_n → GS	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

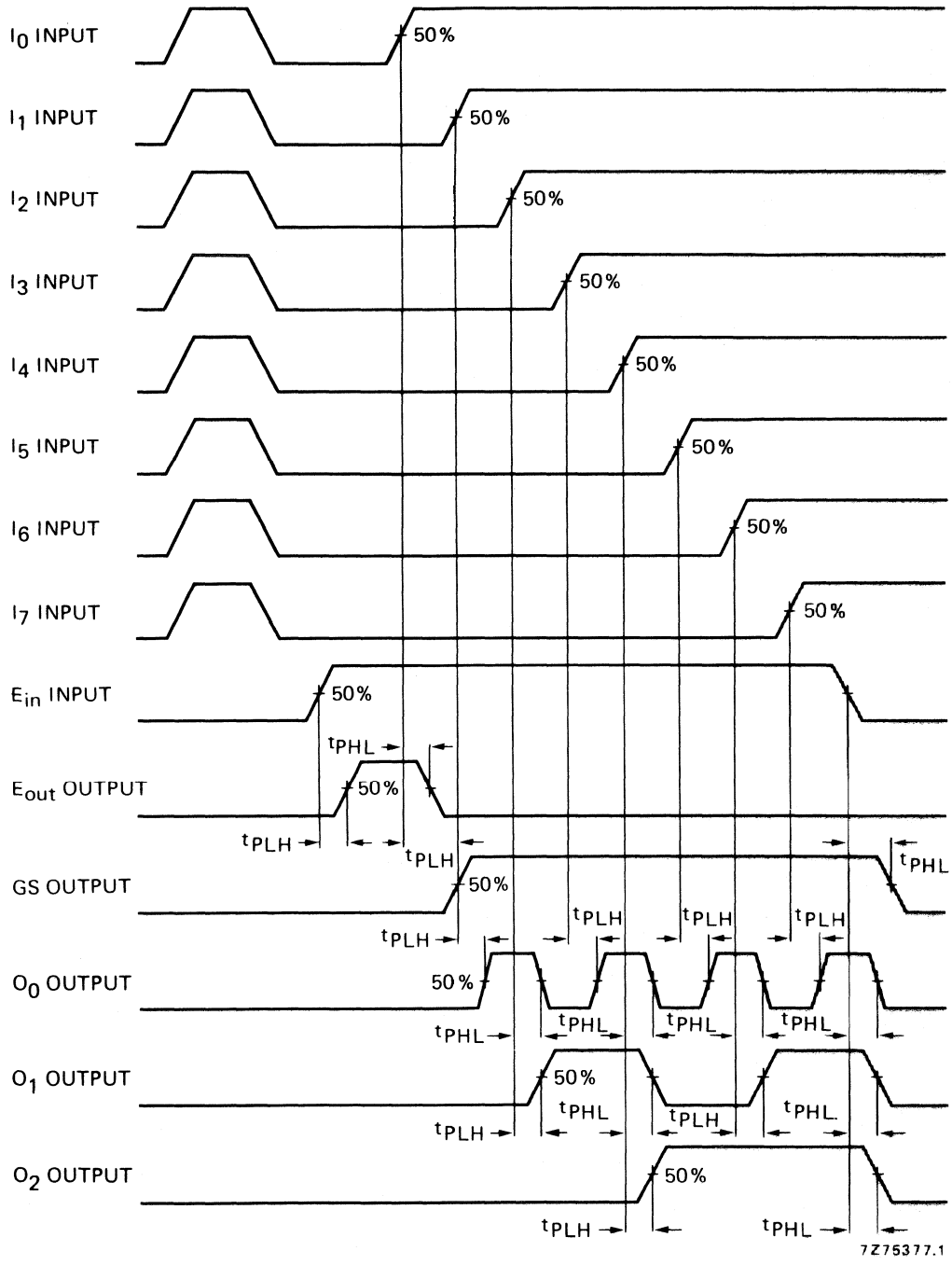


Fig. 4 Waveforms showing propagation delays from inputs to outputs.

APPLICATION INFORMATION

Some examples of applications for the HEF4532B are:

- Priority encoder
- Keyboard encoder

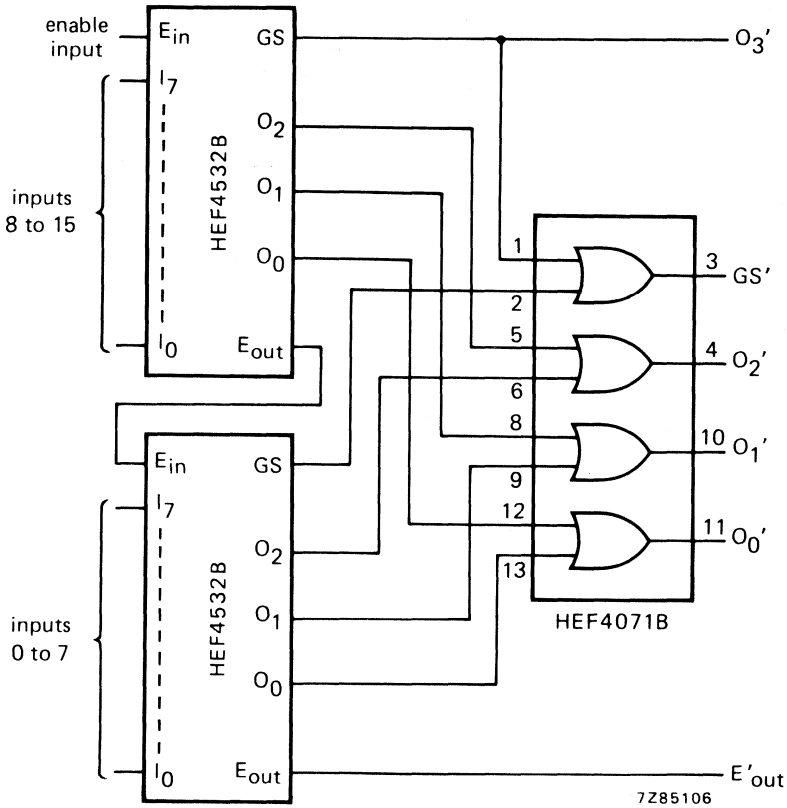


Fig. 5 16-level priority encoder.

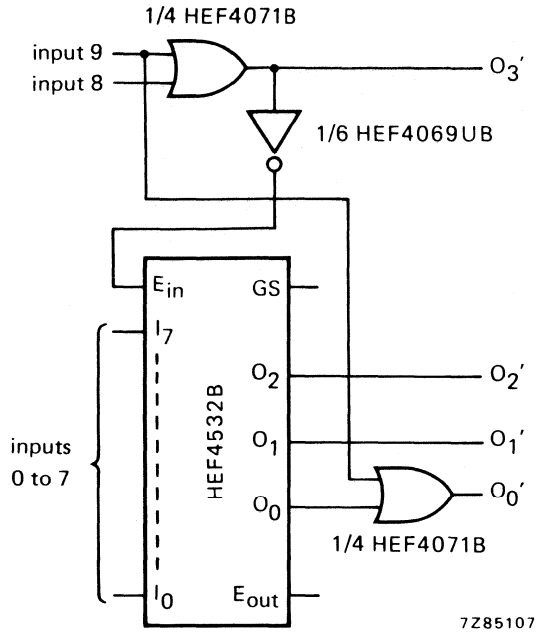


Fig. 6 0-to-9 keyboard encoder.

TRUTH TABLE (for Fig. 6)

inputs										outputs				
9	8	7	6	5	4	3	2	1	0	GS	O_3'	O_2'	O_1'	O_0'
H	X	X	X	X	X	X	X	X	X	L	H	L	L	H
L	H	X	X	X	X	X	X	X	X	L	H	L	L	L
L	L	H	X	X	X	X	X	X	X	H	L	H	H	H
L	L	L	H	X	X	X	X	X	X	H	L	H	H	L
L	L	L	L	H	X	X	X	X	X	H	L	H	L	H
L	L	L	L	L	H	X	X	X	X	H	L	H	L	L
L	L	L	L	L	L	H	X	X	X	H	L	L	H	H
L	L	L	L	L	L	L	H	X	X	H	L	L	H	L
L	L	L	L	L	L	L	L	H	X	H	L	L	L	H
L	L	L	L	L	L	L	L	L	H	H	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

REAL TIME 5-DECADE COUNTER

The HEF4534B is a 5-decade ripple counter. The binary outputs of the decade counters are time-multiplexed by an internal scanner on four BCD outputs (O_0 to O_3). The selected decade is indicated by a logic HIGH on the appropriate digit select output (OS_0: units, 1; OS_1: tens, 10; OS_2: hundreds, 10^2; OS_3: thousands, 10^3; OS_4: ten thousands, 10^4).

The binary outputs (O_0 to O_3) and the select outputs (OS_0 to OS_4) are 3-state controlled via enable inputs $\overline{EO}$ and $\overline{EOS}$ respectively, allowing interface with other bus orientated devices. Cascading may be accomplished by using the carry out (TC). The counter is triggered by a LOW to HIGH transition on the decade clock (CPA) and is reset by a HIGH level on the master reset (MR). The scanner is triggered by a LOW to HIGH transition on the scanner clock (CPS) and is reset (select ten thousand counter) by a HIGH level on the scanner reset (MR_{SC}).

The counter can operate in four modes depending on the state of the mode select inputs (S_A, S_B). The error detector will detect an error when a positive edge on CPA is not accompanied by a negative edge on the error detector clock $\overline{CPE}$ or vice versa, within time limits adjusted by external capacitors connected to $C_{ext\ 1}$ and $C_{ext\ 2}$. Three or more detected errors result in a HIGH level on the error output (OER). The error detector is reset by a HIGH level on MR.

Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.

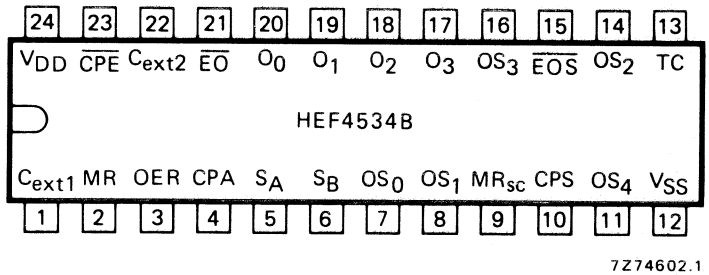


Fig. 1 Pinning diagram.

HEF4534BP : 24-lead DIL; plastic (SOT-101A).
HEF4534BD: 24-lead DIL; ceramic (cerdip) (SOT-94).
HEF4534BT : 24-lead mini-pack; plastic (SO-24; SOT-137A).

PINNING

O_1 to O_3	BCD outputs	$\overline{CPE}$	error detector clock input
OS_0 to OS_3	digit select outputs	S_A, S_B	mode select inputs
OER	error output	MR	master reset input
CPA	decade clock input	MR_{SC}	scanner reset input
CPS	scanner clock input	TC	carry out

FAMILY DATA

I_{DD} LIMITS category LSI } see Family Specifications

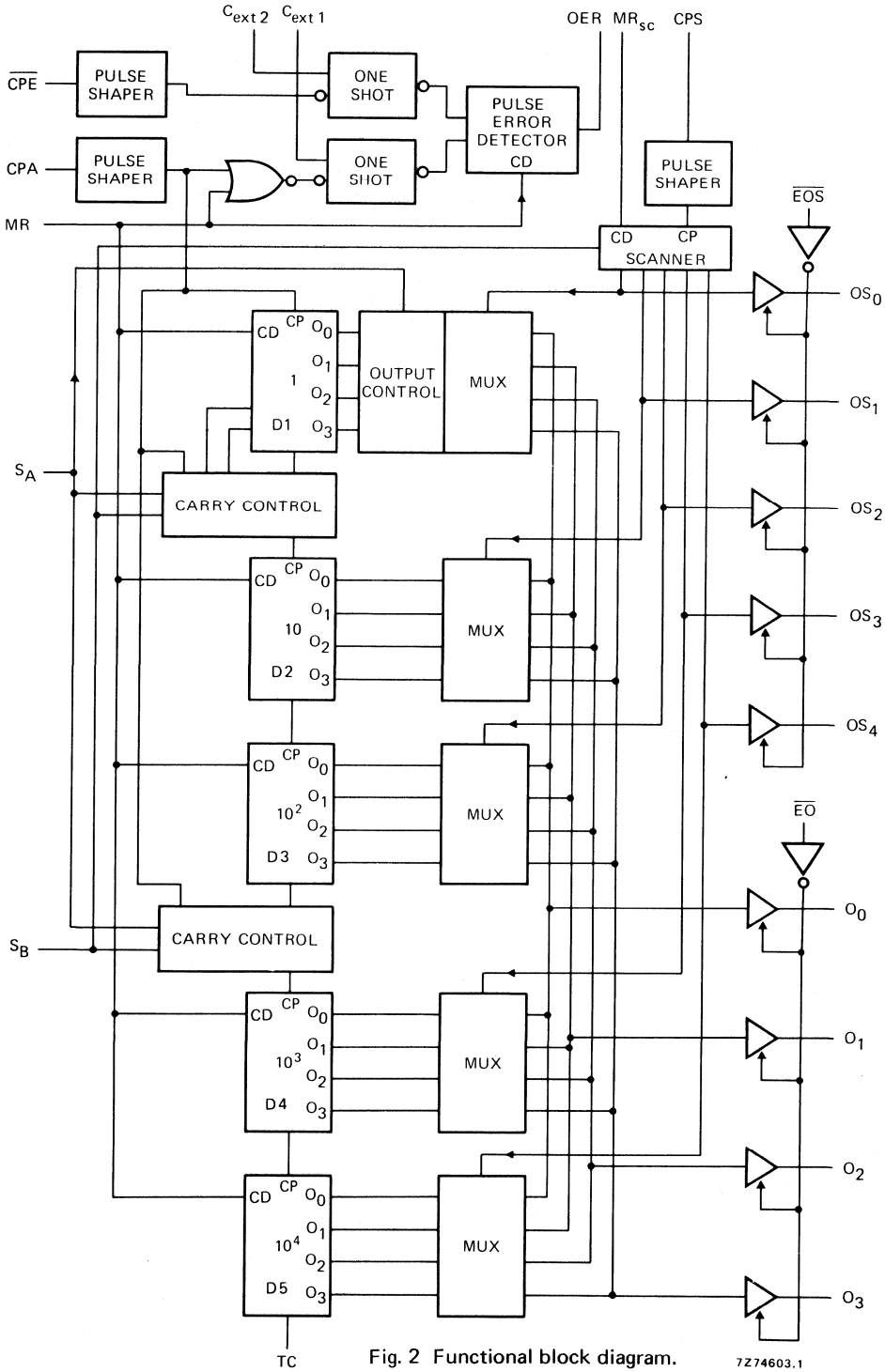


Fig. 2 Functional block diagram.

MODE CONTROL FUNCTION TABLE

select inputs		1st decade output	carry to 2nd stage	carry to 4th stage	mode
S_A	S_B				
L	L	normal count and display	at 9 to 0 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	5-decade counter
L	H	inhibited	input clock	input clock	test purposes: clock directly into stages 1, 2 and 4
H	H	inhibited	at 4 to 5 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	4-decade counter with ÷10 and round-off at front end
H	L	display counts: 3, 4, 5, 6, 7 = 5 8, 9, 0, 1, 2 = 0	at 7 to 8 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	4-decade counter; ½-pence capability

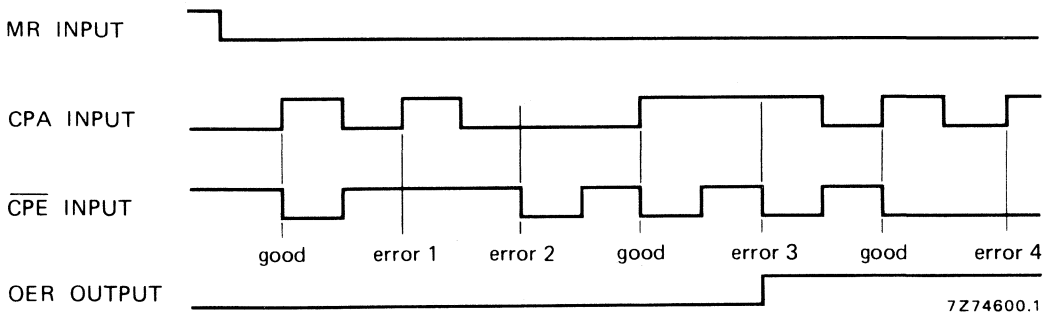


Fig. 3 Error detection timing diagram.

The skew time is the time difference between the LOW to HIGH transition of CPA and the HIGH to LOW transition of $\overline{CPE}$ or vice versa (see Fig. 4). The skew time is typically proportional to the external capacitor (C_{ext}) connected from C_{ext1} and C_{ext2} (pins 1 and 22) to V_{SS}. The error detector will count an error when a positive edge on the counter clock CPA is not succeeded by a negative edge on the error detector clock $\overline{CPE}$ within a skew time t_{SK1} (adjustable by C_{ext1} at pin 1). The same holds for a negative edge at $\overline{CPE}$ succeeded by a positive on CPA within a skew time t_{SK2} (adjustable by C_{ext2} at pin 22). If error detection is not needed, $\overline{CPE}$ must be either HIGH or LOW and no C_{ext} is applied. For further information see Fig. 5.

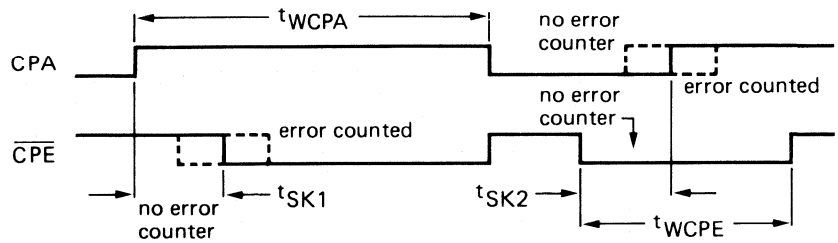


Fig. 4 Skew times timing diagram; $t_{WCPA} > t_{SK1}$; $t_{WCPE} > t_{SK2}$.

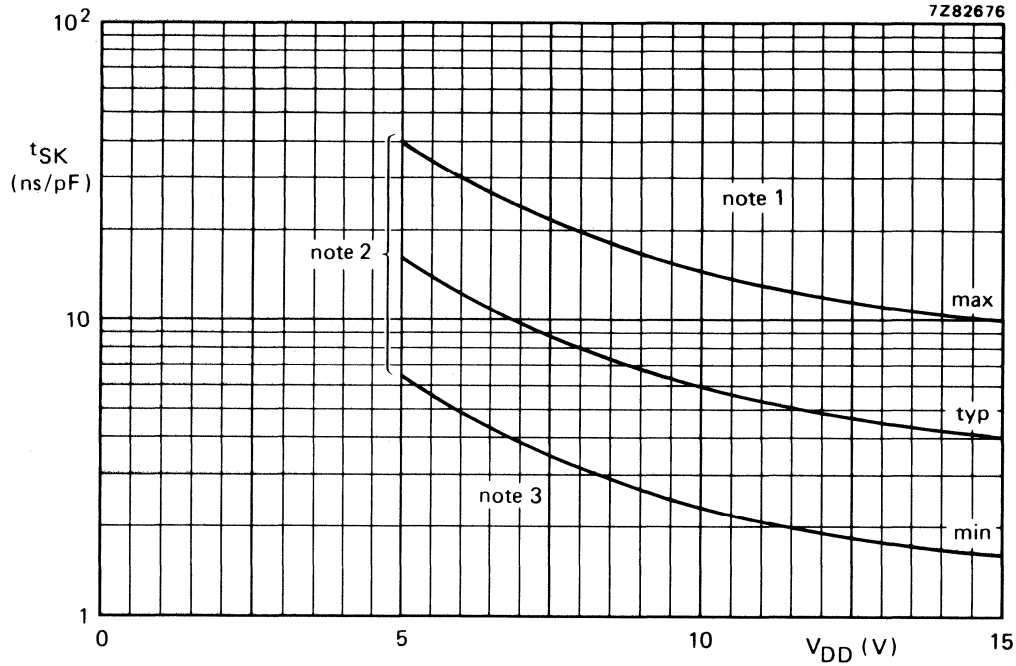


Fig. 5 Typical clock skew as a function of the supply voltage. This graph is accurate for $C_{ext} \geqslant 100$ pF and $T_{amb} = 25\ ^{o}C$.

Notes to Fig. 5

1. Skew in this area results in counted error.
2. Skew in the area between max. and min. curves may or may not result in counted error.
3. Skew in this area results in no error counted.

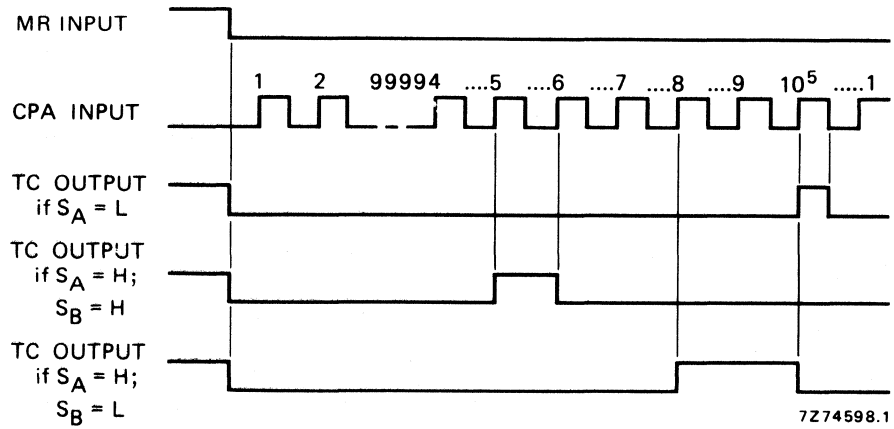


Fig. 6 Carry timing diagram.

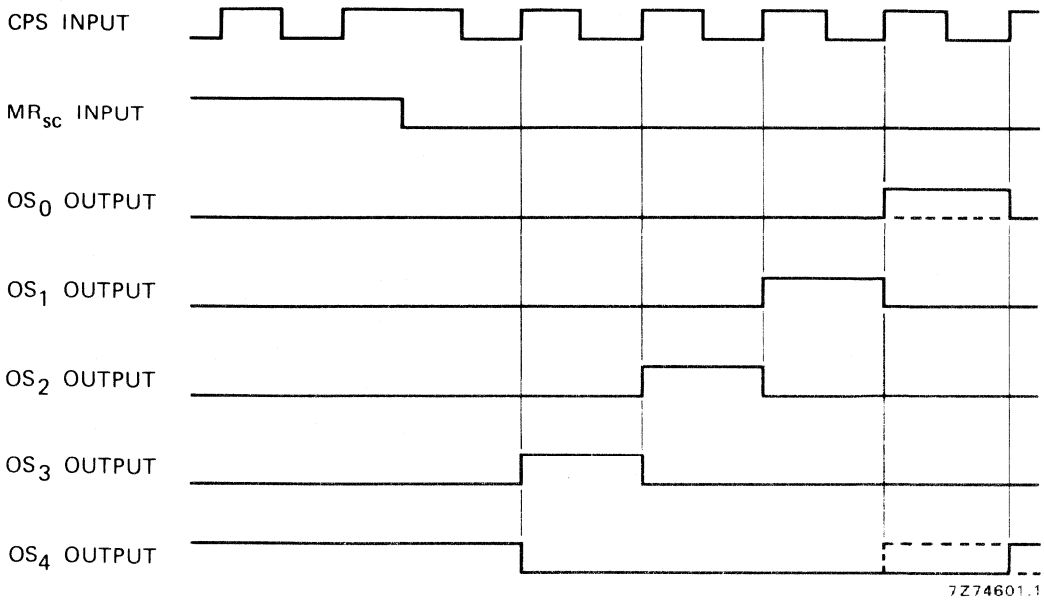


Fig. 7 Scanner timing diagram.

Note: If S_B = H, the 1st decade is inhibited and the cycle will be shortened to four stages (see dotted lines).

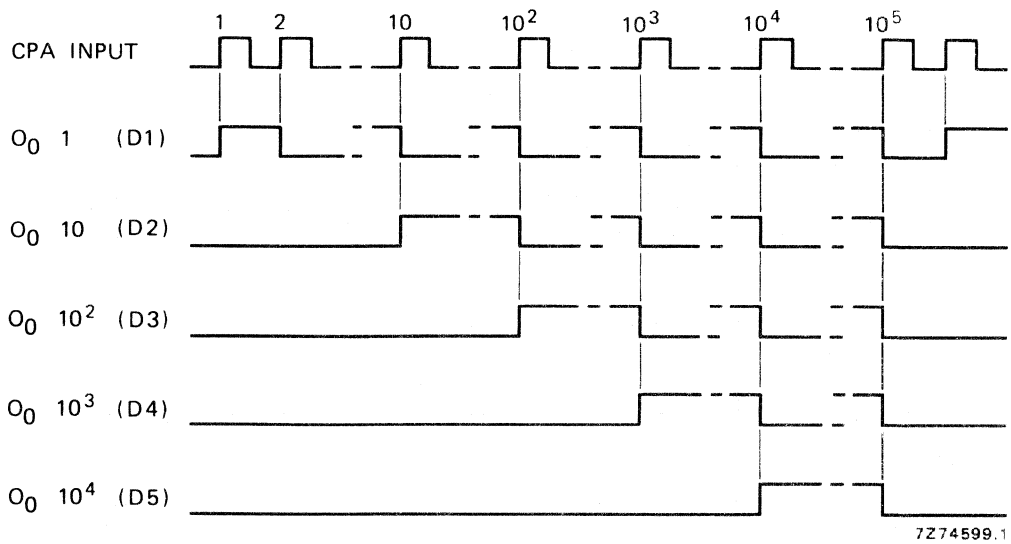


Fig. 8 Counter timing diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CPA → O_n	5			300	600	ns	283 ns + (0,55 ns/pF) C_L
D1 selected	10	t_{PHL}		130	260	ns	119 ns + (0,23 ns/pF) C_L
HIGH to LOW	15			95	190	ns	87 ns + (0,16 ns/pF) C_L
	5			240	480	ns	213 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		100	200	ns	89 ns + (0,23 ns/pF) C_L
	15			75	150	ns	67 ns + (0,16 ns/pF) C_L
CPA → O_n	5			550	1100	ns	523 ns + (0,55 ns/pF) C_L
D5 selected	10	t_{PHL}		230	460	ns	219 ns + (0,23 ns/pF) C_L
HIGH to LOW	15			170	340	ns	162 ns + (0,16 ns/pF) C_L
	5			550	1100	ns	523 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		230	460	ns	219 ns + (0,23 ns/pF) C_L
	15			170	340	ns	162 ns + (0,16 ns/pF) C_L
CPA → TC	5			420	840	ns	393 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		190	380	ns	179 ns + (0,23 ns/pF) C_L
	15			140	280	ns	132 ns + (0,16 ns/pF) C_L
MR → O_n	5			200	400	ns	173 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
MR → OER	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CPS → O_n	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		95	190	ns	84 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		95	190	ns	84 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
CPS → OS_n	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CPA → OS_n	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	
3-state propagation delays						
Output disable times						
$\overline{EO} \rightarrow O_n$;	5			30	60	ns
$\overline{EOS} \rightarrow OS_n$	10	t_{PHZ}		25	50	ns
HIGH	15			20	40	ns
	5			40	80	ns
LOW	10	t_{PLZ}		25	50	ns
	15			20	40	ns
Output enable times						
$\overline{EO} \rightarrow O_n$;	5			35	70	ns
$\overline{EOS} \rightarrow OS_n$	10	t_{PZH}		20	40	ns
HIGH	15			15	30	ns
	5			50	100	ns
LOW	10	t_{PZL}		25	50	ns
	15			15	30	ns
Minimum clock pulse	5		70	35		ns
width; CPA, CPS	10	t_{WCPH}	40	20		ns
HIGH	15		30	15		ns
Minimum reset pulse	5		90	45		ns
width; MR, MR_{sc}	10	t_{WMRH}	60	30		ns
HIGH	15		40	20		ns
Recovery time	5		120	60		ns
for MR	10	t_{RMR}	60	30		ns
	15		50	25		ns
Recovery time	5		60	30		ns
for MR_{sc}	10	t_{RMR}	40	20		ns
	15		30	15		ns
Maximum clock	5		2,5	5		MHz
pulse frequency	10	f_{max}	6	12		MHz
CPA and CPS	15		8	16		MHz

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)*	5	$1\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$12\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

* C_{ext} = 0.

APPLICATION INFORMATION

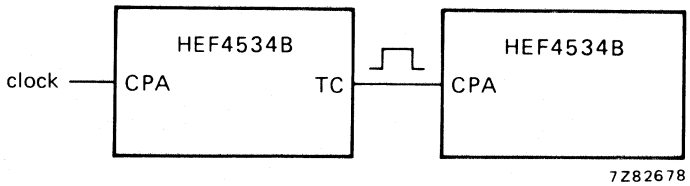


Fig. 9 Two HEF4534B ICs connected for cascade operation. TC is HIGH for a single clock period when all five BCD decades go to zero. TC also goes HIGH when MR is applied.

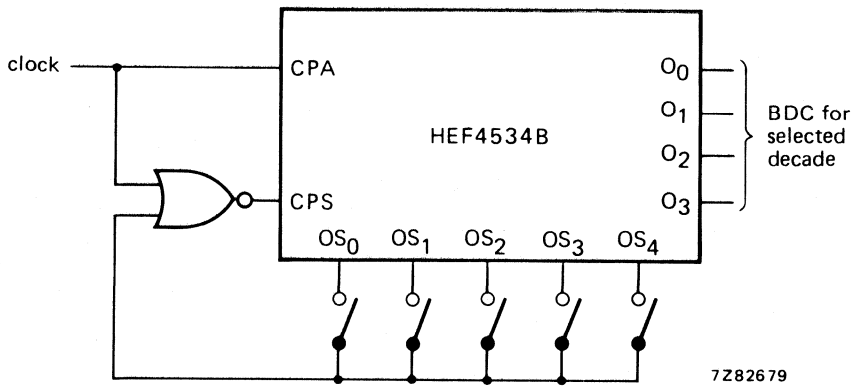


Fig. 10 Forcing a decade to the O_n outputs. When the O_n outputs of a given decade are required, this configuration will lock-up the selected decade within four clock cycles. The select line feed back may be hardwired or switched.

SUPERSEDES DATA OF MAY 1983

DUAL PRECISION MONOSTABLE MULTIVIBRATOR

The HEF4538B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger/retrigger input ($\overline{I}_0$), an active HIGH trigger/retrigger input (I_1), an overriding active LOW direct reset input ($\overline{C}_D$), an output (O) and its complement ($\overline{O}$), and two pins (C_{TC}; RC_{TC}) for connecting the external timing components C_t and R_t. Typical pulse width variation over temperature range is ± 0,2%.

The HEF4538B may be triggered by either the positive or the negative edges of the input pulse and will produce an accurate output pulse with a pulse width range of 10 μs to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t. The output pulse width (T) is equal to $R_t \times C_t$. The linear design techniques in LOCMOS guarantee precise control of the output pulse width.

A LOW level at $\overline{CE}$ terminates the output pulse immediately.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

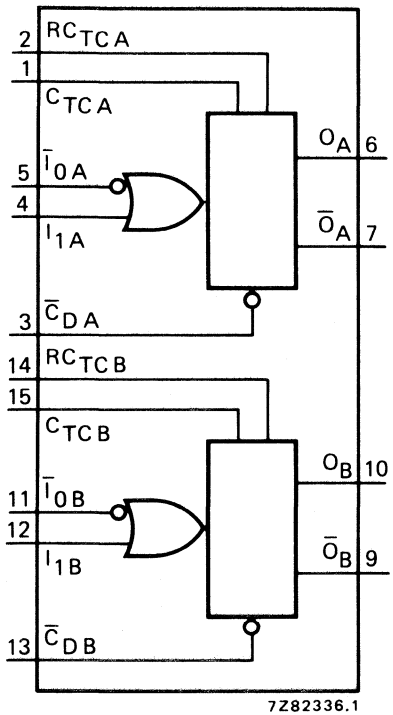


Fig. 1 Functional diagram.

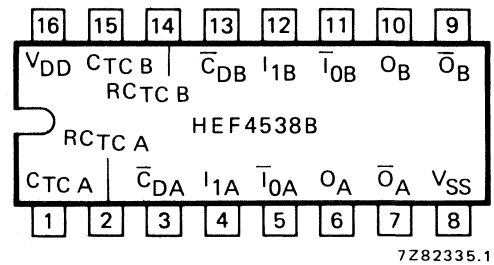


Fig. 2 Pinning diagram.

HEF4538BP : 16-lead DIL; plastic (SOT-38Z).
HEF4538BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4538BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{I}_{0A}$, $\overline{I}_{0B}$	input (HIGH to LOW triggered)
I_{1A}, I_{1B}	input (LOW to HIGH triggered)
$\overline{C}_{DA}$, $\overline{C}_{DB}$	direct reset input (active LOW)
O_A, O_B	output
$\overline{O}_A$, $\overline{O}_B$	complementary output (active LOW)
$C_{TC\,A}$, $C_{TC\,B}$	external capacitor connections*
$RC_{TC\,A}$, $RC_{TC\,B}$	external capacitor/ resistor connections

* Always connected to ground.

FAMILY DATA; I_{DD} LIMITS category MSI: see Family specifications.

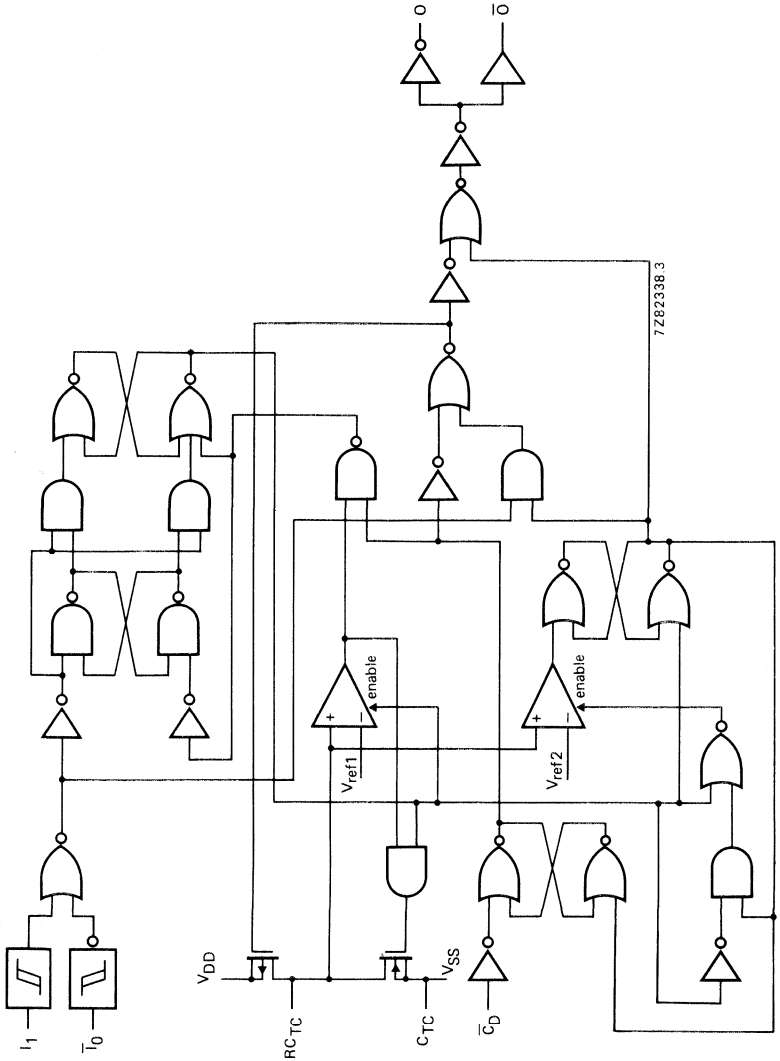


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs			outputs	
$\overline{I}_0$	I_1	$\overline{C}_D$	O	$\overline{O}$
↘	L	H	⎍	⎎
H	↗	H	⎍	⎎
X	X	L	L	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition
⎍ = positive output pulse
⎎ = negative output pulse

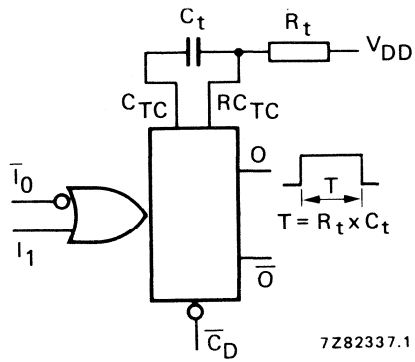


Fig. 4 Connection of the external timing components R_t and C_t.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 typ.	−40 max.	+25 typ.	+25 max.	+85 typ.	+85 max.	
Supply current active state (see note)	5	I_D			55				μA
	10				150				μA
	15				220				μA
Input leakage current (pins 2 and 14)	15	$\pm I_{IN}$				300		1000	nA

Note
Only one monostable is switching: current present during output pulse (output O is HIGH).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{I}_0, I_1 \rightarrow O$	5			200	460	ns	173 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$\overline{I}_0, I_1 \rightarrow \overline{O}$	5			220	440	ns	193 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		85	190	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$\overline{C}_D \rightarrow O$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{C}_D \rightarrow \overline{O}$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Recovery times	5			20	40	ns	
$\overline{C}_D \rightarrow \overline{I}_0, I_1$	10	t_{RCD}		10	20	ns	
	15			5	10	ns	
Retrigger times	5		0			ns	
$O, \overline{O} \rightarrow \overline{I}_0, I_1$	10	t_{RO}	0			ns	
	15		0			ns	
Minimum $\overline{I}_0$	5		90	45		ns	
pulse width; LOW	10	t_{WI0L}	30	15		ns	
	15		24	12		ns	
Minimum I_1	5		50	25		ns	
pulse width; HIGH	10	t_{WI1H}	24	12		ns	
	15		20	10		ns	
Minimum $\overline{C}_D$	5		55	25		ns	
pulse width; LOW	10	t_{WCDL}	25	12		ns	
	15		20	10		ns	
Output O or $\overline{O}$	5		218	230	242	µs	R_t = 100 kΩ; C_t = 0,002 µF
pulse width	10	t_{WO}	213	224	235	µs	
	15		211	223	234	µs	
Output O or $\overline{O}$	5		10,3	10,8	11,3	ms	R_t = 100 kΩ; C_t = 0,1 µF
pulse width	10	t_{WO}	10,2	10,7	11,2	ms	
	15		10,1	10,6	11,1	ms	
Output O or $\overline{O}$	5		1,01	1,09	1,11	s	R_t = 100 kΩ; C_t = 10 µF
pulse width	10	t_{WO}	0,99	1,04	1,09	s	
	15		0,99	1,04	1,09	s	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Change in output O pulse width over temperature (T_{amb})	5	Δt_{WO}		± 0,2		%	
	10			± 0,2		%	
	15			± 0,2		%	
Change in output O pulse width over V_{DD} range 5 to 15 V		Δt_{WO}		± 1,5		%	
Pulse width variation between circuits in same package	5	Δt_{WO}		± 1		%	R_t = 100 kΩ C_t = 2 nF to 10 μF
	10			± 1		%	
	15			± 1		%	
External timing resistor		R_t	5	–	*	kΩ	
External timing capacitor		C_t	2000	–	no limits	pF	
Input capacitance (pin 2 or 14)		C_{IN}		15		pF	

* The maximum permissible resistance R_t, which holds the specified accuracy of t_{WO}, depends on the leakage current of the capacitor C_t and the leakage of the HEF4538B.

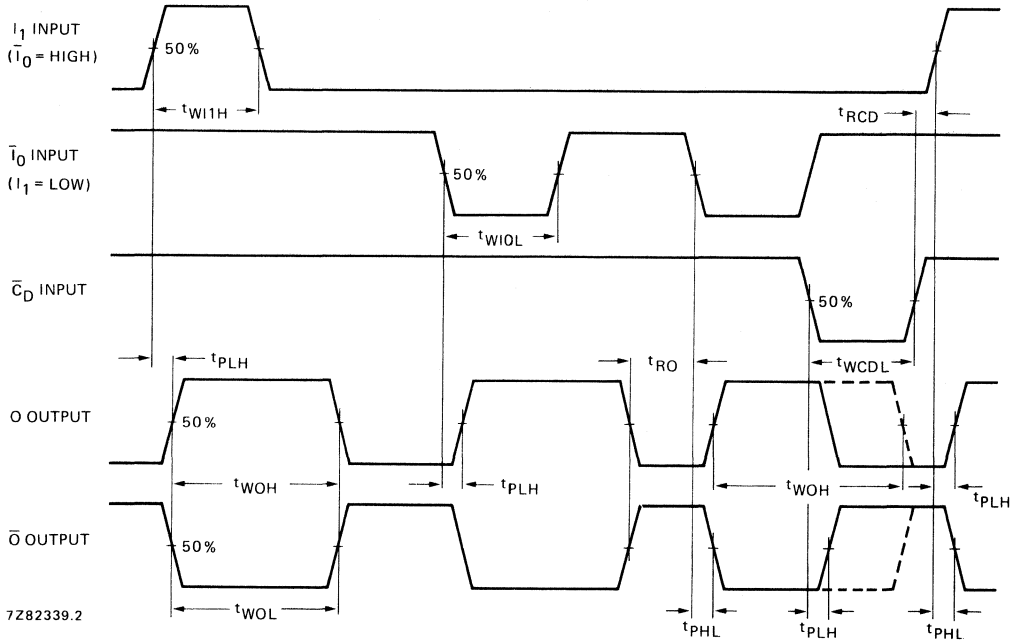
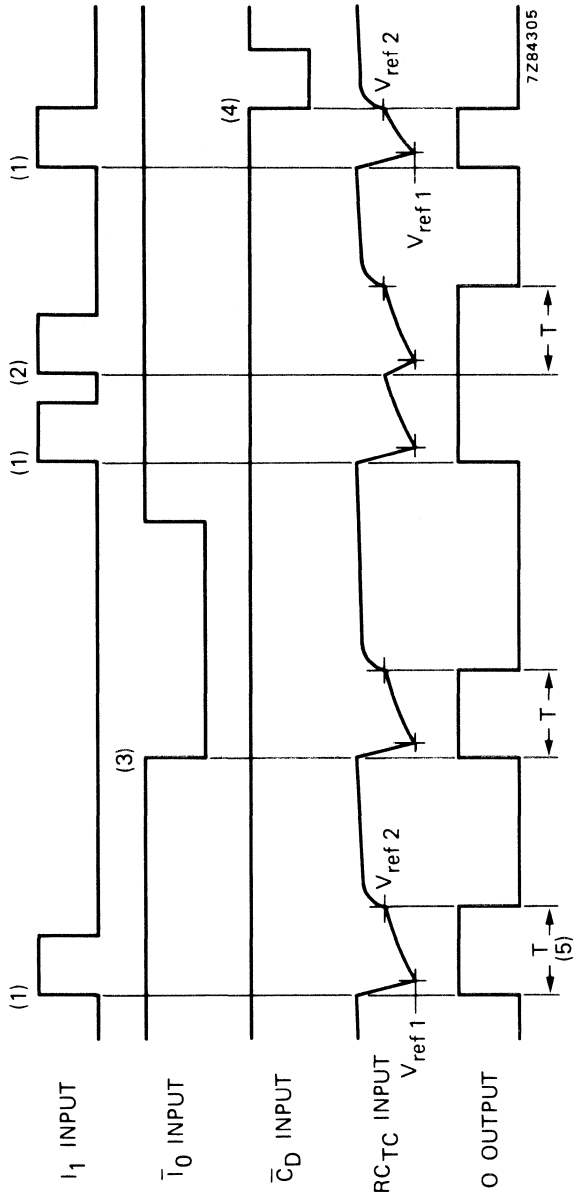
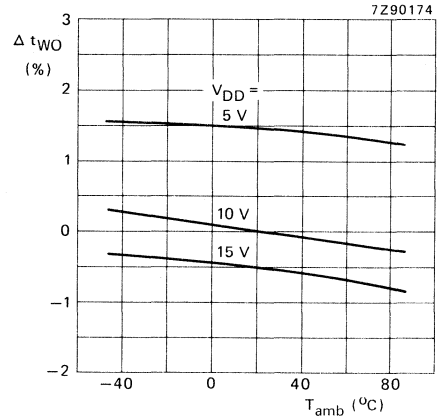


Fig. 5 Waveforms showing minimum $\overline{I}_0$, I_1, O and $\overline{C}_D$ pulse widths, recovery times and propagation delays.

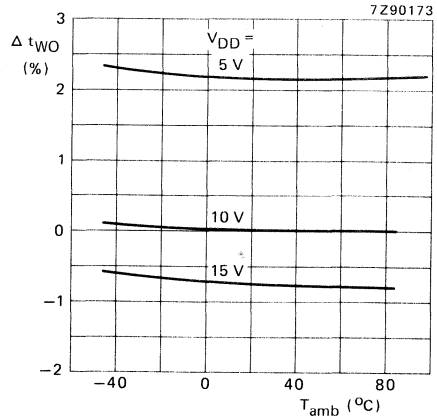


(1) Positive edge triggering.
(2) Positive edge re-triggering (pulse lengthening).
(3) Negative edge triggering.
(4) Reset (pulse shortening).
(5) $T = R_t \times C_t$.

Fig. 6 Timing diagram.



(a)



(b)

Fig. 7 Typical normalized change in output pulse width as a function of ambient temperature; 0% at V_{DD} = 10 V and T_{amb} = 25 °C.
(a) R_t = 100 kΩ; C_t = 100 nF. (b) R_t = 100 kΩ; C_t = 2 nF.

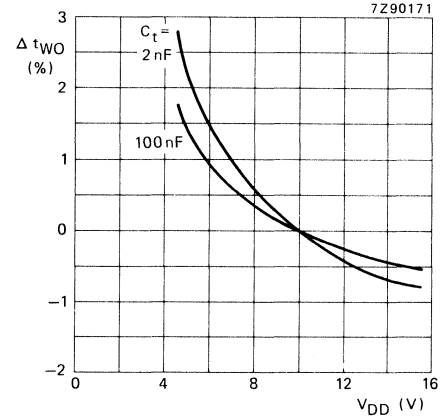


Fig. 8 Typical normalized change in output pulse width as a function of the supply voltage at T_{amb} = 25 °C; 0% at V_{DD} = 10 V; R_t = 100 kΩ.

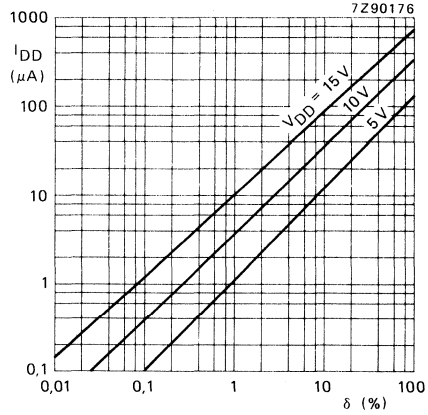


Fig. 9 Total supply current as a function of the output duty factor; R_t = 100 kΩ; C_t = 100 nF; C_L = 50 pF. One monostable multivibrator switching only.

DUAL 4-INPUT MULTIPLEXER

The HEF4539B is a dual 4-input multiplexer with common select logic. Each multiplexer has four multiplexer inputs (I_0 to I_3), an active LOW enable input ($\overline{E}$) and a multiplexer output (O). When HIGH, $\overline{E}$ forces O of the respective multiplexer LOW, independent of the select inputs (S_0 and S_1) and I_0 to I_3. When $\overline{E}$ is LOW, S_0 and S_1 determine which multiplexer input (I_0 to I_3) on each of the multiplexers is routed to the respective multiplexer output (O).

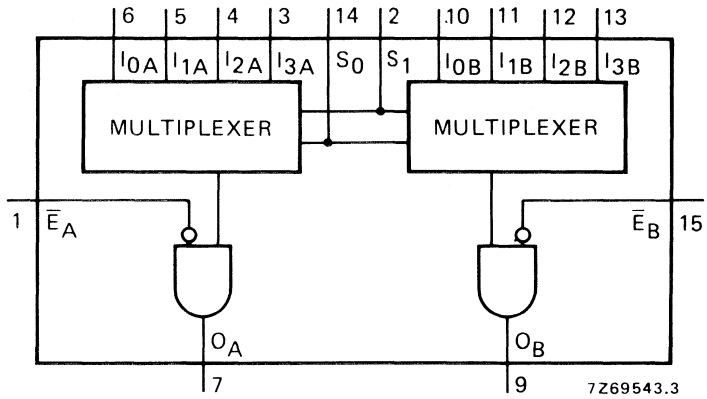


Fig. 1 Functional diagram.

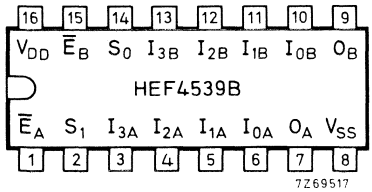


Fig. 2 Pinning diagram.

HEF4539BP : 16-lead DIL; plastic (SOT-38Z).
HEF4539BD : 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4539BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

I_{0A}, I_{1A}, I_{2A}, I_{3A}	multiplexer inputs
I_{0B}, I_{1B}, I_{2B}, I_{3B}	multiplexer inputs
S_0, S_1	select inputs
$\overline{E}_A$, $\overline{E}_B$	enable inputs (active LOW)
O_A, O_B	multiplexer outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Products approved to CECC 90 104-081.

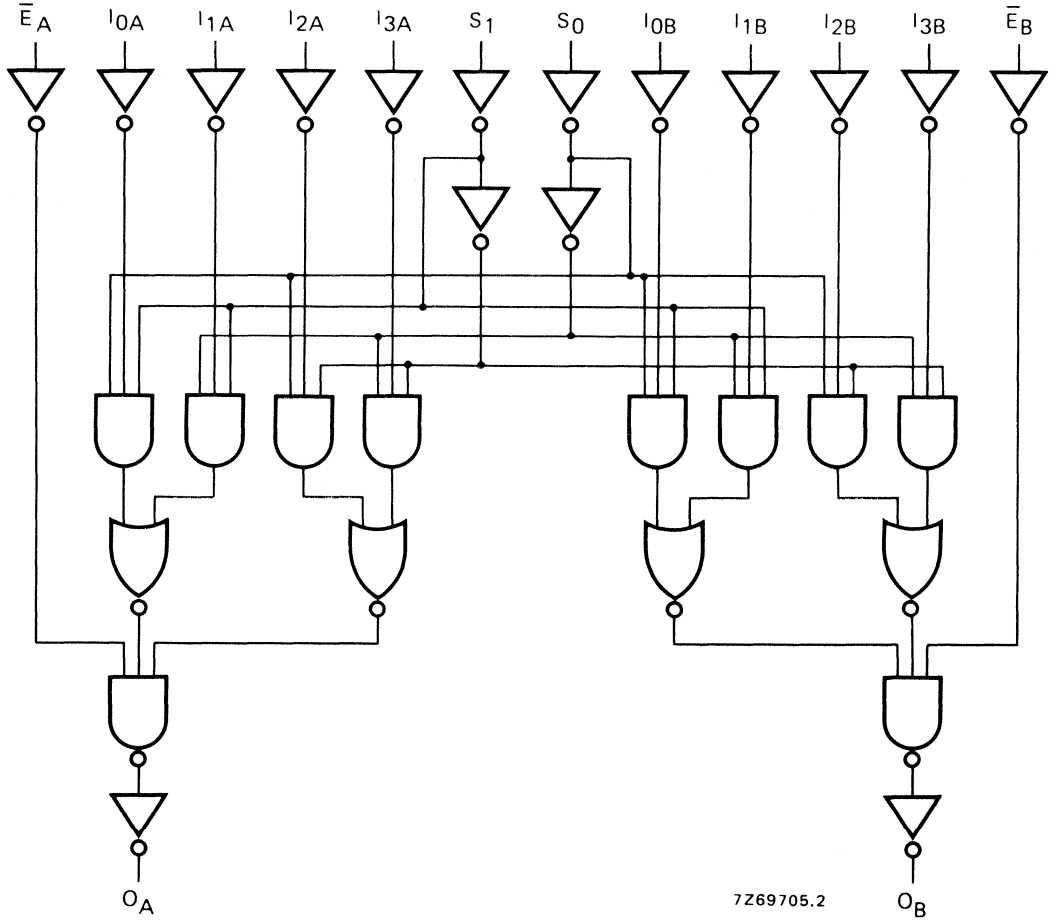


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs			output
S_0	S_1	$\overline{E}_n$	O_n
X	X	H	L
L	L	L	I_0
H	L	L	I_1
L	H	L	I_2
H	H	L	I_3

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$I_n \rightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			120	245	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
$S_n \rightarrow O_n$	5			165	330	ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	125	ns	54 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			155	310	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{E}_n \rightarrow O_n$	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$8100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

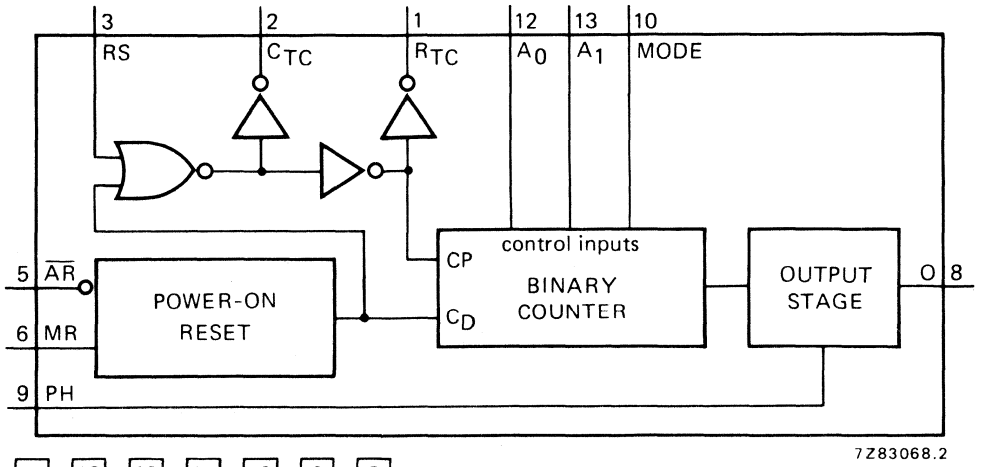
Some examples of applications for the HEF4539B are:

- Data selectors.
- Data multiplexers.

PROGRAMMABLE TIMER

The HEF4541B is a programmable timer which consists of a 16-stage binary counter, an integrated oscillator to be used with external timing components, an automatic power-on reset and output control logic. The frequency of the oscillator is determined by the external components R_t and C_t within the frequency range 1 Hz to 100 kHz. This oscillator may be replaced by an external clock signal at input RS, the timer advances on the positive-going transition of RS. A LOW on the auto reset input ($\overline{AR}$) and a LOW on the master reset input (MR) enables the internal power-on reset. A HIGH level at input MR resets the counter independent on all other inputs. Resetting disables the oscillator to provide no active power dissipation.

A HIGH at input $\overline{AR}$ turns off the power-on reset to provide a low quiescent power dissipation of the timer. The 16-stage counter divides the oscillator frequency by 2^8, 2^{10}, 2^{13} or 2^{16} depending on the state of the address inputs (A_0, A_1). The divided oscillator frequency is available at output O. The phase input (PH) features a complementary output signal. If the mode select input (MODE) is LOW or HIGH the timer can be used respectively as a single transition timer or 2^n frequency divider.



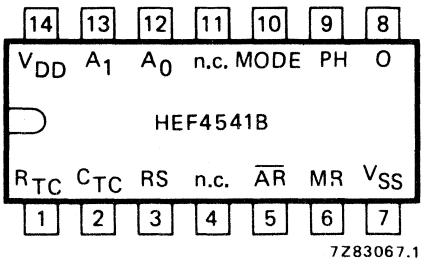


Fig. 2 Pinning diagram.

Fig. 1 Functional diagram.

HEF4541BP : 14-lead DIL; plastic (SOT-27).
HEF4541BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4541BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

FAMILY DATA

see Family Specifications

I_{DD} LIMITS category MSI

Products approved to CECC 90 104-082.

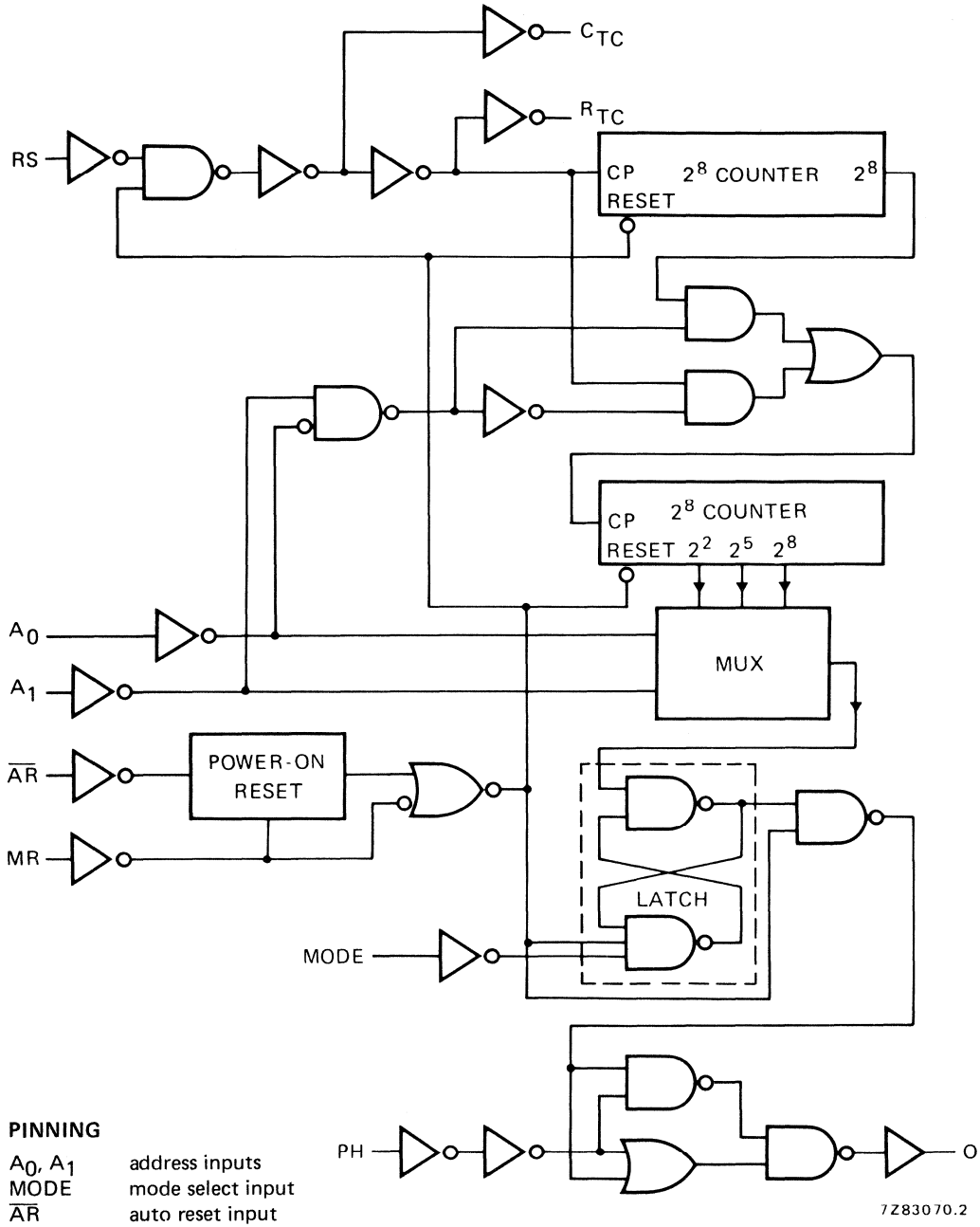


Fig. 3 Logic diagram.

PINNING

A_0, A_1	address inputs
MODE	mode select input
$\overline{AR}$	auto reset input
MR	master reset input
PH	phase input
R_{TC}	external resistor connection (R_t)
C_{TC}	external capacitor connection (C_t)
RS	external resistor connection (R_S) or external clock input

FREQUENCY SELECTION TABLE

A_0	A_1	number of counter stages n	$\frac{f_{osc}}{f_{out}} = 2^n$
L	L	13	8 192
L	H	10	1 024
H	L	8	256
H	H	16	65 536

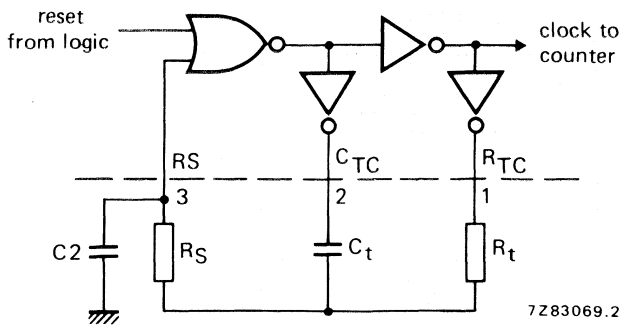
FUNCTION TABLE

inputs				mode
$\overline{AR}$	MR	PH	MODE	
H	L	X	X	auto reset disabled
L	L	X	X	auto reset enabled
X	H	X	X	master reset active
X	L	X	H	normal operation selected division to output
X	L	X	L	single-cycle mode*
X	L	L	X	output initially LOW, after reset
X	L	H	X	output initially HIGH, after reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* The timer is initialized on a reset pulse and the output changes state after 2^{n-1} counts and remains in that state (latched). Reset of this latch is obtained by master reset or by a LOW to HIGH transition on the MODE input.

RC oscillator



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2{,}3 \times R_t \times C_t}$$

Fig. 4 External component connection for RC oscillator; $R_S \approx 2R_t$.

Timing component limitations

The oscillator frequency is mainly determined by R_tC_t, provided $R_t \ll R_S$ and $R_SC2 \ll R_tC_t$. The function of R_S is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500 Ω at V_{DD} = 5 V, 300 Ω at V_{DD} = 10 V and 200 Ω at V_{DD} = 15 V.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t \geqslant 100$ pF, up to any typical value,
10 kΩ $\leqslant R_t \leqslant$ 1 MΩ.

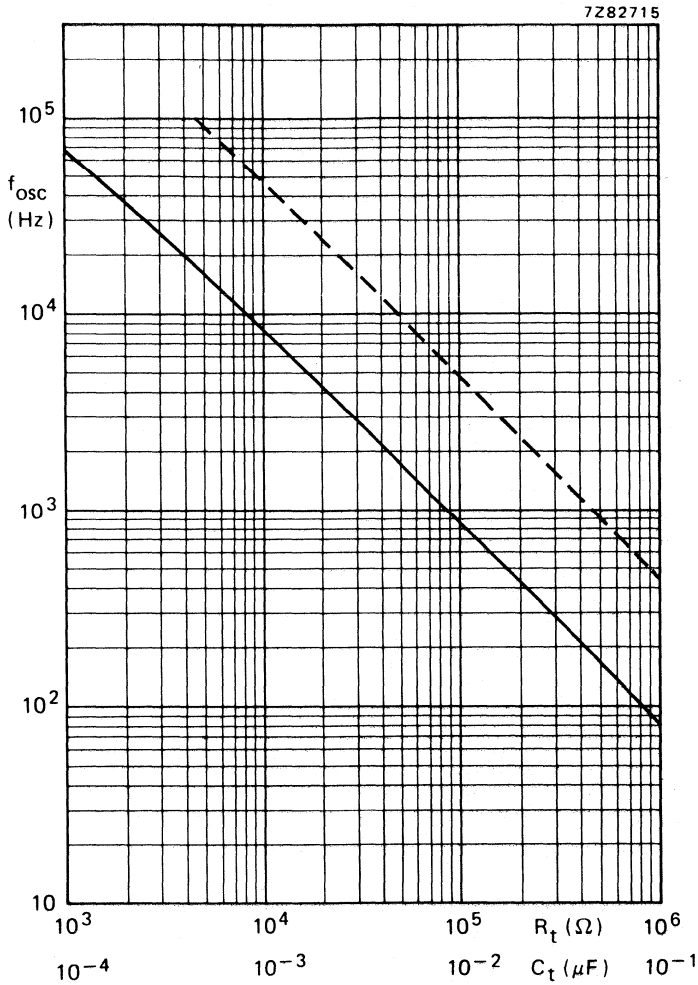


Fig. 5 RC oscillator frequency as a function of R_t and C_t at V_{DD} = 5 to 15 V; T_{amb} = 25 °C.

—— C_t curve at R_t = 56 kΩ; R_S = 120 kΩ.
– – – R_t curve at C_t = 1 nF; $R_S = 2R_t$.

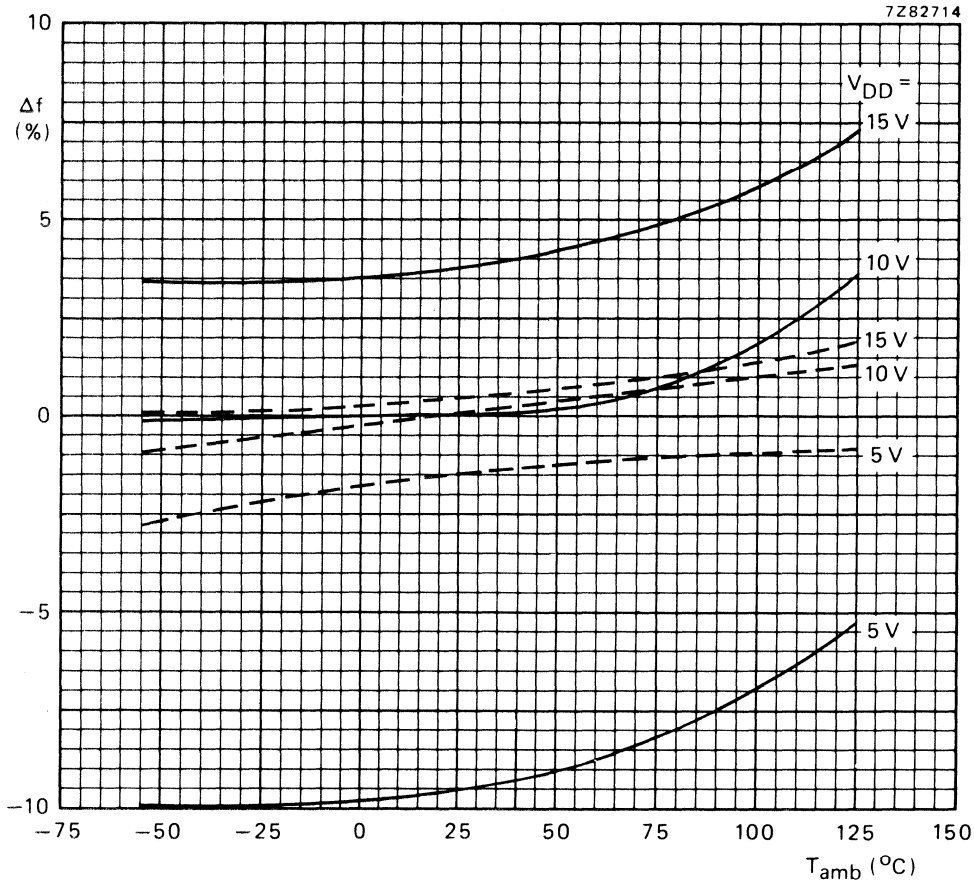


Fig. 6 Frequency deviation (Δf) as a function of ambient temperature; referenced at : f_{osc} at T_{amb} = 25 °C and V_{DD} = 10 V.

——— R_t = 56 kΩ; C_t = 1 nF; R_S = 0.
– – – R_t = 56 kΩ; C_t = 1 nF; R_S = 120 kΩ.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	V_{OH} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 typ.	+25 max.	+85 min.	+85 max.	
Supply current power-on reset enabled (note)	5			I_D	–	80	–	20	80	–	230	μA
	10				–	750	–	250	600	–	700	μA
	15				–	1600	–	500	1300	–	1500	μA
Supply voltage for automatic reset initialization (note)				V_{DD}	–	–	8,5	5	–	–	–	V
Output current HIGH; C_{TC}, R_{TC}	5		4,6	$-I_{OH}$	0,5	–	0,4	–	–	0,3	–	mA
	10		9,5		1,4	–	1,2	–	–	0,95	–	mA
	15		13,5		4,8	–	4,0	–	–	3,2	–	mA
	5		2,5	$-I_{OH}$	1,4	–	1,2	–	–	0,95	–	mA
Output current LOW; C_{TC}, R_{TC}	5	0,4		I_{OL}	0,33	–	0,27	–	–	0,20	–	mA
	10	0,5			1,00	–	0,85	–	–	0,68	–	mA
	15	1,5			3,20	–	2,70	–	–	2,30	–	mA

Note

All inputs at 0 V or V_{DD}, except input $\overline{AR}$ = input MR = 0 V (power-on reset active).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)*
Dynamic power dissipation per package (P)	5	$1\,300\ f_i + f_o C_L V_{DD}^2$
	10	$5\,300\ f_i + f_o C_L V_{DD}^2$
	15	$12\,000\ f_i + f_o C_L V_{DD}^2$
Total power dissipation when using the on-chip oscillator (P)	5	$1\,300\ f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 10\ V_{DD}$
	10	$5\,300\ f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 100\ V_{DD}$
	15	$12\,000\ f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 400\ V_{DD}$

* where:

f_i = input frequency (MHz)
f_o = output frequency (MHz)
C_L = load capacitance (pF)
V_{DD} = supply voltage (V)
C_t = timing capacitance (pF)
f_{osc} = oscillator frequency (MHz)

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
RS ⟶ O						
2^8 selected						
HIGH to LOW	5	t_{PHL};		375	750 ns	348 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		150	300 ns	139 ns + (0,23 ns/pF) C_L
	15			110	220 ns	102 ns + (0,16 ns/pF) C_L
RS ⟶ O						
2^{10} selected						
HIGH to LOW	5	t_{PHL};		425	850 ns	398 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		165	330 ns	154 ns + (0,23 ns/pF) C_L
	15			120	240 ns	112 ns + (0,16 ns/pF) C_L
RS ⟶ O						
2^{13} selected						
HIGH to LOW	5	t_{PHL};		510	1020 ns	483 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		190	380 ns	179 ns + (0,23 ns/pF) C_L
	15			135	270 ns	127 ns + (0,16 ns/pF) C_L
RS ⟶ O						
2^{16} selected						
HIGH to LOW	5	t_{PHL};		575	1150 ns	548 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		210	420 ns	199 ns + (0,23 ns/pF) C_L
	15			150	300 ns	142 ns + (0,16 ns/pF) C_L
Minimum clock	5		60	30	ns	
pulse width; LOW	10	t_{WRSL}	30	15	ns	
	15		24	12	ns	
Minimum reset	5		60	30	ns	
pulse width; HIGH	10	t_{WMRH}	30	15	ns	
	15		24	12	ns	
Maximum clock	5		8	16	MHz	
pulse frequency	10	f_{max}	15	30	MHz	
	15		18	36	MHz	
Oscillator frequency	5			90	kHz	R_t = 5 kΩ
	10	f_{osc}		90	kHz	C_t = 1 nF
	15			90	kHz	R_S = 10 kΩ
Oscillator frequency	5			8	kHz	R_t = 56 kΩ
	10	f_{osc}		8	kHz	C_t = 1 nF
	15			8	kHz	R_S = 120 kΩ

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D_A to D_D), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (O_a to O_g).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

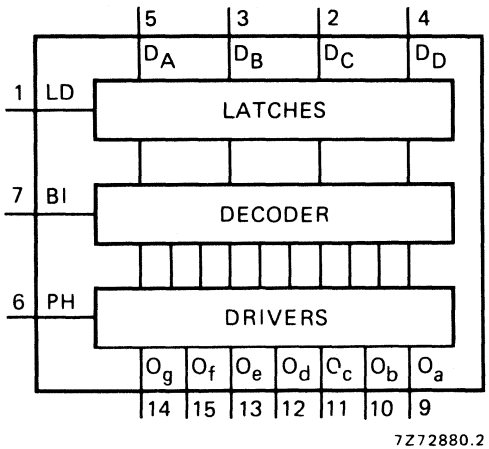


Fig. 1 Functional diagram.

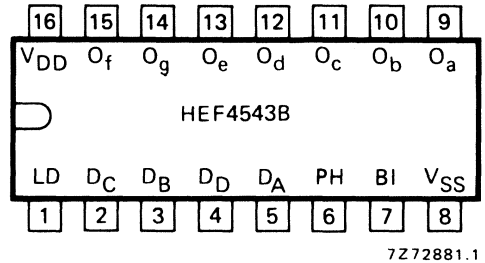


Fig. 2 Pinning diagram.

HEF4543BP : 16-lead-DIL; plastic (SOT-38Z).
HEF4543BD: 16-lead-DIL; ceramic (cerdip) (SOT-74).
HEF4543BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_A to D_D	address (data) inputs
PH	phase input (active HIGH)
BI	blanking input (active HIGH)
LD	latch disable input (active HIGH)
O_a to O_g	segment outputs

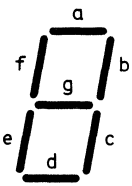


Fig. 3 Segment designation.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

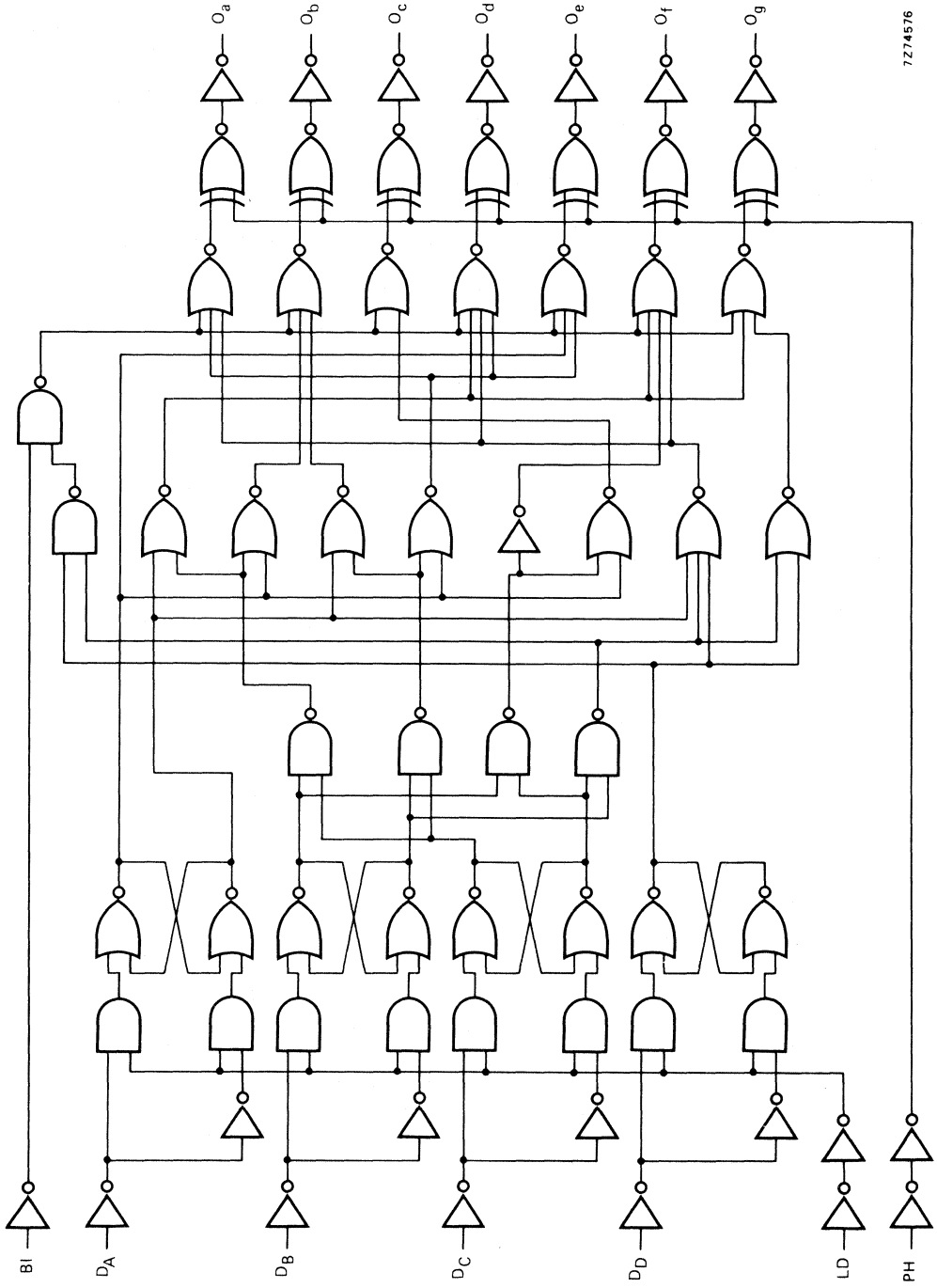


Fig. 4 Logic diagram.

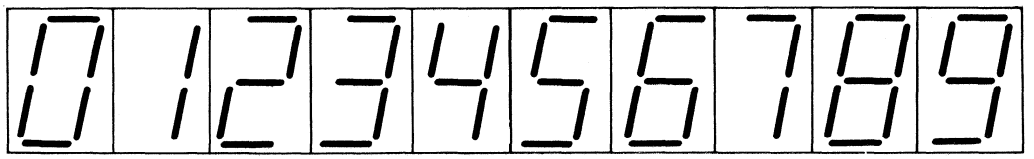
FUNCTION TABLE

inputs							outputs							
LD	BI	PH *	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	biank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				* *				* *
as above		H	as above				inverse of above							as above

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* For liquid crystal displays, apply a square-wave to PH.
For common cathode LED displays, select PH = LOW.
For common anode LED displays, select PH = HIGH.

** Depends upon the BCD-code previously applied when LD = HIGH.



7Z72882

Fig. 5 Display.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$D_n \rightarrow O_n$	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L
$LD \rightarrow O_n$	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			190	380	ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$BI \rightarrow O_n$	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	54 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum LD	5		60	30		ns	
pulse width; HIGH	10	t_{WLDH}	30	15		ns	
	15		20	10		ns	
Set-up time	5		40	20		ns	
$D_n \rightarrow LD$	10	t_{su}	20	5		ns	
	15		15	0		ns	
Hold time	5		0	−15		ns	
$D_n \rightarrow LD$	10	t_{hold}	15	0		ns	
	15		20	5		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2 200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	10 400 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	33 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

APPLICATION INFORMATION

Some examples of applications for the HEF4543B are:

- Driving LCD displays.
- Driving LED displays.
- Driving fluorescent displays
- Driving incandescent displays.
- Driving gas discharge displays.

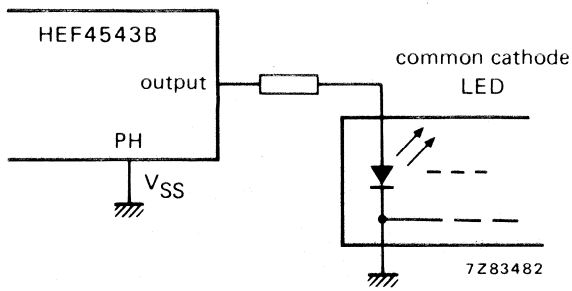


Fig. 6 Connection to common cathode LED display readout.

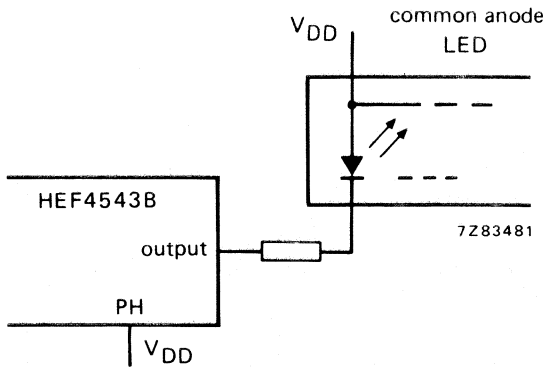


Fig. 7 Connection to common anode LED display readout.

Note to Figs 6 and 7: bipolar transistors may be added for gain where $V_{DD} \leqslant 10$ V or $I_{out} \geqslant 10$ mA.

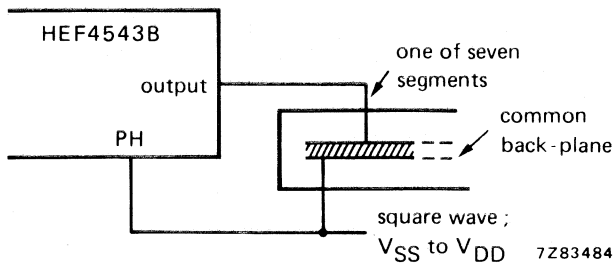


Fig. 8 Connection to liquid crystal (LCD) display readout.

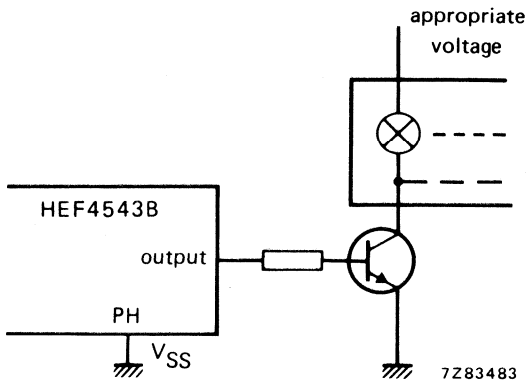


Fig. 9 Connection to incandescent display readout.

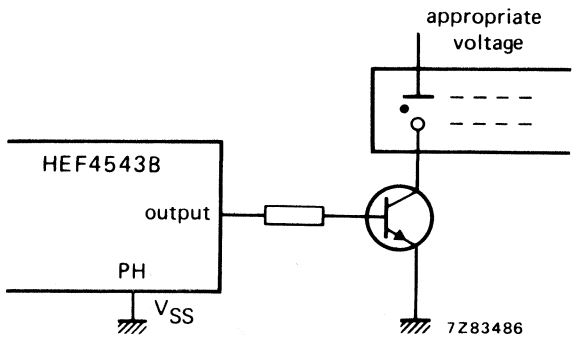


Fig. 10 Connection to gas discharge display readout.

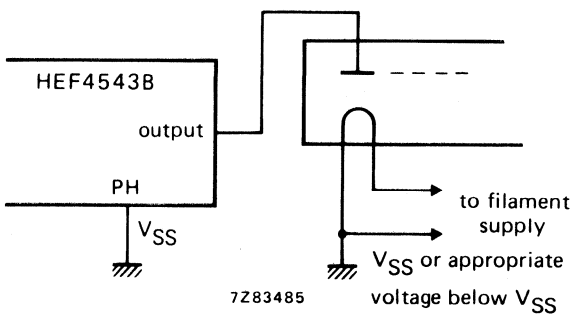


Fig. 11 Connection to fluorescent display readout.

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The HEF4555B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs which are active HIGH (O_0 to O_3). When used as a decoder, $\overline{E}$ when HIGH, forces O_0 to O_3 LOW. When used as a demultiplexer, the appropriate output is selected by the information on A_0 and A_1 with $\overline{E}$ as data input. All unselected outputs are LOW.

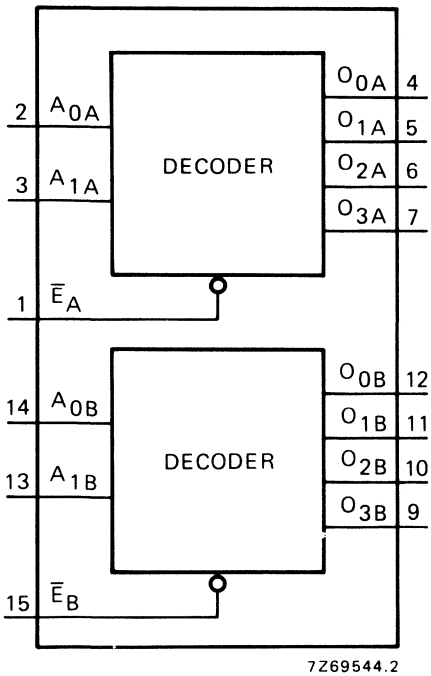


Fig. 1 Functional diagram.

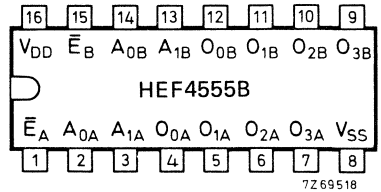


Fig. 2 Pinning diagram.

HEF4555BP : 16-lead DIL; plastic (SOT-38Z).
HEF4555BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4555BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{E}$	enable inputs (active LOW)
A_0 and A_1	address inputs
O_0 to O_3	outputs (active HIGH)

FAMILY DATA
I_{DD} LIMITS category MSI
see Family Specifications

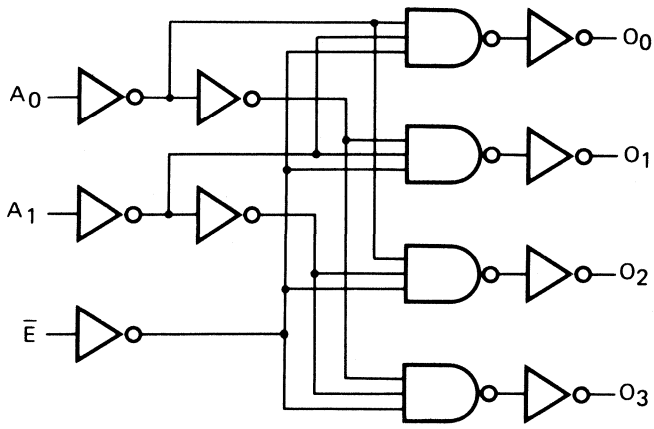


Fig. 3 Logic diagram (one decoder/multiplexer).

TRUTH TABLE

inputs			outputs			
$\overline{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$A_n \rightarrow O_n$	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
$\overline{E}_n \rightarrow O_n$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			150	295	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns +((1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$4500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$18\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$45\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4555B are:

- Code conversion.
- Address decoding.
- Demultiplexing: when using the enable input as data input.

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The HEF4556B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs which are active LOW ($\overline{O}_0$ to $\overline{O}_3$). When used as a decoder, $\overline{E}$ when HIGH, forces $\overline{O}_0$ to $\overline{O}_3$ HIGH. When used as a demultiplexer, the appropriate output is selected by the information on A_0 and A_1 with $\overline{E}$ as data input. All unselected outputs are HIGH.

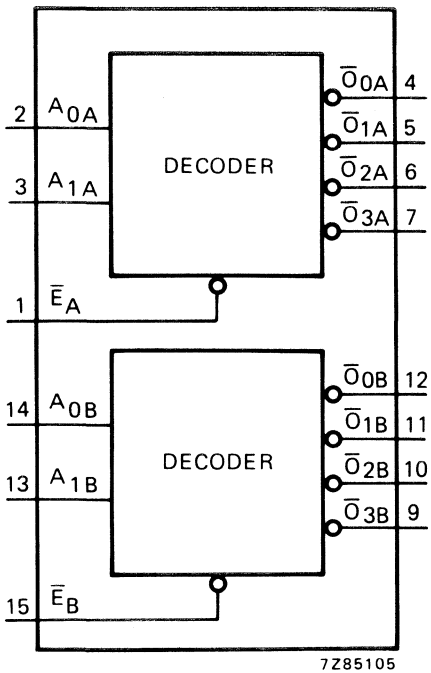


Fig. 1 Functional diagram.

Fig. 2 Pinning diagram.

HEF4556BP : 16-lead DIL; plastic (SOT-38Z).
HEF4556BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4556BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{E}$	enable inputs (active LOW)
A_0 and A_1	address inputs
$\overline{O}_0$ to $\overline{O}_3$	outputs (active LOW)

FAMILY DATA
I_{DD} LIMITS category MSI
} see Family Specifications

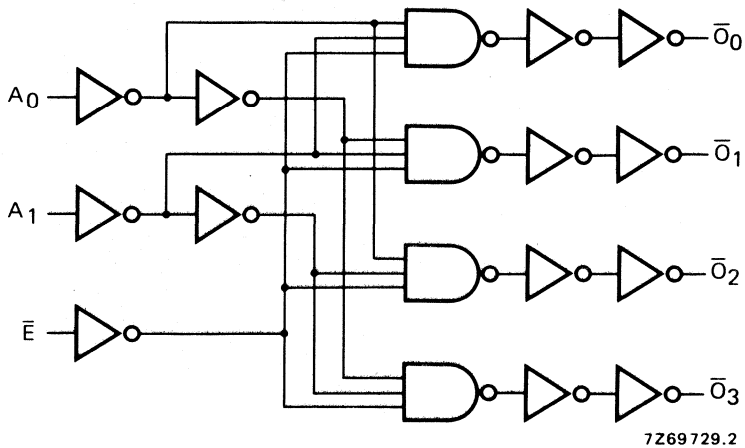


Fig. 3 Logic diagram (one decoder/multiplexer).

TRUTH TABLE

inputs			outputs			
$\bar{E}$	A_0	A_1	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$A_n \rightarrow \overline{O}_n$	5			130	255	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{E}_n \rightarrow \overline{O}_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			105	205	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	4400 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	18 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	43 300 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

APPLICATION INFORMATION

Some examples of applications for the HEF4556B are:

- Code conversion.
- Address decoding.
- Demultiplexing: when using the enable input as data input.

1-to-64 BIT VARIABLE LENGTH SHIFT REGISTER

The HEF4557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled length control inputs (L_1, L_2, L_4, L_8, L_{16} and L_{32}) plus one. Serial data may be selected from the D_A or D_B data inputs with the $A/\overline{B}$ select input. This feature is useful for recirculation purposes. Information on D_A or D_B is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP_0 while $\overline{CP}_1$ is LOW or on the HIGH to LOW transition of $\overline{CP}_1$ while CP_0 is HIGH. A HIGH on master reset (MR) resets the register and forces O to LOW and $\overline{O}$ to HIGH, independent of the other inputs.

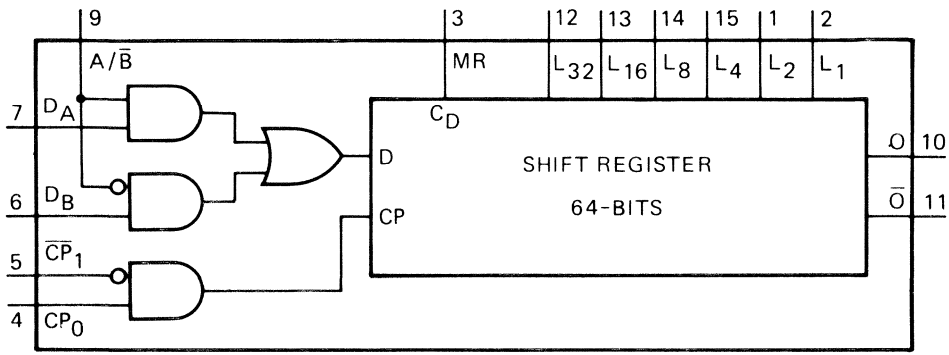


Fig. 1 Functional diagram.

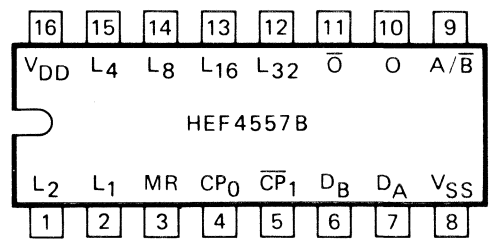


Fig. 2 Pinning diagram.

PINNING

D_A, D_B	data inputs
$A/\overline{B}$	select data input
CP_0	clock input
$\overline{CP}_1$	clock enable input
MR	asynchronous master reset
L_1 to L_{32}	bit-length control inputs
O, $\overline{O}$	buffered outputs

HEF4557BP : 16-lead DIL; plastic (SOT-38Z).
HEF4557BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4557BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

Products approved to CECC 90 104-086.

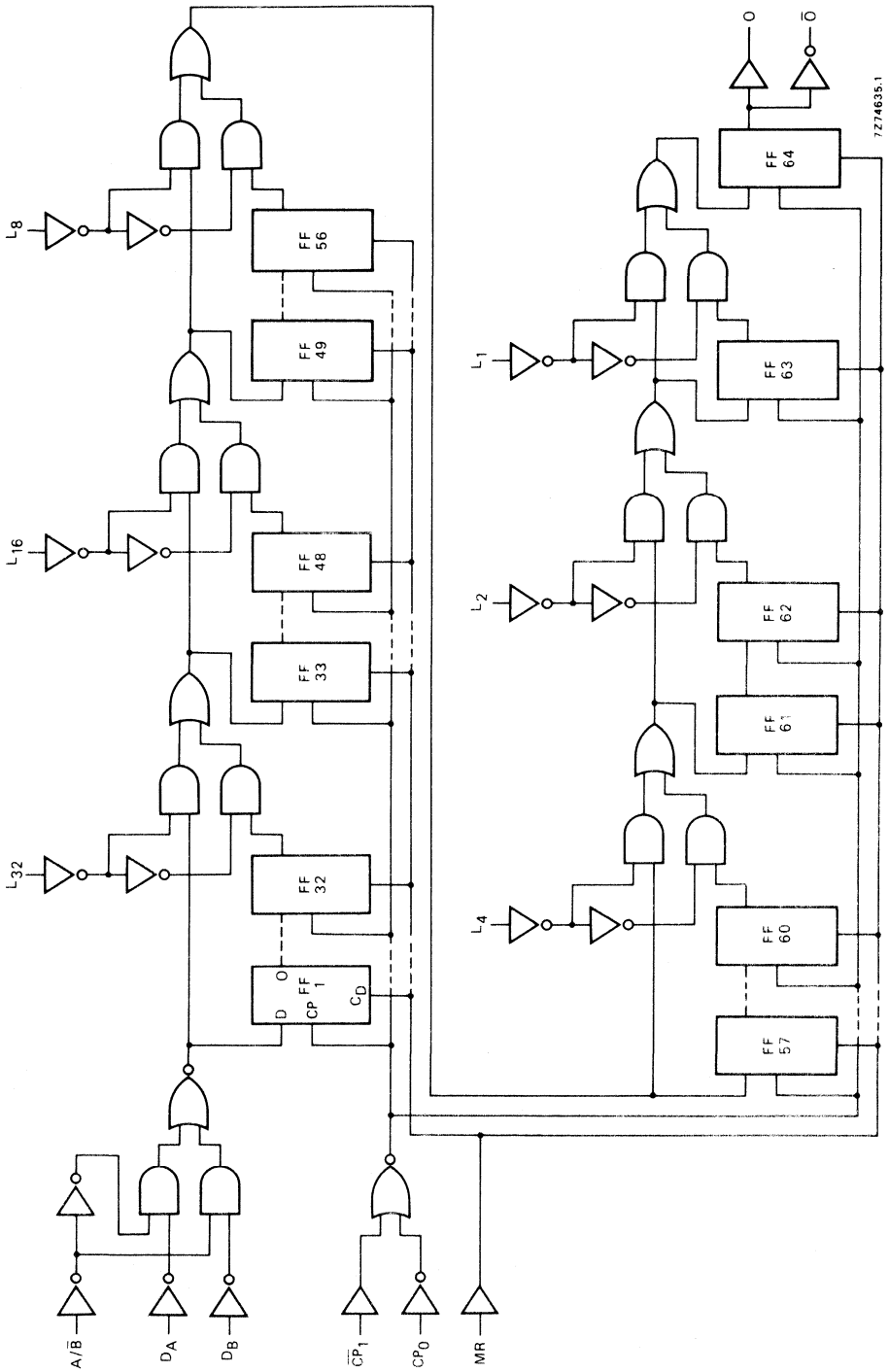


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs						output
MR	A/$\overline{B}$	D_A	D_B	CP_0	$\overline{CP}_1$	O *
L	L	D_1	D_2	∫	L	D_2
L	H	D_1	D_2	∫	L	D_1
L	L	D_1	D_2	H	⟍	D_2
L	H	D_1	D_2	H	⟍	D_1
H	X	X	X	X	X	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⟍ = negative-going transition
D_n = either HIGH or LOW

* The moment D_n appears at O depends on the bit-length shown in the table below.

BIT-LENGTH SELECT FUNCTION TABLE

L_{32}	L_{16}	L_8	L_4	L_2	L_1	register length
L	L	L	L	L	L	1-bit
L	L	L	L	L	H	2-bits
L	L	L	L	H	L	3-bits
L	L	L	L	H	H	4-bits
L	L	L	H	L	L	5-bits
L	L	L	H	L	H	6-bits
L	L	L	H	H	L	7-bits
L	L	L	H	H	H	8-bits
↓	↓	↓	↓	↓	↓	↓
L	H	H	H	H	H	32-bits
H	L	L	L	L	L	33-bits
H	L	L	L	L	H	34-bits
↓	↓	↓	↓	↓	↓	↓
H	H	H	H	L	L	61-bits
H	H	H	H	L	H	62-bits
H	H	H	H	H	L	63-bits
H	H	H	H	H	H	64-bits

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3\,500\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$15\,000\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$37\,000\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
CP_0, $\overline{CP}_1$ → O, $\overline{O}$	5		240	480	ns	213 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	90	180	ns	79 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		240	480	ns	213 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	90	180	ns	79 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
MR → O	5		170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	80	160	ns	69 ns + (0,23 ns/pF) C_L
	15		60	120	ns	52 ns + (0,16 ns/pF) C_L
MR → $\overline{O}$	5		140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		55	110	ns	47 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

Interpolation table (see note next page)

length control inputs						minimum number of bits selected	set-up, hold, recovery times
L_1	L_2	L_4	L_8	L_{16}	L_{32}		
L	L	L	L	L	L	1	specified
H	L	L	L	L	L	2	⋮
X	H	L	L	L	L	3	⋮
X	X	H	L	L	L	5	six equal steps
X	X	X	H	L	L	9	⋮
X	X	X	X	H	L	17	⋮
X	X	X	X	X	H	33	specified

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leqslant$ 20 ns; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.		
Minimum clock pulse width; LOW for CP_0 or HIGH for $\overline{CP}_1$	5	t_{WCPL} or t_{WCPH}	180	90	ns	
	10		60	30	ns	
	15		40	20	ns	
Minimum reset pulse width; HIGH	5	t_{WMRH}	150	75	ns	
	10		70	35	ns	
	15		50	25	ns	
Set-up times D_A, D_B, $A/\overline{B}$ → CP_0, $\overline{CP}_1$ L_1 to L_{32} = LOW	5	t_{su}	360	180	ns	see note
	10		140	70	ns	
	15		90	45	ns	
L_{32} = HIGH	5	t_{su}	40	-20	ns	
	10		35	-10	ns	
	15		30	-5	ns	
Hold times D_A, D_B, $A/\overline{B}$ → CP_0, $\overline{CP}_1$ L1 to L32 = LOW	5	t_{hold}	-40	-110	ns	
	10		-10	-45	ns	
	15		0	-30	ns	
L_{32} = HIGH	5	t_{hold}	90	30	ns	
	10		60	20	ns	
	15		50	15	ns	
Recovery times for MR L_1 to L_{32} = LOW	5	t_{RMR}	500	250	ns	
	10		250	125	ns	
	15		150	75	ns	
L_{32} = HIGH	5	t_{RMR}	110	50	ns	
	10		70	30	ns	
	15		60	25	ns	
Minimum clock pulse frequency	5	f_{max}	2,5	5	MHz	
	10		7	14	MHz	
	15		10	20	MHz	

Note

The set-up, hold and recovery times vary with the minimum number of bits selected. For other values as specified one may interpolate as shown in the table (see previous page).

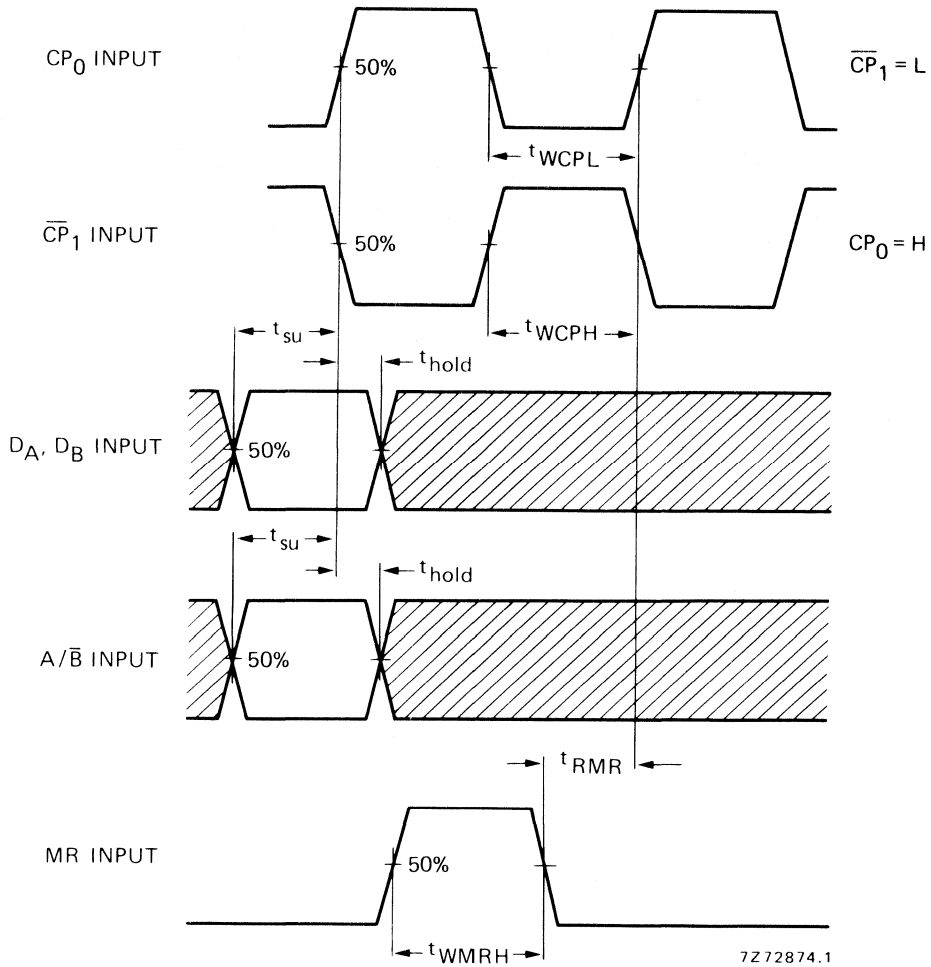


Fig. 4 Waveforms showing recovery time for MR and minimum CP_0, $\overline{CP}_1$ and MR pulse widths, set-up and hold times for D_A, D_B and $A/\overline{B}$ to CP_0 and $\overline{CP}_1$. Set-up and hold times are shown as positive values but may be specified as negative values.

4-BIT MAGNITUDE COMPARATOR

The HEF4585B is a 4-bit magnitude comparator which compares two 4-bit words (A and B), whether they are 'less than', 'equal to', or 'greater than'. Each word has four parallel inputs (A_0 to A_3 and B_0 to B_3); A_3 and B_3 being the most significant inputs. Three outputs are provided; A greater than B ($O_{A>B}$), A less than B ($O_{A<B}$) and A equal to B ($O_{A=B}$). Three expander inputs ($I_{A>B}$, $I_{A<B}$ and $I_{A=B}$) allow cascading of the devices without external gates.

For proper compare operation the expander inputs to the least significant position must be connected as follows: $I_{A=B} = I_{A>B}$ = HIGH, $I_{A<B}$ = LOW. For words greater than 4-bits, units can be cascaded by connecting outputs $O_{A<B}$ and $O_{A=B}$ to the corresponding inputs of the next significant comparator (input $I_{A>B}$ is connected to a HIGH).

Operation is not restricted to binary codes, the devices will work with any monotonic code. The function table describes the operation of the device under all possible logic conditions.

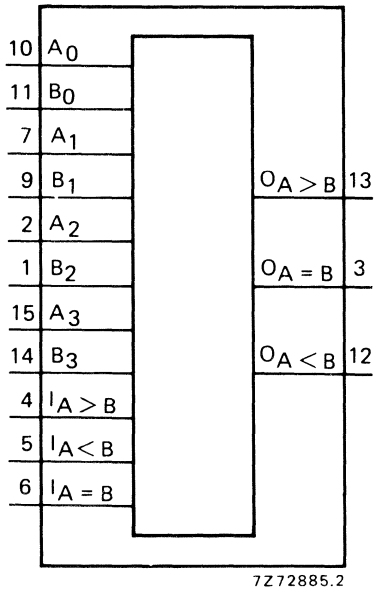


Fig. 1 Functional diagram.

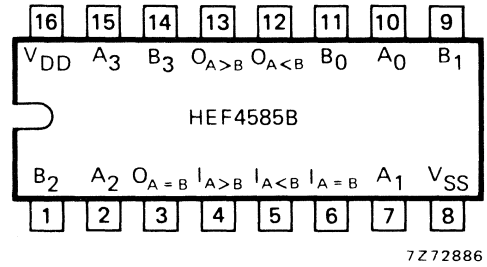


Fig. 2 Pinning diagram.

HEF4585BP : 16-lead DIL; plastic (SOT-38Z).
HEF4585BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4585BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

A_0 to A_3	word A parallel inputs
B_0 to B_3	word B parallel inputs
$I_{A>B}$, $I_{A<B}$, $I_{A=B}$	expander inputs
$O_{A>B}$	A greater than B output
$O_{A<B}$	A less than B output
$O_{A=B}$	A equal to B output

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Products approved to CECC 90 104-087.

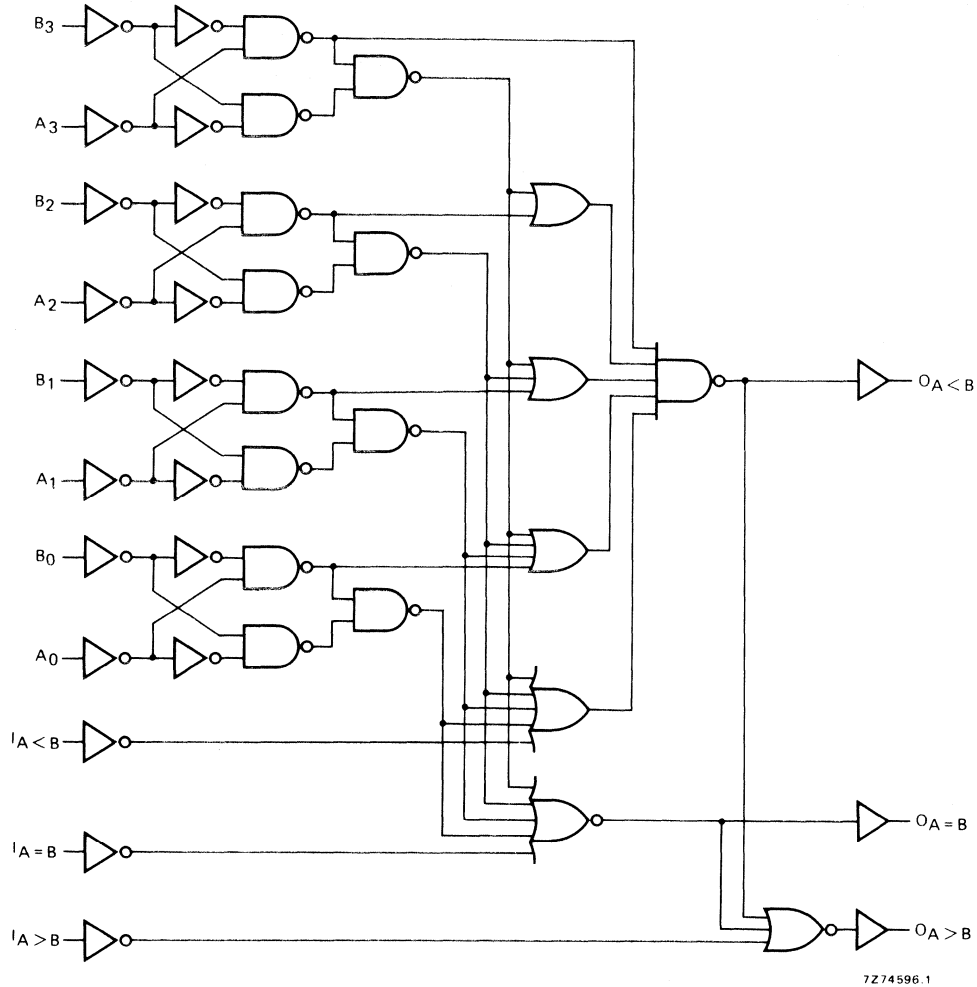


Fig. 3 Logic diagram.

FUNCTION TABLE

comparing inputs				cascading inputs			outputs		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3 > B_3$	X	X	X	H	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	H	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	H	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	H	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	H	H	L	H	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a serial expansion scheme.

The lower 2 lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
A_n, B_n → O_n	5			160	320 ns	133 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
	5			150	300 ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
I_n → O_n	5			110	220 ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90 ns	34 ns + (0,23 ns/pF) C_L
	15			30	60 ns	22 ns + (0,16 ns/pF) C_L
	5			120	240 ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
Output transition times						
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1250\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4585B are:

- Process controllers.
- Servo-motor control.

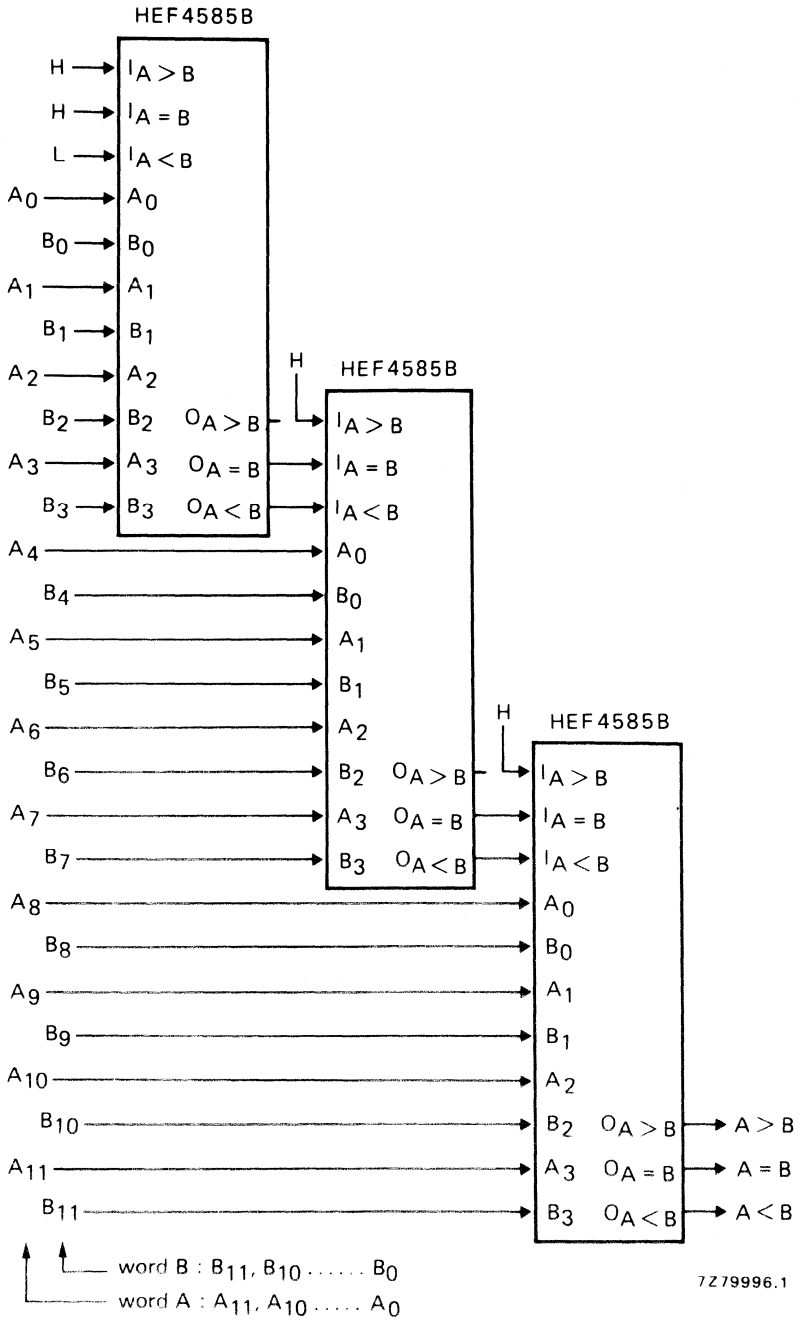


Fig. 4 Example of cascading comparators.

256-BIT, 1-BIT PER WORD RANDOM ACCESS MEMORIES

The HEF4720B and HEF4720V are 256-bit, 1-bit per word random access memories with 3-state outputs. The memories are fully decoded and completely static.

Recommended supply voltage range for HEF4720B is 3 to 15 V and for HEF4720V is 4,5 to 12,5 V; minimum stand-by voltage for both types is 3 V.

The use of LOCMOS gives the added advantage of very low stand-by power. The circuits can be directly interfaced with standard bipolar devices (TTL) without using special interface circuits. The memory operates from a single power supply. The separate chip select input ($\overline{CS}$) allows simple memory expansion when the outputs are wire-ORed. If $\overline{CS}$ is HIGH, the outputs are floating and no new information can be written into the memory. The signal at O has the same polarity as the data input D, while the signal at $\overline{O}$ is the complement of the signal at O. The write control W must be HIGH for writing into the memory.

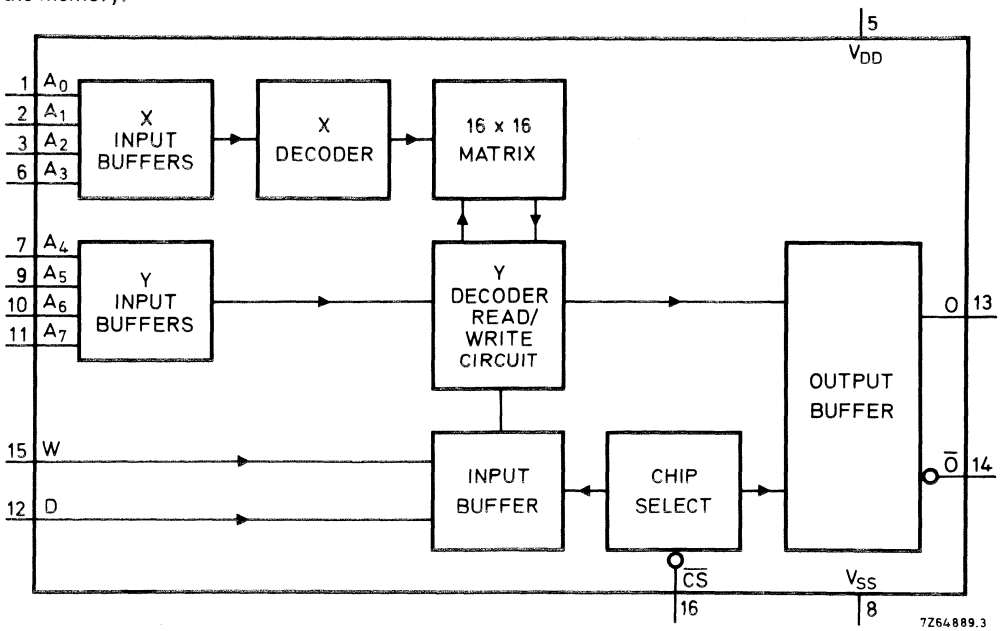


Fig. 1 Functional diagram.

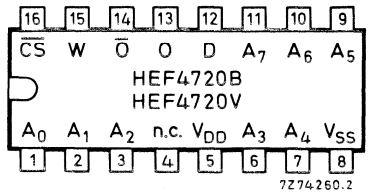


Fig. 2 Pinning diagram.

HEF4720BP; HEF4720VP: 16-lead DIL; plastic (SOT-38Z).
HEF4720BD; HEF4720VD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4720BT; HEF4720VT: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

FAMILY DATA: see Family Specifications.

I_{DD} LIMITS: see next page.

Products approved to CECC 90 104-088.

FUNCTION TABLE

$\overline{CS}$	W	O	$\overline{O}$	mode
L	H	data written into memory	complement of data written into memory	write
L	L	data written into memory	complement of data written into memory	read
H	X	Z	Z	inhibit

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance OFF-state

PINNING

$\overline{CS}$	chip select input (active LOW)
W	write enable input
D	data input
A_0 to A_7	address inputs
O	3-state output (active HIGH)
$\overline{O}$	3-state output (active LOW)

SUPPLY VOLTAGE

	rating	recommended operating	stand-by min.
HEF4720B	−0,5 to 18	3,0 to 15,0	3 V
HEF4720V	−0,5 to 18	4,5 to 12,5	3 V

The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4720V, because of its lower supply voltage range.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output current LOW	4,75	0,4	I_{OL}	2,4		2		1,6		mA
	10	0,5		4,8		4		3,2		mA
	15	1,5		10,0		10		7,5		mA
Quiescent device current	5		I_{DD}		25		25		200	μA
	10				50		50		400	μA
	15				100		100		800	μA
Input leakage current HEF4720V	10		$\pm I_{IN}$		0,3		0,3		1	μA
HEF4720B	15				0,3		0,3		1	μA

A.C. CHARACTERISTICS

	V_{DD} V	symbol	min.	typ.	max.		
Output capacitance	5	C_O		5		pF	
	10			5		pF	
	15			5		pF	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Read cycle							
Read access time	5	t_{ACC}		320	580	ns	292 ns + (0,55 ns/pF) C_L
	10			130	220	ns	118 ns + (0,23 ns/pF) C_L
	15			100	160	ns	92 ns + (0,16 ns/pF) C_L
Chip select to output time	5	t_{CO}			180	ns	
	10				70	ns	
	15				50	ns	
Address hold time	5	t_{OA}	0			ns	
	10		0			ns	
	15		0			ns	
Output hold time with respect to address input	5	t_{VAL1}	60	170		ns	142 ns + (0,55 ns/pF) C_L
	10		20	50		ns	38 ns + (0,23 ns/pF) C_L
	15		15	40		ns	32 ns + (0,16 ns/pF) C_L
Output hold time with respect to chip select input	5	t_{COH}			130	ns	
	10				70	ns	
	15				60	ns	
Output floating time with respect to chip select input	5	t_{COF}	0			ns	
	10		0			ns	
	15		0			ns	
Read cycle time	5	t_{RC}	580			ns	
	10		220			ns	
	15		160			ns	
Output transition times LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
HIGH to LOW	5	t_{THL}		40	80	ns	14 ns + (0,52 ns/pF) C_L
	10			22	40	ns	11 ns + (0,22 ns/pF) C_L
	15			15	30	ns	7 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	
Write cycle						
Write cycle time	5	t_{WC}	580			ns
	10		220			ns
	15		160			ns
Address to write set-up time	5	t_{AW}	110			ns
	10		50			ns
	15		50			ns
Write pulse width	5	t_{WP}	370		10 000	ns
	10		130		10 000	ns
	15		80		10 000	ns
Write recovery time	5	t_{WR}	100			ns
	10		40			ns
	15		30			ns
Data set-up time	5	t_{DW}	250			ns
	10		100			ns
	15		80			ns
Data hold time	5	t_{DH}	100			ns
	10		30			ns
	15		20			ns
Chip select set-up time with respect to write pulse	5	t_{CSW}	370			ns
	10		130			ns
	15		80			ns
Chip select hold time with respect to write pulse	5	t_{CSH}	0			ns
	10		0			ns
	15		0			ns
Chip select lead time over write pulse to prevent writing	5	t_{CSL}	0			ns
	10		0			ns
	15		0			ns
Read-modify-write cycle						
Read enable hold time	5	t_{RH}	0			ns
	10		0			ns
	15		0			ns
Output hold time with respect to write pulse	5	t_{VAL2}	60			ns
	10		20			ns
	15		15			ns
Read-modify-write cycle time	5	t_{RWC}	1050			ns
	10		390			ns
	15		270			ns

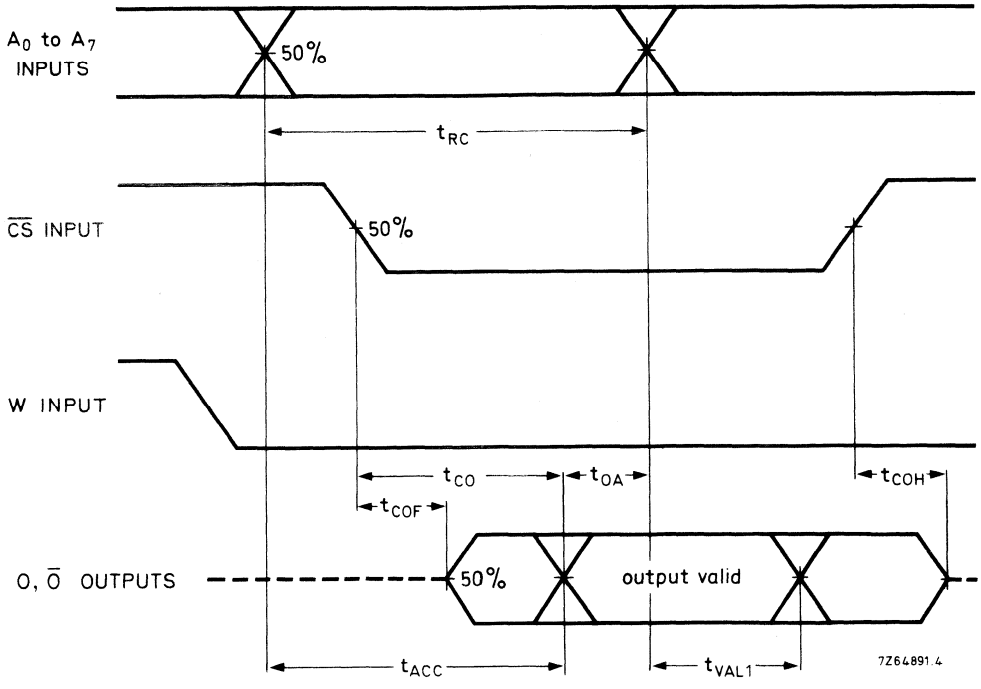


Fig. 3 Read cycle timing diagram.

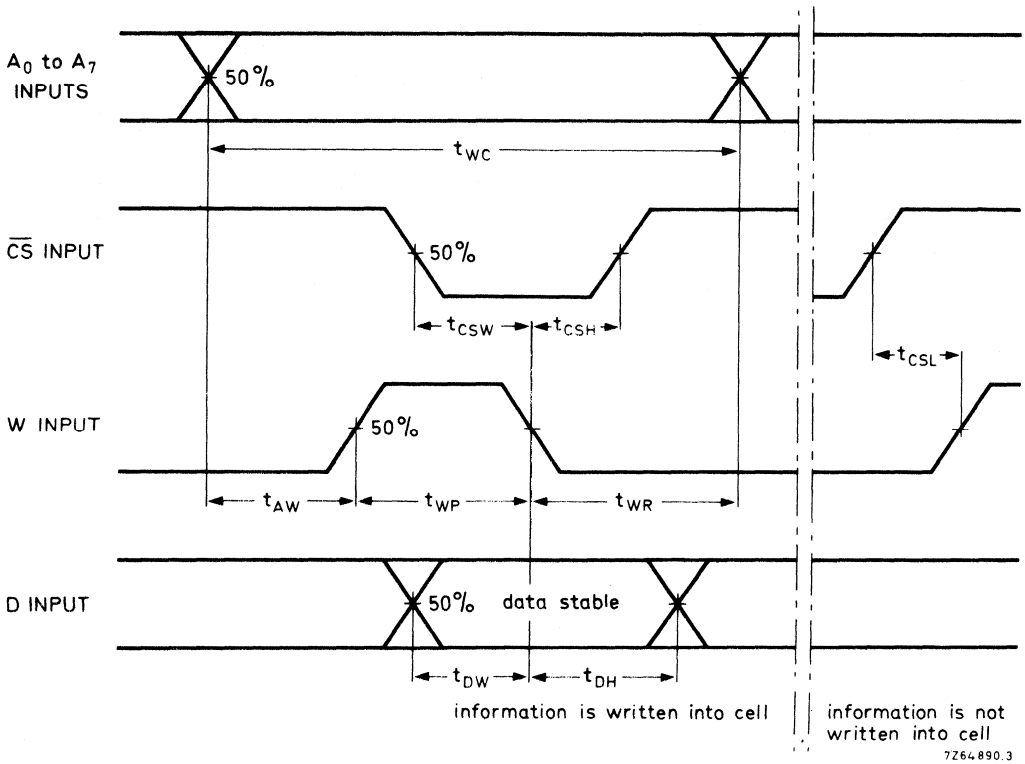


Fig. 4 Write cycle timing diagram.

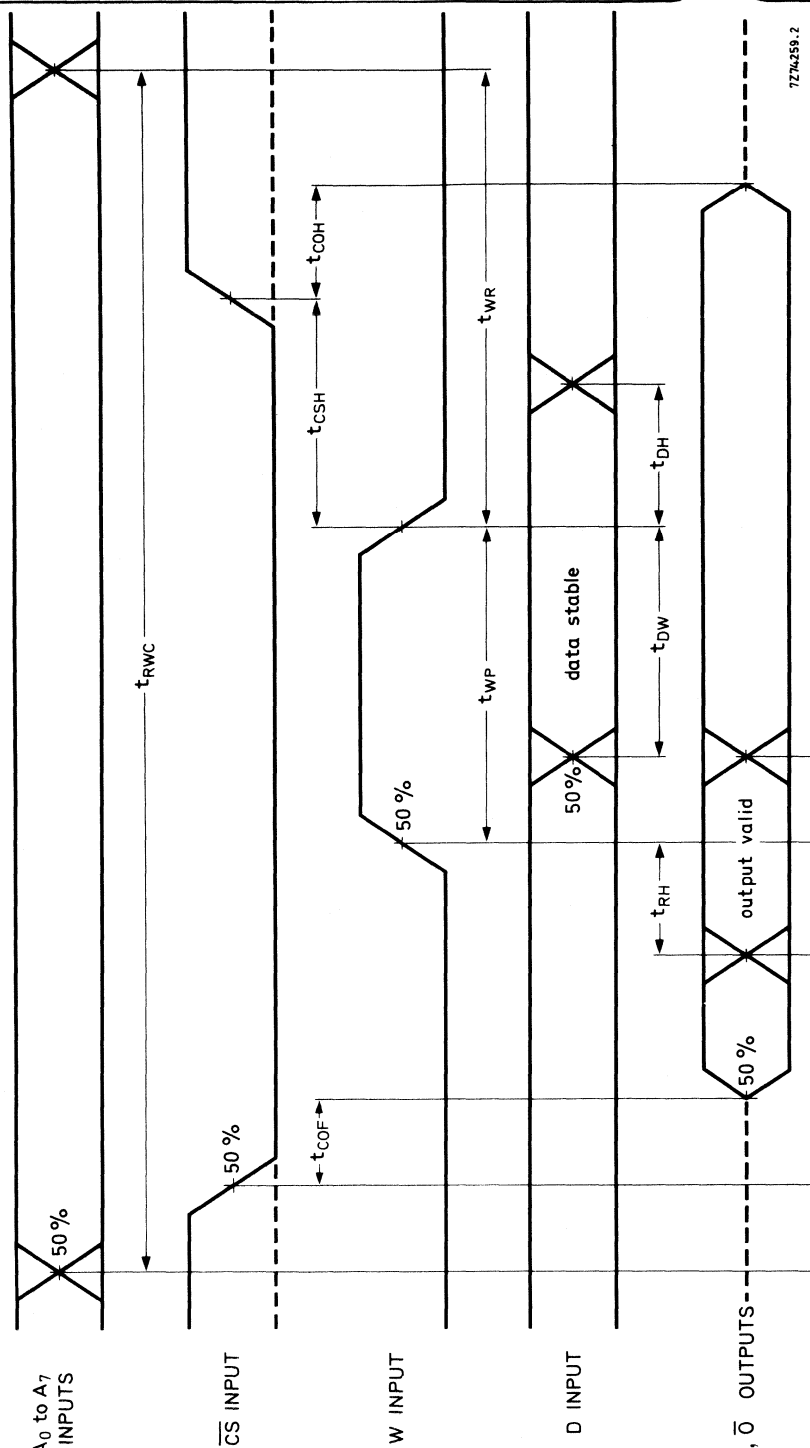


Fig. 5 Read-modify-write cycle timing diagram.

APPLICATION INFORMATION

Extension of memory capacity

The memory capacity of the HEF4720B; V is 256 bits (or 256 words of 1 bit). The capacity of a system can be extended in various ways by the connection of further HEF4720B; V ICs.

Extending the word length

By connecting a number of HEF4720B; V ICs as shown in Fig. 6, the word length (i.e. bits per word) is multiplied by that number. That is, each device stores 1 bit per word but the total number of words remains 256. For example, if four devices are used in this way, 256 four-binary-bit words can be stored.

Extending the number of words

If a number of HEF4720B; V ICs are connected as shown in Fig. 7, the words available are multiplied by that number, but the word length remains 1 bit. Notice that in this case additional addresses are used in conjunction with the $\overline{CS}$ input. In the case shown in Fig. 7 (4 x HEF4720B; V in parallel), the addresses and data inputs are loaded with four inputs (= 20 pF), the $\overline{CS}$ inputs are loaded with one input each.

Extending both the word length and number of words

Figure 8 shows how a combination of the extensions described above can be used to obtain both greater word length and additional words. It is clear that the capacitive load of the driving circuits puts a limit to the free choice of the interface. In Fig. 8, each address is loaded with 16 inputs, i.e. 16 x 5 = 80 pF: each CS inverter is loaded with 8 inputs, i.e. 8 x 5 = 40 pF. The data inverters in this case are loaded with only two inputs each.

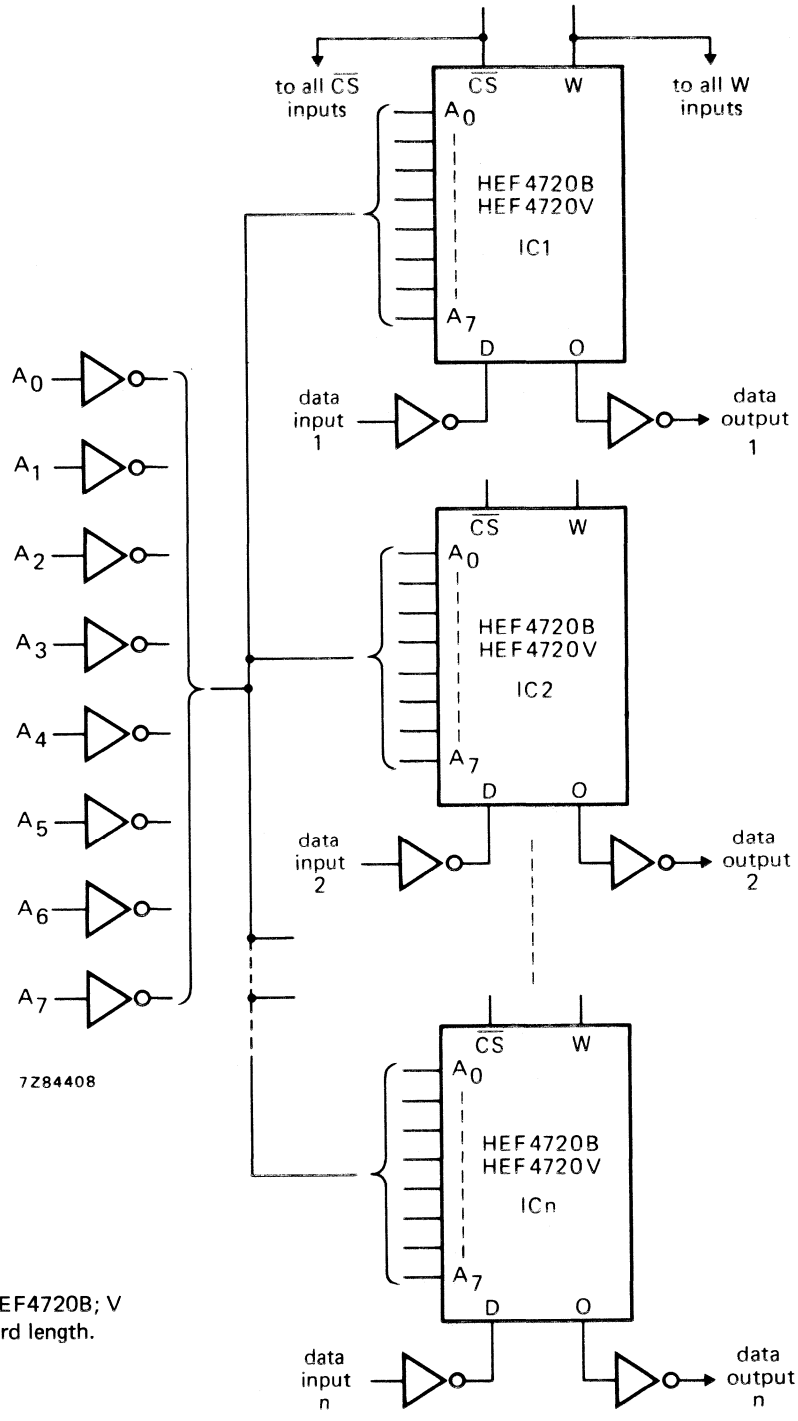


Fig. 6 Using extra HEF4720B; V ICs to extend the word length.

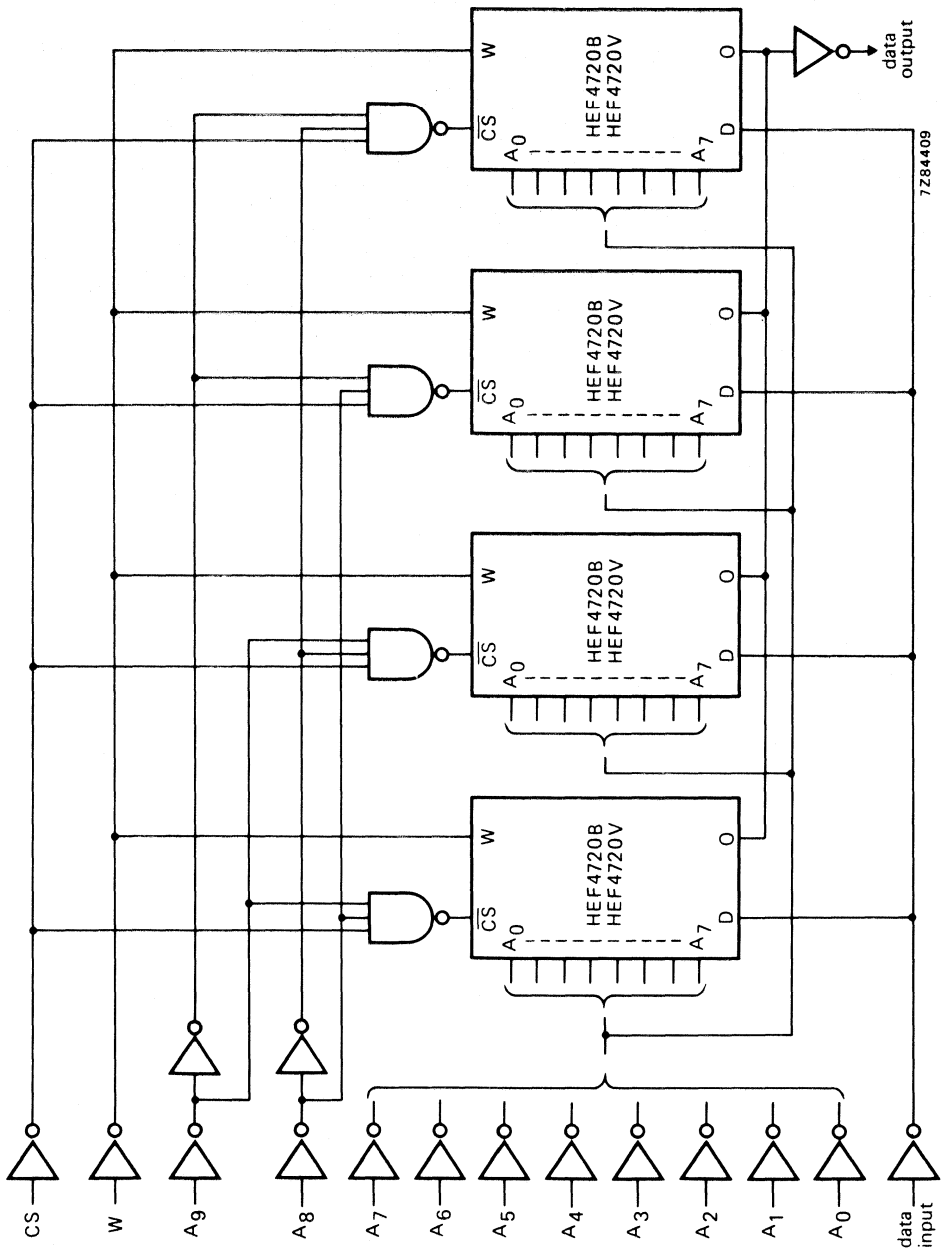


Fig. 7 Using extra HEF4720B; V ICs to obtain more words.

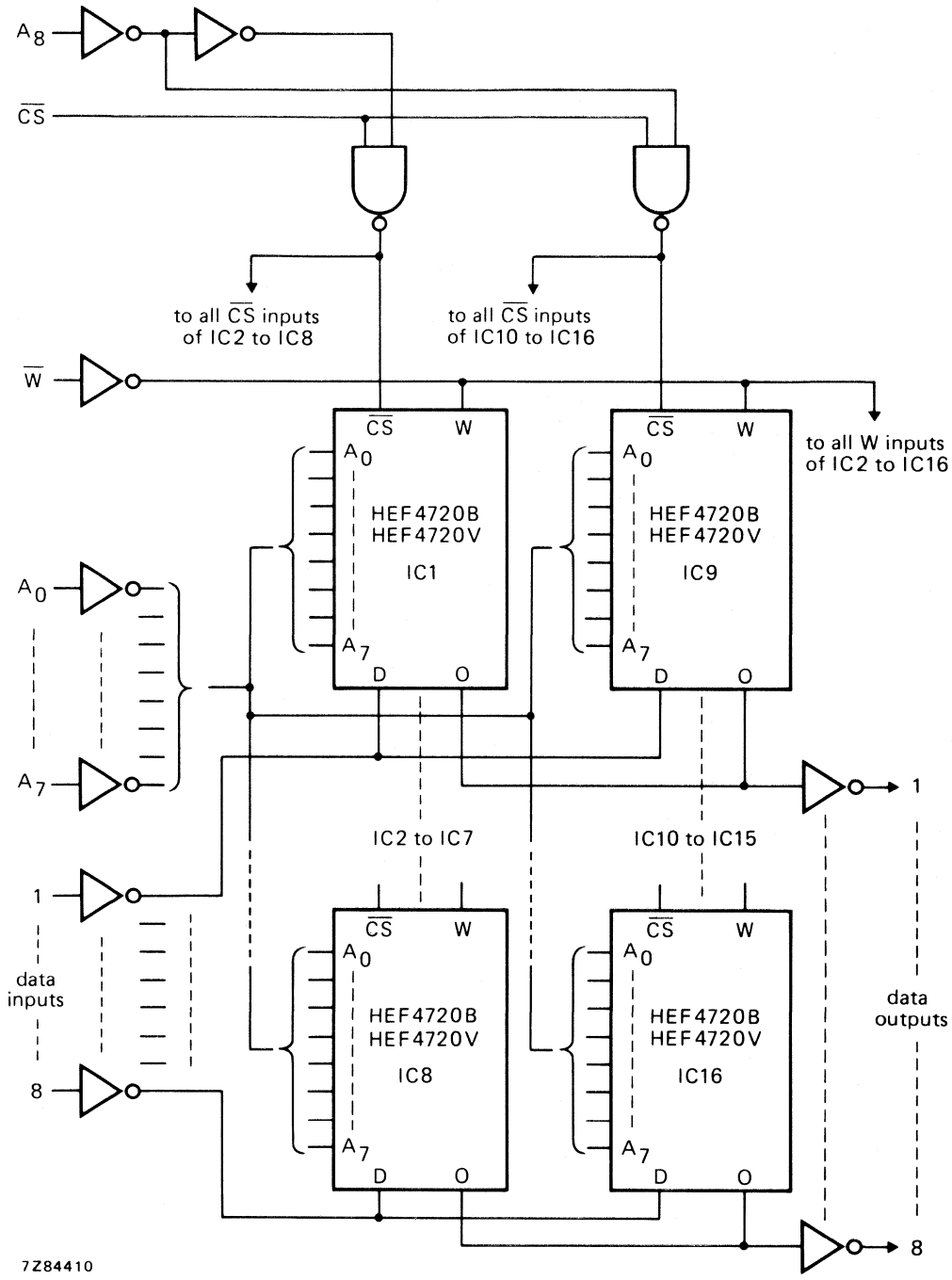


Fig. 8 Using extra HEF4720B; V ICs to obtain more words and greater word length.

APPLICATION INFORMATION (continued)

Memory retention

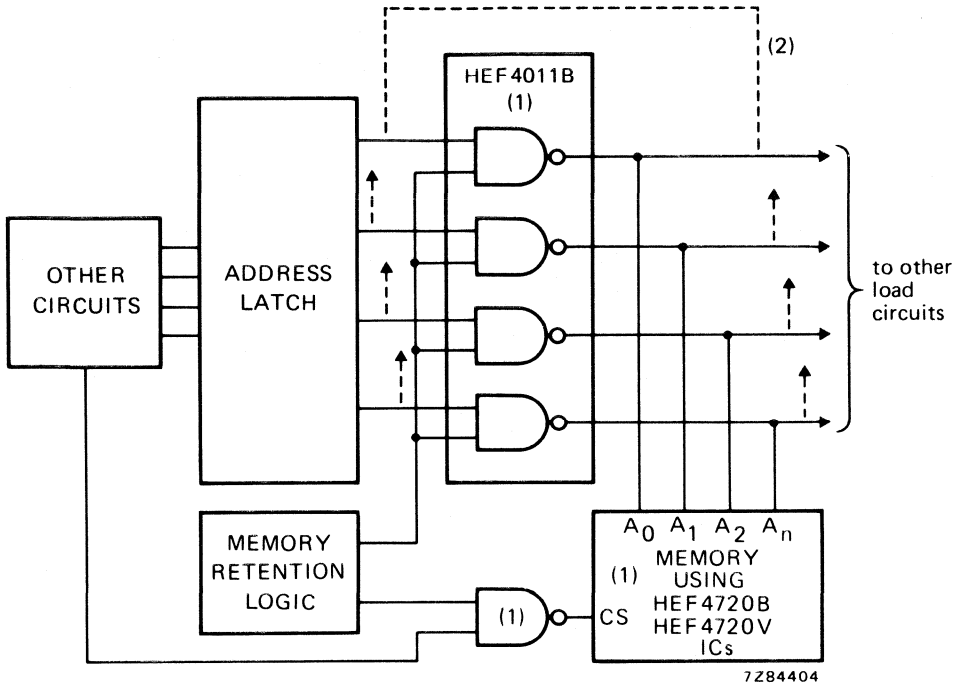
It is sometimes necessary to ensure that the information stored in the memory cannot be erased inadvertently. This can be arranged by adding detection circuits, by measures in the timing, and by the addition of a battery. With the HEF4720B; V, memory retention is very easily obtained because its current drain in the stand-by condition is almost zero. The wide supply voltage range makes it possible to keep the memory active by means of a simple battery, thereby preventing information loss.

In designing the memory retention circuits, two aspects should be kept in mind. The memory retention will not function in an optimum way if the battery voltage is low or if the voltage transitions at the address input are too slow. The first of these is usually the result of using too simple a battery back-up circuit, e.g. a battery charged via a diode from the TTL supply voltage. In this case, the LOCMOS supply voltage falls below the safe operating voltage. Special arrangements should be made to overcome this.

Slow address transitions (the second cause of memory loss) are due to a long RC-time in the power system. When the power is switched on or off, the 5 V line changes between 0 and 5 V in milliseconds to seconds so producing a correspondingly long transition time in the various logic outputs. This creates problems in the proper operation of the HEF4720B; V, with loss of memory as a possible result. This can be prevented by ensuring that input rise and fall times do not exceed 10 μs.

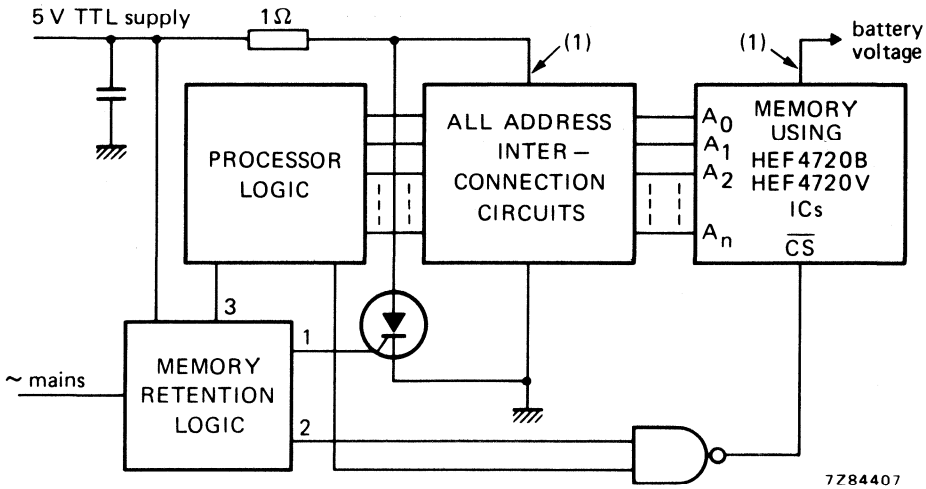
Three possibilities for controlling the rise and fall times at the HEF4720B; V interface are given here:

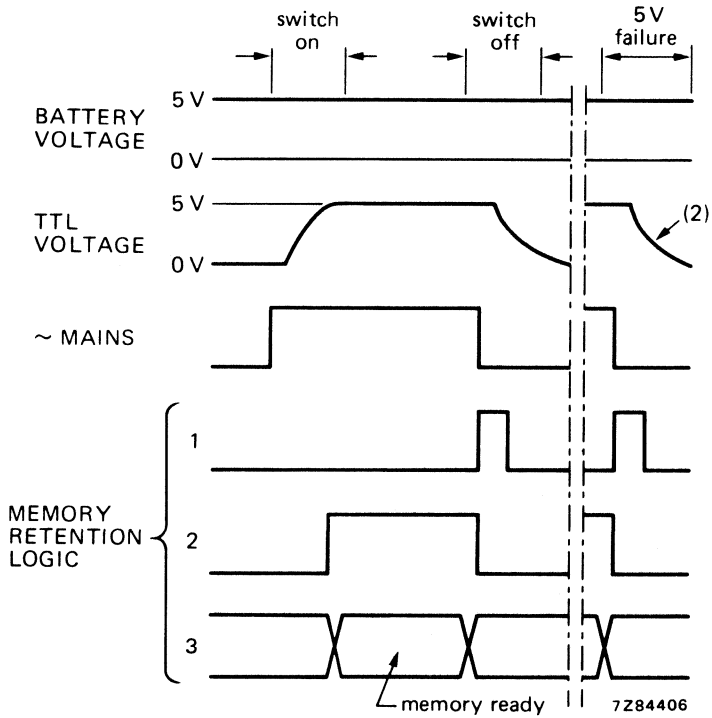
1. LOCMOS gates can be connected between the address latch and the HEF4720B; V (Fig. 9). In the event of a low voltage, or mains supply failure, the gates can be blocked by a signal from the memory retention logic thus isolating the HEF4720B; V from the address and $\overline{CS}$ inputs.
2. The interface power supply can be separated from the TTL power supply by means of a low-value resistor (Fig. 10); a thyristor is connected from the interface power supply to earth. The system is arranged so that, upon switching off or failure of the interface supply, the thyristor turns on thus ensuring a rapid fall of the supply voltage.
3. The best solution is to select the interface circuits from the LOCMOS family and to feed all these circuits from the battery (Fig. 11). These stages then remain active when the TTL 5 V supply fails. The interface circuits are mostly only active on a clock pulse, have the possibility of being inactive on a gate level, or can be forced into one position.



(1) These devices have a battery supply.
(2) Alternative connection.

Fig. 9 Use of battery-operated LOCMOS gates to isolate the memory in case of power supply failure. Devices marked (1) are connected to the battery. The HEF4011B can sink about 0,7 mA: if the load is greater than this, only the memory should be connected, other loads being connected to the address latch as shown by the dashed-line connections.





(1) Leads should be so arranged to prevent cross-talk; thyristor connections must be short.
(2) Slope > 500 mV/μs in the vicinity of the threshold.

Fig. 10 Using a thyristor to ensure a rapid fall of interface supply at switch-off or supply failure.

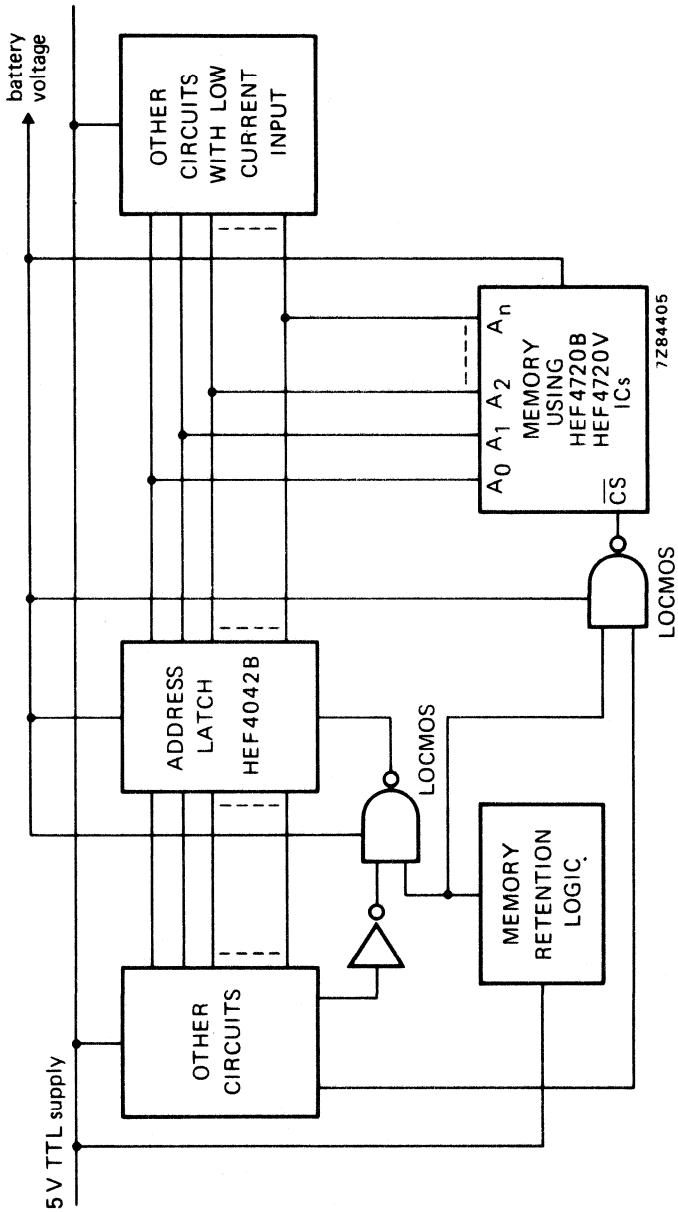


Fig. 11 Preferred solution for memory retention; all interface circuits are battery-fed LOCMOS. Note that maximum sink current of the HEF4042B is about 1,5 mA.

8-BIT ADDRESSABLE LATCH

The HEF4724B is an 8-bit addressable latch with three address inputs (A_0 to A_2), a data input (D), an active LOW enable input ($\overline{E}$), an active HIGH clear input (CL), and eight parallel latch outputs (O_0 to O_7).

When $\overline{E}$ and CL are HIGH, all outputs (O_0 to O_7) are LOW. Eight-channel demultiplexing or active HIGH 1-of-8 decoding with output enable operation occurs when CL is HIGH and $\overline{E}$ is LOW. When CL and $\overline{E}$ are LOW, the selected output (O_0 to O_7; determined by A_0 to A_2) follows D. When $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of A_0 to A_2 could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

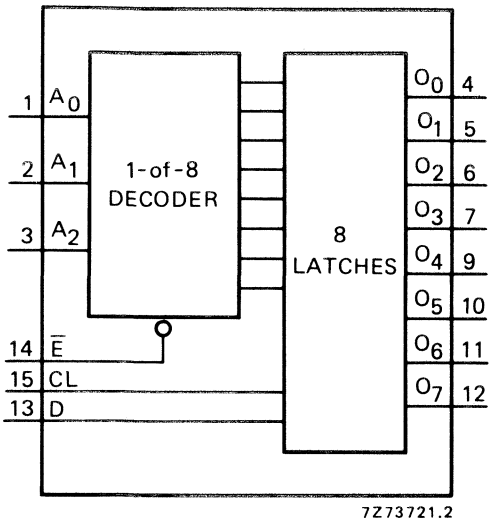


Fig. 1 Functional diagram.

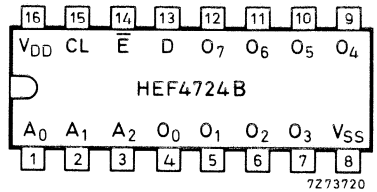


Fig. 2 Pinning diagram.

HEF4724BP : 16-lead DIL; plastic (SOT-38Z).
HEF4724BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4724BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

A_0 to A_2	address inputs
D	data input
$\overline{E}$	enable input (active LOW)
CL	clear input (active HIGH)
O_0 to O_7	parallel latch outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Products approved to CECC 90 104-089.

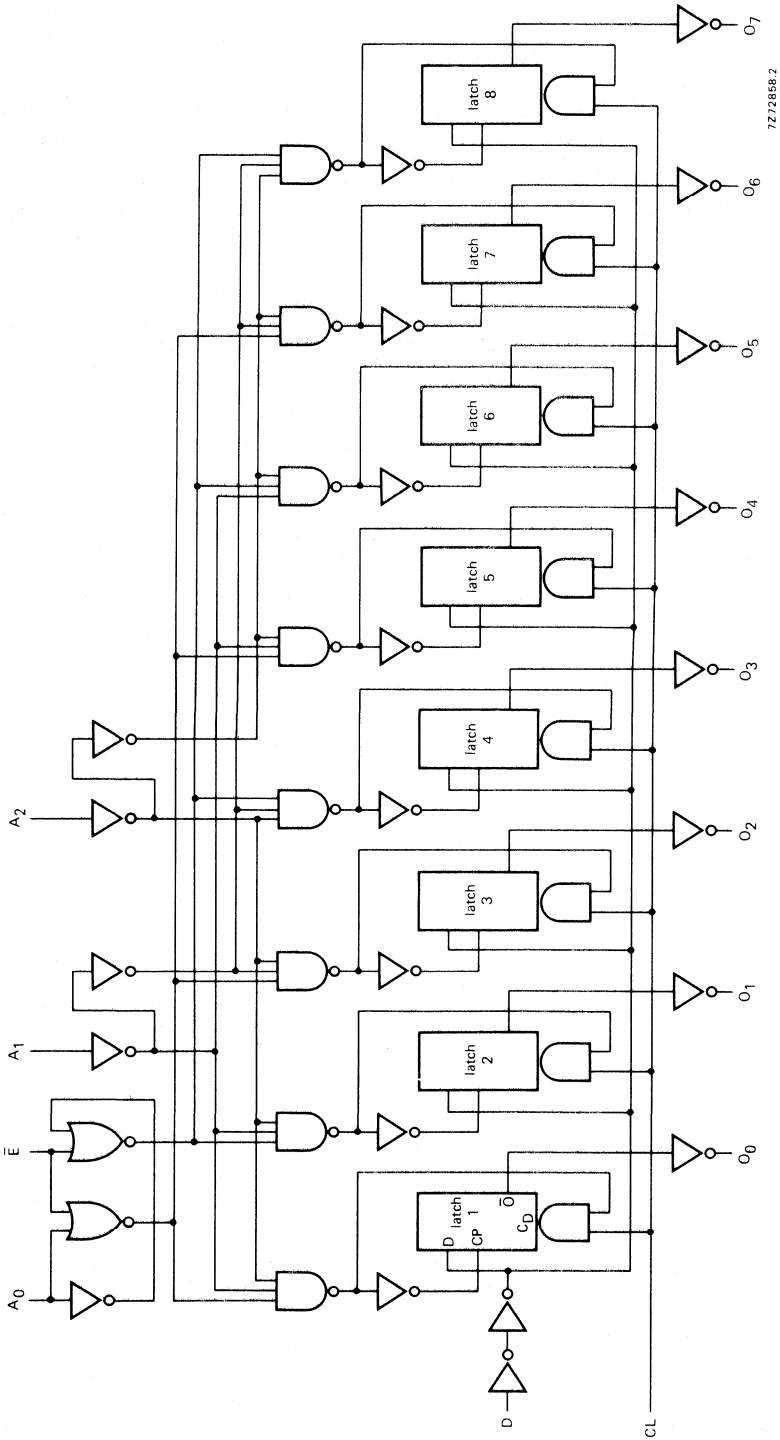


Fig. 3 Logic diagram.

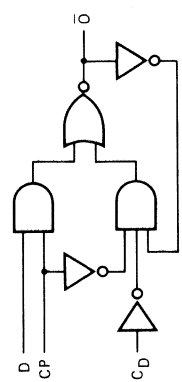


Fig. 4 Logic diagram (one latch).

MODE SELECTION

$\overline{E}$	CL	mode
L	L	addressable latch
H	L	memory
L	H	active HIGH 8-channel demultiplexer
H	H	clear

FUNCTION TABLE

CL	$\overline{E}$	D	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	mode
H	H	X	X	X	X	L	L	L	L	L	L	L	L	clear
H	L	D_1	L	L	L	D_1	L	L	L	L	L	L	L	demultiplexer; unaddressed latch is cleared
H	L	D_1	H	L	L	L	D_1	L	L	L	L	L	L	
H	L	D_1	L	H	L	L	L	D_1	L	L	L	L	L	
H	L	D_1	H	H	L	L	L	L	D_1	L	L	L	L	
H	L	D_1	L	L	H	L	L	L	L	D_1	L	L	L	
H	L	D_1	H	L	H	L	L	L	L	L	D_1	L	L	
H	L	D_1	L	H	H	L	L	L	L	L	L	D_1	L	
H	L	D_1	H	H	H	L	L	L	L	L	L	L	D_1	
L	H	X	X	X	X	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	memory
L	L	D_1	L	L	L	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	addressable latch; unaddressed latch holds previous state
L	L	D_1	H	L	L	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	L	H	L	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	H	H	L	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	L	L	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	H	L	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	
L	L	D_1	L	H	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	
L	L	D_1	H	H	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
O_{n-1} = state before the positive transition of $\overline{E}$
D_1 = either HIGH or LOW

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

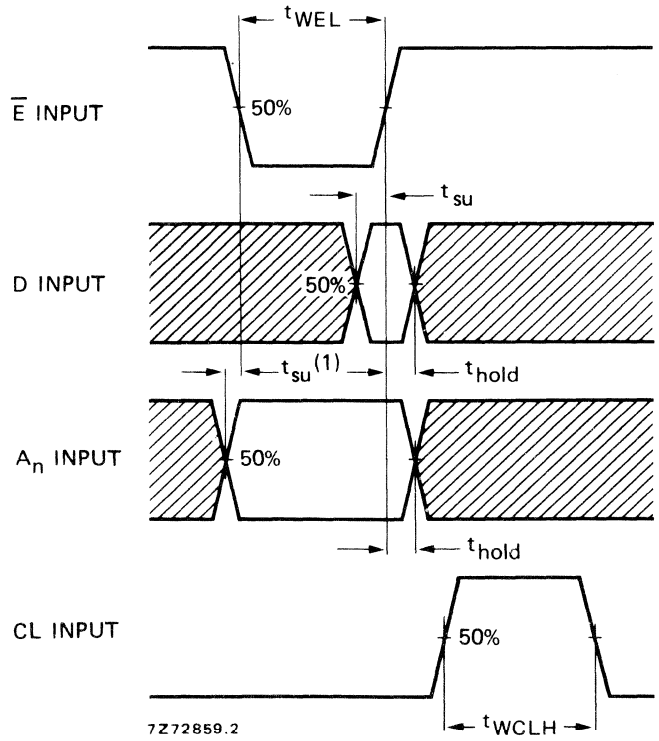
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{E} \rightarrow O_n$	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	195	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
$D \rightarrow O_n$	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	75	ns	24 ns + (0,23 ns/pF) C_L
	15			25	55	ns	17 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	75	ns	24 ns + (0,23 ns/pF) C_L
	15			25	55	ns	17 ns + (0,16 ns/pF) C_L
$A_n \rightarrow O_n$	5			110	225	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
$CL \rightarrow O_n$	5			85	165	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Set-up times	5		40	20		ns	
$D \rightarrow \overline{E}$	10	t_{su}	15	5		ns	
	15		10	0		ns	
	5		40	20		ns	
$A_n \rightarrow \overline{E}$	10	t_{su}	20	10		ns	
	15		15	5		ns	
Hold times	5		20	0		ns	
$D \rightarrow \overline{E}$	10	t_{hold}	15	5		ns	
	15		15	5		ns	see also waveforms Fig. 5
	5		50	25		ns	
$A_n \rightarrow \overline{E}$	10	t_{hold}	20	10		ns	
	15		15	5		ns	
Minimum $\overline{E}$	5		75	35		ns	
pulse width; LOW	10	t_{WEL}	30	15		ns	
	15		20	10		ns	
Minimum CL	5		70	35		ns	
pulse width; HIGH	10	t_{WCLH}	30	15		ns	
	15		20	10		ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times							
HIGH to LOW	5	t_{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L



(1) The address to enable set-up time is the time before the HIGH to LOW enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.

Fig. 5 Waveforms showing minimum $\overline{E}$ and CL pulse widths, set-up times, hold times. Set-up and hold times are shown as positive values but may be specified as negative values.

QUADRUPLE 64-BIT STATIC SHIFT REGISTER

The HEF4731B and HEF4731V are quadruple 64-bit static shift registers each with separate serial data inputs (D_A to D_D), clock inputs ($\overline{CP}_A$ to $\overline{CP}_D$) and data outputs (O_{63A} to O_{63D}) from the 64th register position.

Recommended supply voltage range for HEF4731B is 3 to 15 V and for HEF4731V is 4,5 to 12,5 V.

Data are shifted to the next stage on the negative-going transitions of the clock. Low impedance outputs are provided for direct interface to TTL.

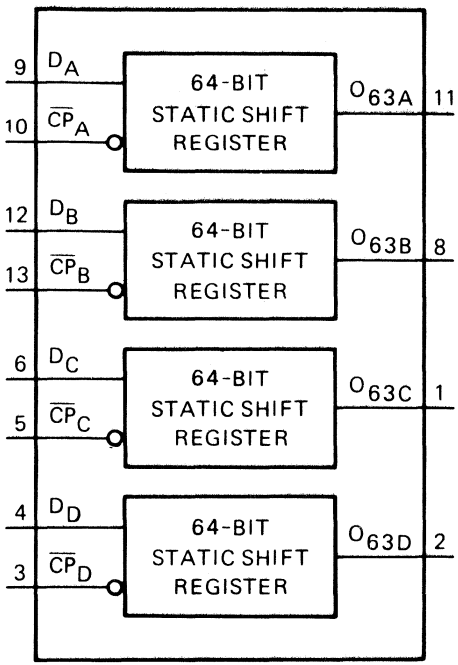


Fig. 1 Functional diagram. 7Z74633.1

Fig. 2 Pinning diagram. 7Z74631

HEF4731BP; HEF4731VP : 14-lead DIL; plastic (SOT-27).
HEF4731BD; HEF4731VD : 14-lead DIL; ceramic (cerdip) (SOT-73).

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

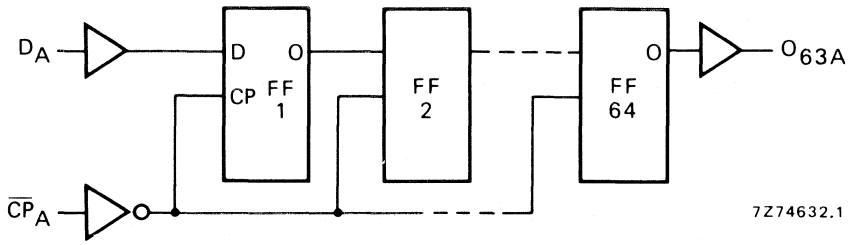


Fig. 3 Logic diagram (one of 64-bits shift register).

The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4731V, because of its reduced supply voltage range.

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}

	V_{DD} V	V_{OL} V	V_{OH} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+ 25 min.	+ 25 max.	+ 85 min.	+ 85 max.	
Output (source) current HIGH	5		2,5	$-I_{OH}$	3		2,5		2,0		mA
	5		4,6		1		0,85		0,65		mA
	10		9,5		3		2,5		2,0		mA
	15		13,5		10		8,5		6,5		mA
Output (sink) current LOW	4,75	0,4		I_{OL}	2,3		2,0		1,6		mA
	10	0,5			6,0		5,0		4,0		mA
	15	1,5			20,0		18,0		14,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	13 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz)
	10	55 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_o = output freq. (MHz)
	15	140 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$\overline{CP} \rightarrow O_{63}$	5			145	290	ns	132 ns + (0,26 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	47 ns + (0,16 ns/pF) C_L
	15			40	80	ns	34 ns + (0,11 ns/pF) C_L
	5			160	320	ns	138 ns + (0,45 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	56 ns + (0,19 ns/pF) C_L
	15			45	90	ns	39 ns + (0,13 ns/pF) C_L
Transition times O_{63}	5			30	60	ns	10 ns + (0,40 ns/pF) C_L
HIGH to LOW	10	t_{THL}		12	24	ns	3 ns + (0,18 ns/pF) C_L
	15			10	20	ns	3 ns + (0,13 ns/pF) C_L
	5			40	80	ns	8 ns + (0,65 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		20	40	ns	5 ns + (0,30 ns/pF) C_L
	15			15	30	ns	5 ns + (0,20 ns/pF) C_L
Minimum clock	5		160	80		ns	
pulse width; HIGH	10	t_{WCPH}	60	30		ns	
	15		40	20		ns	
Set-up time	5		25	-5		ns	
D → $\overline{CP}$	10	t_{su}	15	-5		ns	see also waveforms Fig. 4
	15		15	-5		ns	
Hold time	5		50	20		ns	
D → $\overline{CP}$	10	t_{hold}	30	10		ns	
	15		20	5		ns	
Maximum clock	5		3	6		MHz	Note: the maximum
pulse frequency	10	f_{max}	8	16		MHz	power dissipation has
	15		12	25		MHz	to be observed

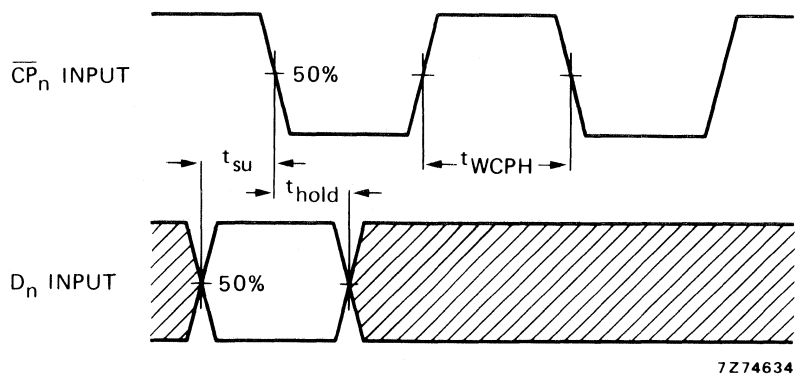


Fig. 4 Waveforms showing minimum clock pulse width, set-up and hold times for D to $\overline{CP}$. Set-up and hold times are shown as positive values but may be specified as negative values.

QUADRUPLE STATIC DECADE COUNTERS

The HEF4737B and HEF4737V are static quadruple decade counters for frequencies from 0 to 10 MHz. The counters are supplied with an extra overload flip-flop giving a total count capability of 19 999. The counter has the following inputs and outputs: a count input (CP), an asynchronous reset input (MR), an asynchronous preset input (PL), a transfer input (T), an output enable input (EO) (which controls the BCD outputs), the digit select inputs (S_A, S_B, S_C) (which perform selection of the contents of the latches to the 3-state BCD outputs (O_0 to O_3)), and the carry outputs (CO_2 to CO_5) (which give the carry signals of the decades except from the first decade).

The complementary MOS structure gives the devices very low stand-by and operating dissipation. Operating from a single supply voltage all outputs can drive one standard TTL input without interface circuitry under all specified operating conditions.

The BCD digit outputs are LOCMOS 3-state outputs. The high impedance off-state feature allows common busing of the outputs. The counters are supplied with asynchronous reset and preset to 19 999 facilities making them suitable for counter and time base applications. All carry signals are available except from the first decade.

Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

Recommended supply voltage range for HEF4737B is 3 to 15 V and for HEF4737V is 4,5 to 12,5 V.

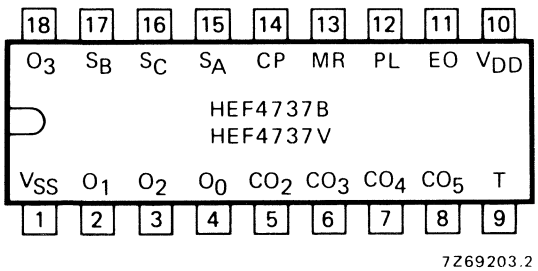


Fig. 1 Pinning diagram.

PINNING

CP	count input
MR	asynchronous reset input
PL	asynchronous preset input
T	transfer input
S_A, S_B, S_C	digit select inputs
EO	output enable input
O_0 to O_3	BCD outputs
CO_2 to CO_5	carry outputs

HEF4737BP; HEF4737VP: 18-lead DIL; plastic (SOT-102).
HEF4737BD; HEF4737VD: 18-lead DIL; ceramic (cerdip) (SOT-133B).

SUPPLY VOLTAGE

	rating	recommended operating	
HEF4737B	−0,5 to 18	3,0 to 15,0	V
HEF4737V	−0,5 to 18	4,5 to 12,5	V

FAMILY DATA

I_{DD} LIMITS category LSI } see Family Specifications

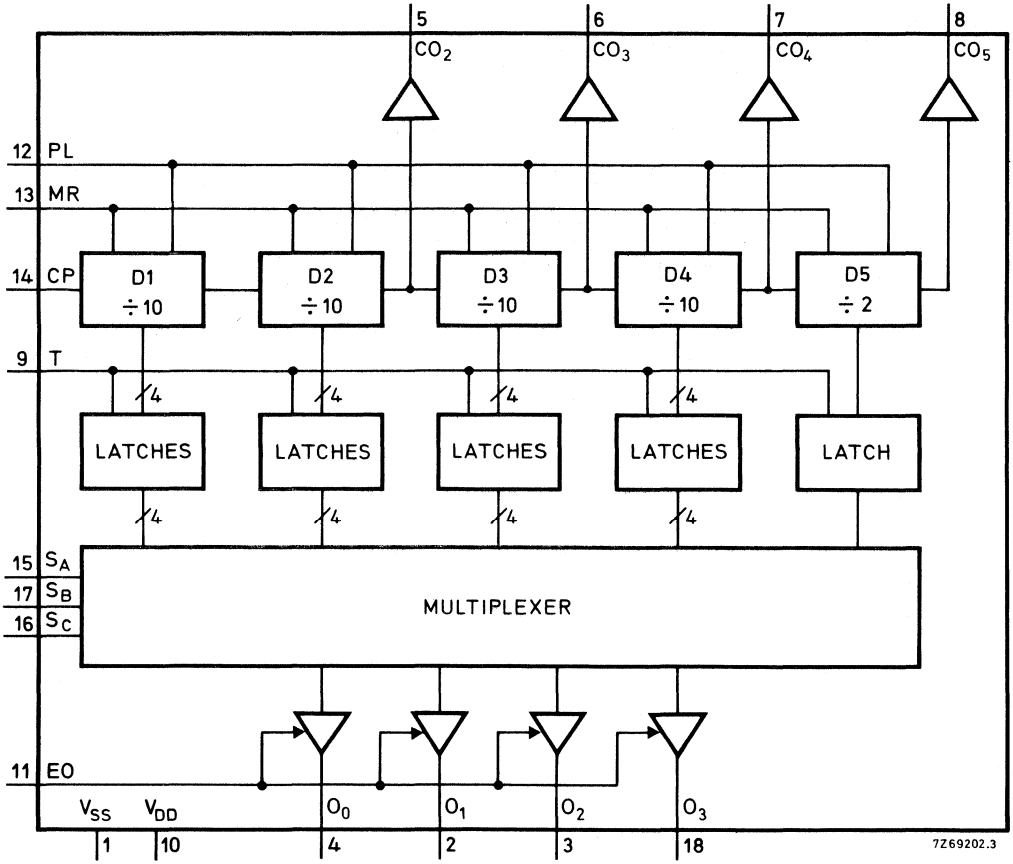


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION

Input signals

Count input (CP)

The signal to be counted is applied to this input. When PL and MR are LOW the contents of the counter increments by one at a LOW to HIGH transition of CP.

Reset input (MR)

This is an asynchronous reset. A HIGH level applied to this input will reset the counter to zero independent of the level at the count input and preset input.

Preset input (PL)

This is an asynchronous preset. When MR is LOW a HIGH at the PL input will preset the counter to 19 999 independent of the level at the count input.

Transfer input (T)

A HIGH level applied to this input allows the information held by the counter to pass to the latches.

Output enable input (EO)

A HIGH level at this input enables the BCD outputs and information can be read out of the latches using the multiplexer. A LOW level at this input disables the BCD outputs making them floating (high impedance off-state).

Digit select inputs (S_A, S_B, S_C)

S_A	S_B	S_C	
L	L	L	selects D1 (LSD)
H	L	L	selects D2
L	H	L	selects D3
H	H	L	selects D4
X	X	H	selects D5 (MSD)

When D5 is selected, the contents of D5 is available at O_0 and O_1, O_2 and O_3 are LOW.

LSD = least significant divider
MSD = most siginificant divider

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

Output signals

The carry outputs are active LOW outputs.

Carry output CO_2

When the contents of the first two decades of the counter are both 9 then the CO_2 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first two decades are zero. CO_2 is LOW when the contents of the counter are: 00 099, 00 199, 00 299 etc.

Carry output CO_3

When the contents of the first three decades of the counter are all 9 then the CO_3 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first three decades are zero. CO_3 is LOW when the contents of the counter are 00 999, 01 999, 02 999 etc.

Carry output CO_4

When the contents of the first four decades of the counter are all 9 then the CO_4 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first four decades are zero. CO_4 is LOW when the contents of the counter are 09 999 and 19 999.

The carry signals CO_2, CO_3 and CO_4 are suppressed while the preset is active. A HIGH to the preset input sets the counter to 19 999 but the carry signals remain HIGH until preset input returns to LOW, then the carry outputs will also become LOW.

Carry output CO_5

When the content of the counter is 10 000 the CO_5 output becomes LOW. It returns to HIGH when the content of the counter is zero.

Digit outputs (O_0 to O_3)

The digit outputs give the contents of the selected latch. The output is in the form of BCD, positive logic.

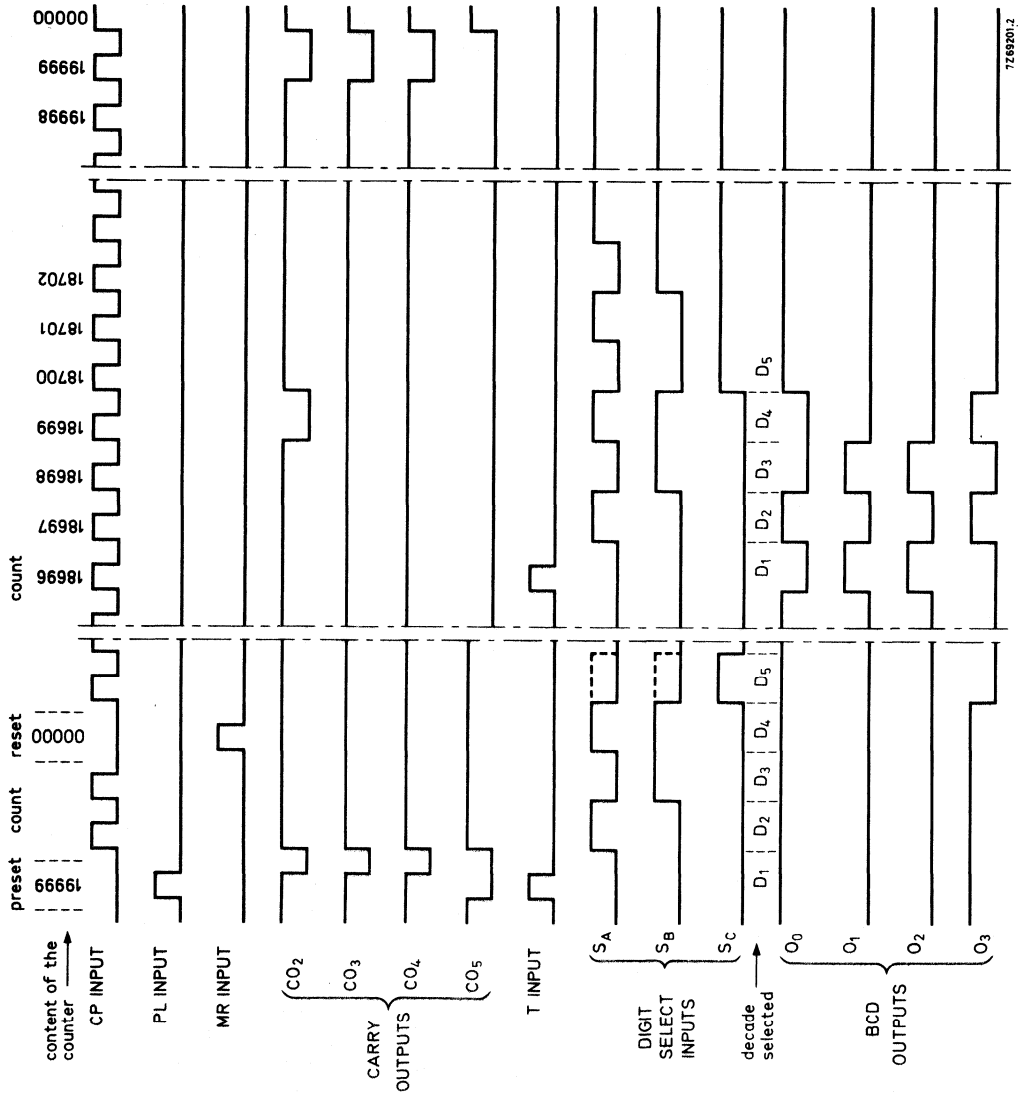


Fig. 3 Timing diagram.

The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4737V, because of its reduced supply voltage range.

D.C. CHARACTERISTICS V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Input leakage current at V_I = 0 or V_{DD}	10			$\pm I_{IN}$	–	–	–	0,3	–	1	μA
	15				–	–	–	0,3	–	1	μA
Output (sink) current LOW	4,75		0,4	I_{OL}	1,6	–	1,6	–	1,4	–	mA
	10		0,5		2,5	–	2,3	–	1,7	–	mA
	15		1,5		7,0	–	6,0	–	4,0	–	mA
Output (source) current HIGH	5	4,6		$-I_{OH}$	0,96	–	0,80	–	0,65	–	mA
	10	9,5			2,4	–	2,0	–	1,6	–	mA
	15	13,5			7,0	–	6,0	–	4,5	–	mA
Output (source) current HIGH	5	2,5		$-I_{OH}$	3,0	–	2,5	–	2,0	–	mA
3-state output leakage current V_O = 0 or V_{DD}	10			$\pm I_{OZ}$	–	1,6	–	1,6	–	12	μA
	15				–	1,6	–	1,6	–	12	μA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 15 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays CP ⟶ O_n (D1 selected) HIGH to LOW	5	t_{PHL}		320	640	ns	308 ns + (0,24 ns/pF) C_L
	10			120	240	ns	125 ns + (0,10 ns/pF) C_L
	15			90	180	ns	86 ns + (0,07 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		320	640	ns	296 ns + (0,48 ns/pF) C_L
	10			120	240	ns	110 ns + (0,20 ns/pF) C_L
	15			90	180	ns	82 ns + (0,15 ns/pF) C_L
CP ⟶ O_n (D5 selected) HIGH to LOW	5	t_{PHL}		620	1240	ns	608 ns + (0,24 ns/pF) C_L
	10			330	660	ns	325 ns + (0,10 ns/pF) C_L
	15			250	500	ns	246 ns + (0,07 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		620	1240	ns	596 ns + (0,48 ns/pF) C_L
	10			330	660	ns	320 ns + (0,20 ns/pF) C_L
	15			250	500	ns	242 ns + (0,15 ns/pF) C_L
CP ⟶ CO_2 HIGH to LOW	5	t_{PHL}		220	440	ns	208 ns + (0,24 ns/pF) C_L
	10			110	220	ns	105 ns + (0,10 ns/pF) C_L
	15			85	170	ns	81 ns + (0,07 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		220	440	ns	196 ns + (0,48 ns/pF) C_L
	10			110	220	ns	100 ns + (0,20 ns/pF) C_L
	15			85	170	ns	77 ns + (0,15 ns/pF) C_L

A.C. CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 15 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → CO_5	5			350	700	ns	338 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		160	320	ns	155 ns + (0,10 ns/pF) C_L
	15			120	240	ns	116 ns + (0,07 ns/pF) C_L
	5			350	700	ns	326 ns + (0,48 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		160	320	ns	150 ns + (0,20 ns/pF) C_L
	15			120	240	ns	112 ns + (0,15 ns/pF) C_L
S_n → O_n	5			200	400	ns	188 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	75 ns + (0,10 ns/pF) C_L
	15			55	110	ns	51 ns + (0,07 ns/pF) C_L
	5			200	400	ns	176 ns + (0,48 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	160	ns	70 ns + (0,20 ns/pF) C_L
	15			55	110	ns	47 ns + (0,15 ns/pF) C_L
T → O_n	5			220	440	ns	208 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	85 ns + (0,10 ns/pF) C_L
	15			60	120	ns	56 ns + (0,07 ns/pF) C_L
	5			220	440	ns	196 ns + (0,48 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		90	180	ns	80 ns + (0,20 ns/pF) C_L
	15			60	120	ns	52 ns + (0,15 ns/pF) C_L
MR → O_n	5			490	980	ns	478 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		200	400	ns	195 ns + (0,10 ns/pF) C_L
	15			60	120	ns	56 ns + (0,07 ns/pF) C_L
PL → O_n	5			260	520	ns	236 ns + (0,48 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		110	220	ns	100 ns + (0,20 ns/pF) C_L
	15			85	170	ns	77 ns + (0,15 ns/pF) C_L
MR → CO_n	5			350	700	ns	326 ns + (0,48 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		160	320	ns	150 ns + (0,20 ns/pF) C_L
	15			120	240	ns	112 ns + (0,15 ns/pF) C_L
PL → CO_n	5			350	700	ns	338 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		160	320	ns	155 ns + (0,10 ns/pF) C_L
	15			120	240	ns	116 ns + (0,07 ns/pF) C_L
Output transition	5			35	70	ns	15 ns + (0,40 ns/pF) C_L
times; any output	10	t_{THL}		18	36	ns	9 ns + (0,18 ns/pF) C_L
HIGH to LOW	15			15	30	ns	8 ns + (0,13 ns/pF) C_L
	5			50	100	ns	15 ns + (0,70 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	13 ns + (0,33 ns/pF) C_L
	15			25	50	ns	13 ns + (0,23 ns/pF) C_L

	V_{DD} V	symbol	min.	typ.	max.		
3-state propagation delays							
Output disable times							
EO → O_n	5			60	120	ns	
HIGH	10	t_{PHZ}		35	70	ns	
	15			25	50	ns	
	5			60	120	ns	
LOW	10	t_{PLZ}		35	70	ns	
	15			25	50	ns	
Output enable times							
EO → O_n	5			90	180	ns	
HIGH	10	t_{PZH}		40	80	ns	
	15			30	60	ns	
	5			90	180	ns	
LOW	10	t_{PZL}		40	80	ns	
	15			30	60	ns	
Minimum CP pulse	5		160	80		ns	
width; LOW	10	t_{WCPL}	60	30		ns	
	15		50	25		ns	
Minimum MR pulse	5		100	50		ns	
width; HIGH	10	t_{WMRH}	50	25		ns	
	15		40	20		ns	
Minimum PL pulse	5		120	60		ns	
width; HIGH	10	t_{WPLH}	60	30		ns	
	15		50	25		ns	
Minimum T pulse	5		100	50		ns	
width; HIGH	10	t_{WTH}	40	20		ns	
	15		36	18		ns	
Maximum clock	5		3	6		MHz	
pulse frequency	10	f_{max}	8	16		MHz	
	15		10	20		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$950\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$11\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

IEC/IEEE BUS INTERFACE

The HEF4738V is an implementation of the IEC-bus as described in IEC report 66 CO 22 (interface system for programmable measuring apparatus) as well as in IEEE standard 488-1975 (standard digital interface for programmable instrumentation).
Together with bus-drivers, level converters and multiplexers it is suitable for connecting electronic programmable and non-programmable equipment to an IEC/IEEE interface bus.
All inputs have standard HE4000B family levels.
In the circuit the following standard interface functions are incorporated:

- Complete source handshake (subset SH1)
- Complete acceptor handshake (subset AH1)
- Basic talker with serial poll and talk-only mode (when It = LOW, subset T1; It = HIGH, subset T5)
- Basic listener with listen-only mode (when It = LOW, subset L1; It = HIGH, subset L3)
- Complete service request (subset SR1)
- Complete remote local (subset RL1)
- Remote parallel poll configuration (subset PP1)
- Complete device clear (subset DC1)
- Complete device trigger (subset DT1)
- Some controller facilities

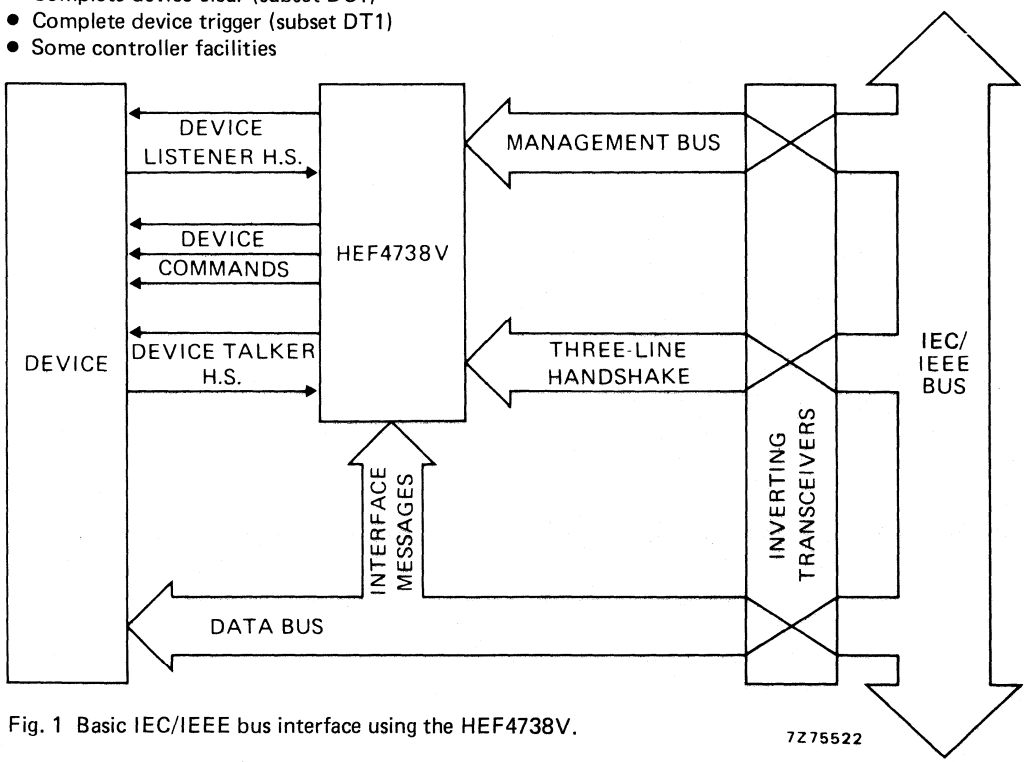


Fig. 1 Basic IEC/IEEE bus interface using the HEF4738V.

SUPPLY VOLTAGE

rating	recommended operating
−0,5 to 18	4,5 to 12,5 V

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

GENERAL DESCRIPTION

The inputs IRFD, IDAC, $\overline{\text{IDAV}}$, $\overline{\text{IIFC}}$, $\overline{\text{IREN}}$, $\overline{\text{IATN}}$, $\overline{\text{IIDY}}$ and IDIO1 to IDIO7 must be connected via an inverting TTL to LOCMOS level converter to the respective bus lines: NRFD, NDAC, DAV, IFC, REN, ATN, IDY and DIO1 to DIO7.

The outputs ORFD, ODAC, $\overline{\text{ODAV}}$ and $\overline{\text{OSRQ}}$ can drive one standard TTL load and are suitable for driving NRFD, NDAC, DAV and SRQ via an inverting bus-driver circuit.

The parallel poll outputs OP1, OP2, OP3 and OPP can also drive one standard TTL load. Outputs OP1, OP2 and OP3 are connected to flip-flops, which store the attendant bits P1, P2 and P3 of the last PPE message. OP1, OP2 and OP3 have to be decoded externally and multiplexed to the DIO-lines when OPP is LOW.

All other output stages are standard HE4000B family.

Most of the functions in the IEC/IEEE interface IC are realized with synchronous sequential logic, which is driven from the clock input CP. HIGH to LOW transitions are used to synchronize input signals and LOW to HIGH transitions trigger the internal flip-flops. In order to meet the IEC/IEEE timing specifications, the maximum clock frequency is 2 MHz. The maximum data transfer is then 200 kbytes/second.

Input $\overline{\text{Irdy}}$ (not ready for next message) and output Odvd (data valid device) are intended for a two-wire handshake procedure between the acceptor function in the IC and the data input of the device (instrument to be connected to the interface system). The procedure is made so, that if the device reacts fast enough, the handshake procedure can be omitted by interconnecting Odvd and $\overline{\text{Irdy}}$. The conditions to be fulfilled by the device are:

- The device must be able to accept a data byte within one clock period after dvd goes HIGH under all conditions.
- The device must be ready to process a data byte within two clock periods plus the minimum settling time of the talker devices under all conditions.

Input $\overline{\text{Inba}}$ (not new byte available) and output Odcd (don't change data) are intended for a two-wire handshake procedure with the source function in the IC and the data output of the device (instrument). The procedure is so made that if the device reacts fast enough the handshake procedure can be omitted by interconnecting Odcd and $\overline{\text{Inba}}$. The conditions to be fulfilled by the device are:

- The device must be able to set a new data byte on the bus within one clock period after dcd goes LOW under all conditions.
- The device must be able to have the next data byte available within seven clock periods under all conditions.

Input Isr and output Ored should be connected to an external parallel-in/serial-out (when Ored is HIGH parallel-in, when LOW serial-out) shift register, which must be connected to the clock CP and must trigger on the LOW to HIGH transitions. The data on the parallel inputs of this external shift register are loaded in parallel and shifted-out via input Isr into an internal shift register. The eleven serial input signals are in the order of shifting: A5, A4, A3, A2, A1, ton, lon, It, rsv, rtl and ist. Signals A5, A4, A3, A2 and A1 represent the device talker and listener address. When signal It (either listener or talker) is HIGH, a listener addressing sets the talker to the idle state and a talker addressing sets the listener to the idle state (subset T5 and L3). With It LOW, the device can be addressed to be a listener and a talker. Because of the serial input procedure, all these input signals arrive in the interface functions of the IC between 16 and 32 clock cycles.

The signals ton, lon, rsv, rtl and ist are standard IEC/IEEE inputs. When using ton or lon no controller action is possible.

The output Oclr or Otrg is HIGH for one clock pulse if DCAS (device clear active state) or DTAS (device trigger active state) respectively is active.

The output Oloc is HIGH when LOCS (local state) or LWLS (local with lock-out state) is active.
Output $\overline{OSRQ}$ is HIGH when the rsv signal is read from the external shift register and the SRQS (request service state) is active. After this request has been answered by a serial poll, $\overline{ORQS}$ is HIGH in the APRS (affirmative poll response state). The inverted signal on $\overline{ORQS}$ must be multiplexed to bus-line DIO7, together with the status byte of the other DIO lines, when output Osp is HIGH in the SPAS (serial poll active state).
When the device is in the SPAS state the signal rsv may be removed (can be checked on $\overline{ORQS}$).
N.B.: When the interface has asked for service via rsv and is addressed as talker in the serial poll mode, a handshake must be initialized by the device via $\overline{Inba}$.

Input Icats and output Otct are intended for use of this IC in a controller. When Icats is HIGH, the source handshake function will exit SIDS and SIWS and enter respectively SGNS and SWNS. When the controller function is not used, the input Icats must be connected to V_{SS}. Output Otct is HIGH if the tct message is sent over the interface and the ACDS state is active. A HIGH on input Ipon sets each function to its initial state. This level can be set to LOW after the IC has received 32 clock pulses at stabilized supply voltage.

Note

After power-on the input Ipon must stay LOW for at least 32 clock pulses, then HIGH for 32 clock pulses in order to force the function to its initial state.
After this, Ipon must be set LOW.

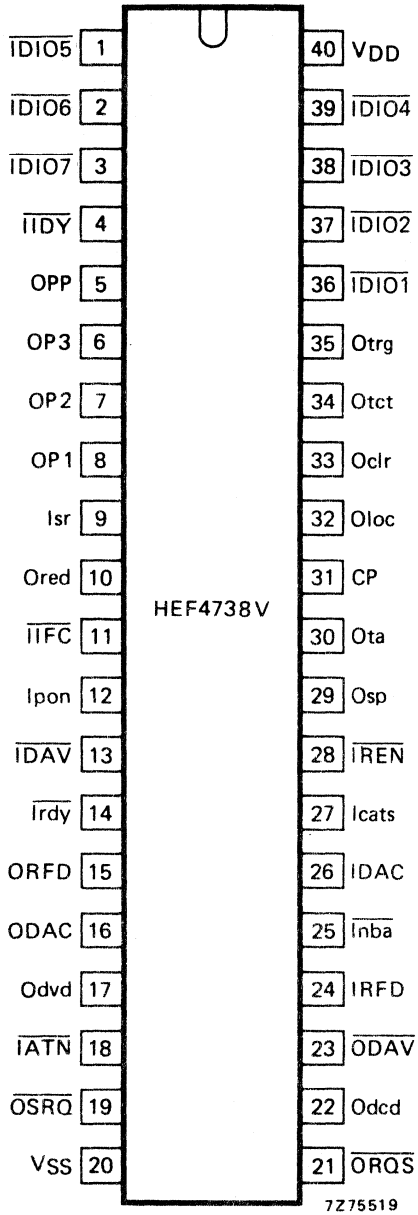


Fig. 2 Pinning diagram; for abbreviations see the following list.
HEF4738VP: 40-lead DIL; plastic (SOT-129).

Input pins

1,2,3,36, 37,38,39 = IDIO1 to 7:	input DIO
4 = IIDY	input IDY not
*9 = Isr	input shift register
11 = IIFC	input IFC not
12 = Ipon	input pon
13 = IDAV	input DAV not
14 = Irdy	input rdy not
18 = IATN	input ATN not
24 = IRFD	input RFD
25 = Inba	input nba not
26 = IDAC	input DAC
27 = Icats	input cats
28 = IREN	input REN not
31 = CP	clock pulse input

Output pins

5 = OPP	output PP
8,7,6, = OP1 to OP3	output P1 to P3
10 = Ored	output red
15 = ORFD	output RFD
16 = ODAC	output DAC
17 = Odvd	output dvd
19 = OSRQ	output SRQ not
21 = ORQS	output RQS not
22 = Odcd	output dcd
23 = ODAV	output DAV not
29 = Osp	output sp
30 = Ota	output ta
32 = Oloc	output loc
33 = Oclr	output clr
34 = Otct	output tct
35 = Otrg	output trg

Supply pins

20 = V_{SS}:	more negative supply line
40 = V_{DD}:	more positive supply line

* Isr is serial input for signals A5, A4, A3, A2, A1, ton, lon, It, rsv, rtl and ist.

Note

Because the circuit uses positive logic and the bus uses negative logic, all inputs and outputs to the bus must be inverted. For that reason, all terminals that are working with the bus have mnemonics which are the inverted ones of those on the bus.

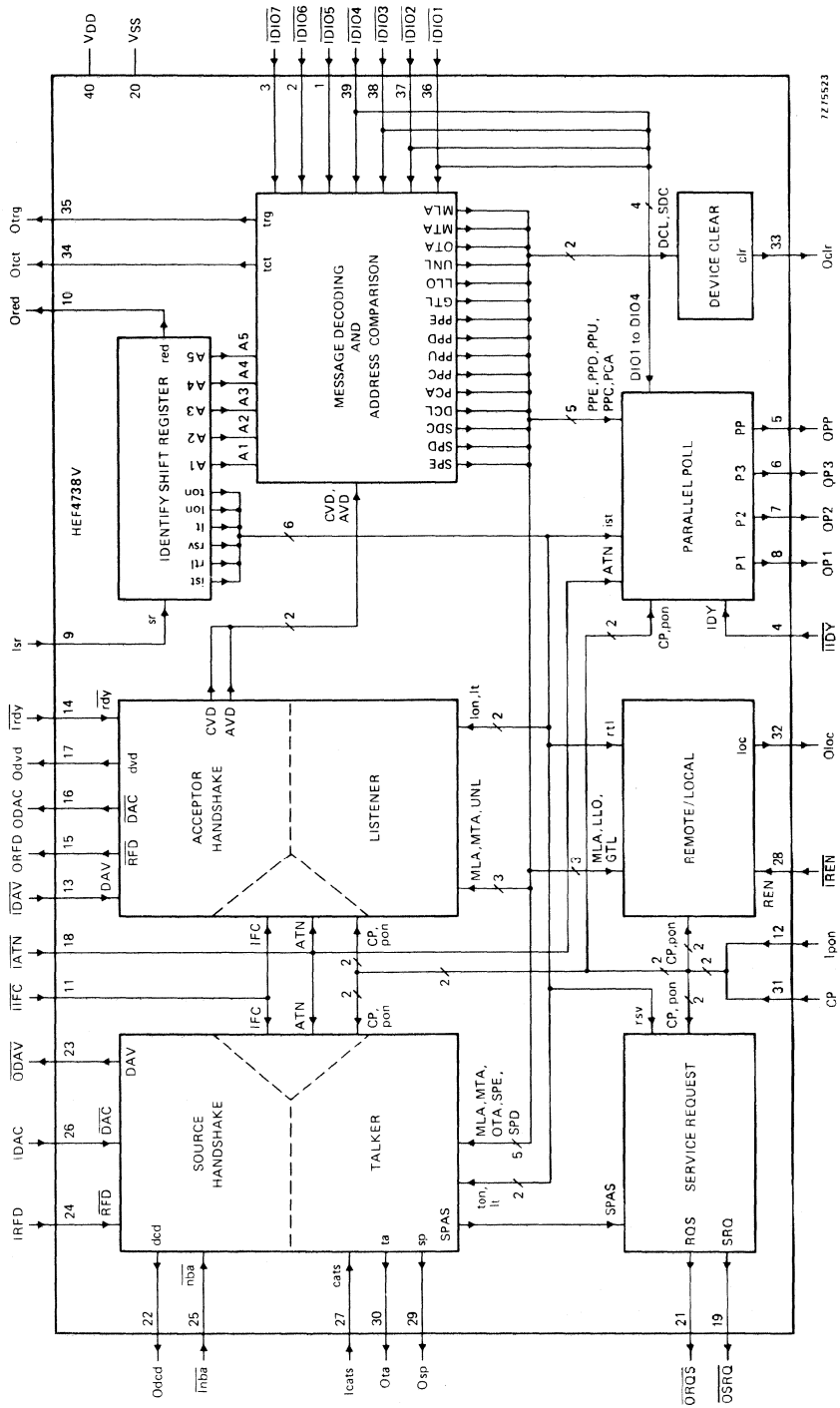


Fig. 3 Block diagram.

LIST OF USED ABBREVIATIONS

A1 to A5	address
ACDS	acceptor data state
APRS	affirmative poll response state
ATN	attention
AVD	address valid
cats	controller active or transfer state
clr	device clear
CVD	command valid
DAC	data accepted
DAV	data valid
DCAS	device clear active state
dcd	don't change data
DCL	device clear
DIO	data input output
DTAS	device trigger active state
dvd	data valid device
EOI	end of output/identify
GTL	go to local
IDY	identify
IFC	interface clear
ist	individual status
LLO	local lock-out
loc	local
LOCS	local state
lon	listen only
lt	decides whether the device can only be listener/talker or listener and talker simultaneously
LWLS	local with lock-out state
MLA	my listen address
MTA	my talk address
nba	new byte available
NRFD	not ready for data
NDAC	not data accepted
OTA	other talk address
P1 to P3	parallel response messages
PCA	parallel poll configure accepted
pon	power on
PP	parallel poll message enable
PPC	parallel poll configure
PPD	parallel poll disable
PPE	parallel poll enable
PPU	parallel poll unconfigure
rdy	ready for next message
red	ready for next shift cycle
REN	remote enable
RFD	ready for data
RQS	requested service
rsv	request for service
rtl	return to local
SDC	selected device clear
SGNS	source generate state
SIDS	source idle state
SIWS	source idle wait state
sp	serial poll
SPAS	serial poll active state
SPD	serial poll disable
SPE	serial poll enable
sr	shift register
SRQ	service request
SRQS	request service state
SWNS	source wait for new cycle state
ta	talker active
tct	talk control
ton	talk only
trg	trigger
UNL	unlisten

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	V_{OH} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output current HIGH; see note	5		2,5	$-I_{OH}$	3		2,5		2,0		mA
	5		4,6		1		0,85		0,65		mA
	10		9,5		3		2,5		2,0		mA
Output current LOW; see note	4,75	0,4		I_{OL}	2,7		2,3		1,8		mA
	10	0,5			9,5		8,0		6,3		mA
Quiscent device current	5			I_{DD}		50		50		375	μA
	10					100		100		750	μA

Note

Output currents for pins: 5 = OPP, 6 = OP3, 7 = OP2, 8 = OP1, 15 = ORFD, 16 = ODAC; 19 = $\overline{\text{OSRQ}}$, 23 = $\overline{\text{ODAV}}$. These pins can drive one standard TTL load.

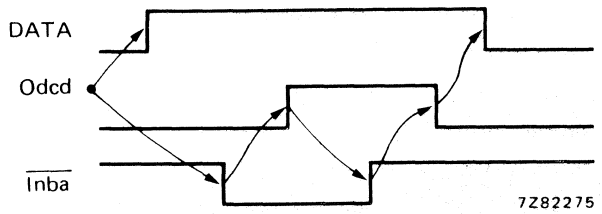


Fig. 4 Waveforms showing data exchange in talker function.

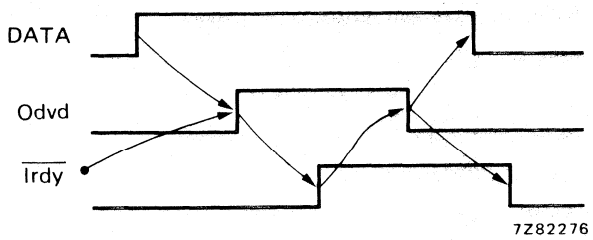


Fig. 5 Waveforms showing data exchange in listener function.

APPLICATION INFORMATION

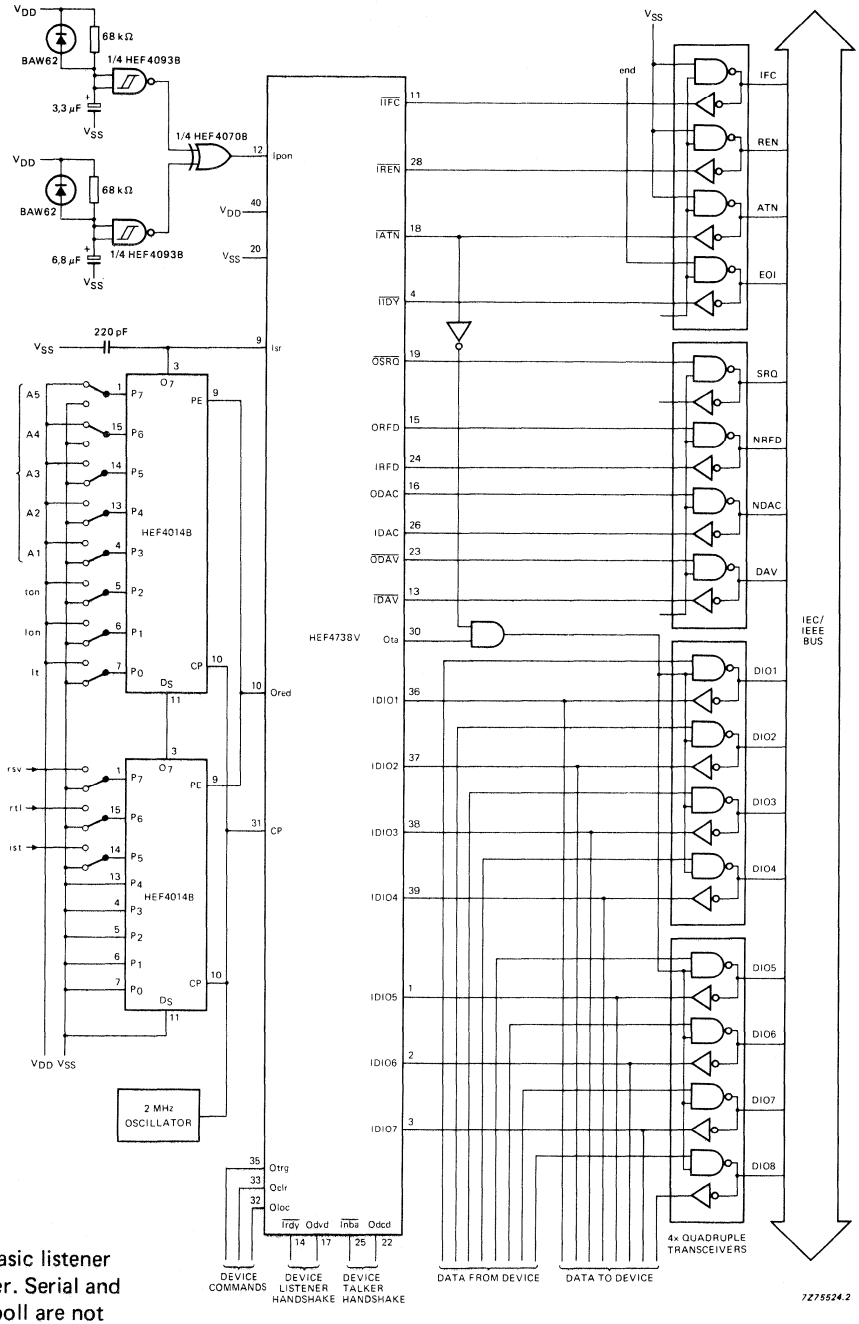


Fig. 6 Basic listener and talker. Serial and parallel poll are not implemented.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

FREQUENCY SYNTHESIZER

The HEF4750V frequency synthesizer is one of a pair of LOCMOS devices, primarily intended for use in high-performance frequency synthesizers, e.g. in all communication, instrumentation, television and broadcast applications. A combination of analogue and digital techniques results in an integrated circuit that enables high performance. The complementary device is the universal divider type HEF4751V.

Together with a standard prescaler, the two LOCMOS integrated circuits offer low-cost single loop synthesizers with full professional performance. Salient features offered (in combination with HEF4751V) are:

- Wide choice of reference frequency using a single crystal.
- High-performance phase comparator — low phase noise — low spurii.
- System operation to > 1 GHz.
- Typical 15 MHz input at 10 V.
- Flexible programming:
  - frequency offsets
  - ROM compatible
  - fractional channel capability.
- Programme range 6½ decades, including up to 3 decades of prescaler control.
- Division range extension by cascading.
- Built-in phase modulator.
- Fast lock feature.
- Out-of-lock indication.
- Low power dissipation and high noise immunity.

APPLICATION INFORMATION

Some examples of applications for the HEF4750V in combination with the HEF4751V are:

- VHF/UHF mobile radios.
- HF s.s.b. transceivers.
- Airborne and marine communications and navaids.
- Broadcast transmitters.
- High quality radio and television receivers.
- High performance citizens band equipment.
- Signal generators.

SUPPLY VOLTAGE

rating	recommended operating
−0,5 to + 15	9,5 to 10,5 V

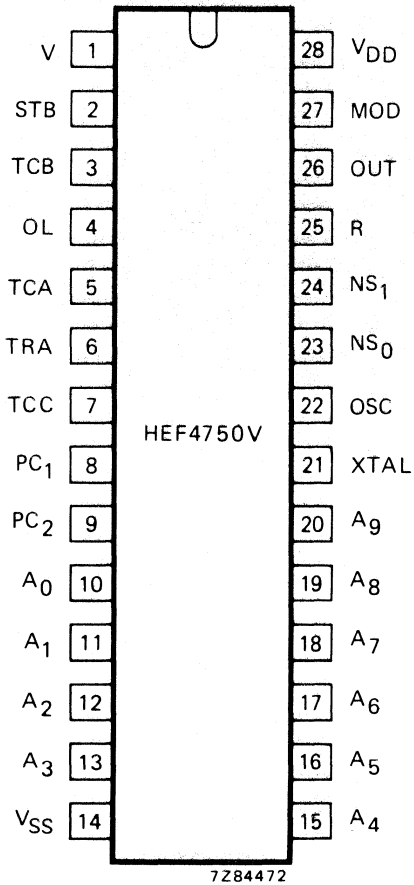


Fig. 1 Pinning diagram.

HEF4750VD: 28-lead DIL; ceramic (cerdip) (SOT-135A).

PINNING

R	phase comparator input, reference
V	phase comparator input
STB	strobe input
TCA	timing capacitor C_A pin
TCB	timing capacitor C_B pin
TCC	timing capacitor C_C pin
TRA	biasing pin (resistor R_A)
PC_1	analogue phase comparator output
PC_2	digital phase comparator output
MOD	phase modulation input
OL	out-of-lock indication
OSC	reference oscillator/buffer input
XTAL	reference oscillator/buffer output
A_0 to A_9	programming inputs/programmable divider
NS_0, NS_1	programming inputs, prescaler
OUT	reference divider output

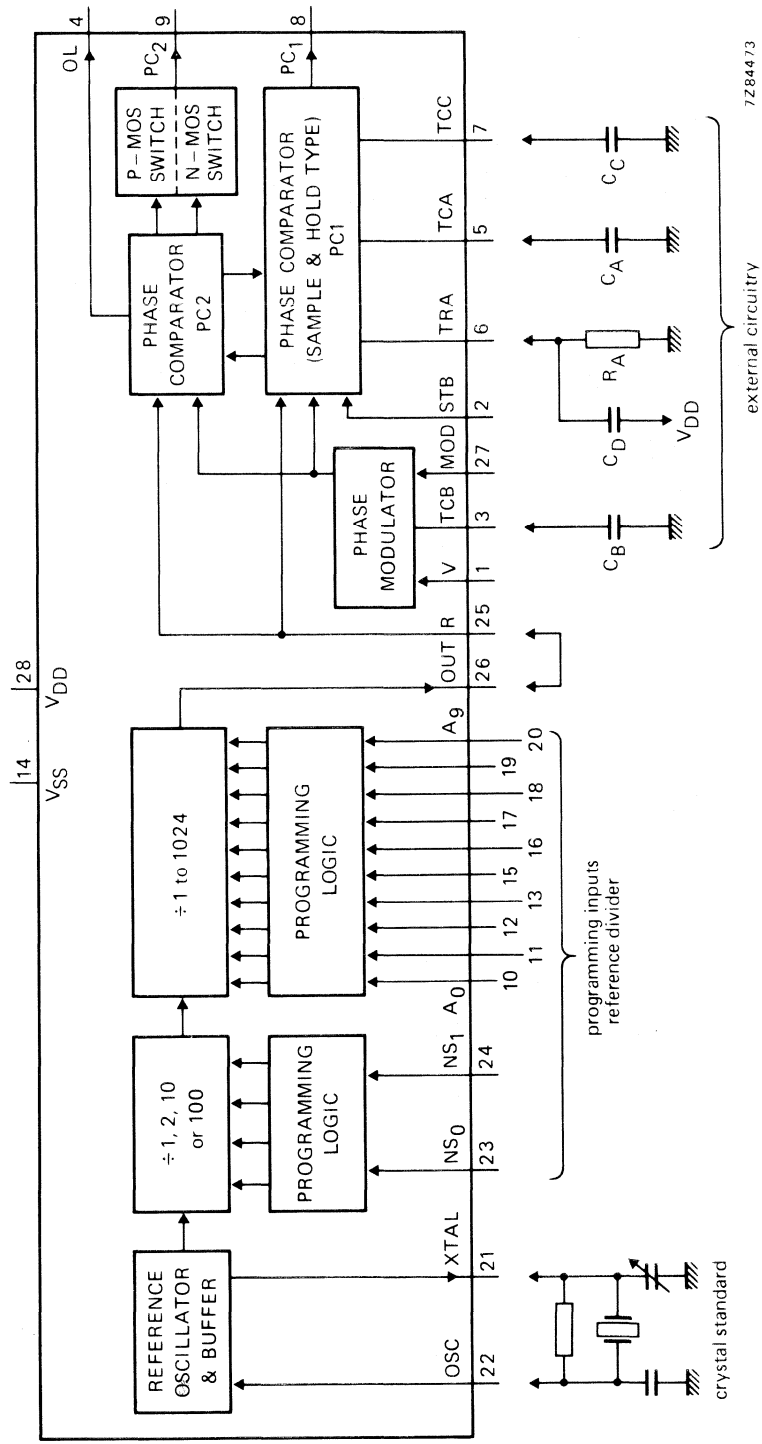


Fig. 2 Block diagram comprising five basic functions: phase comparator 1 (PC1), phase comparator 2 (PC2), phase modulator, reference oscillator and reference divider. These functions are described separately.

N.B. PC_1 = analogue output; PC_2 = 3-state output.

FUNCTIONAL DESCRIPTION

Phase comparator 1

Phase comparator 1 (PC1) is built around a SAMPLE and HOLD circuit. A negative-going transition at the V-input causes the hold capacitor (C_A) to be discharged and after a specified delay, caused by the Phase Modulator by means of an internal V' pulse, it produces a positive-going ramp. A negative-going transition at the R-input terminates the ramp. Capacitor C_A holds the voltage that the ramp has attained. Via an internal sampling switch this voltage is transferred to C_C and in turn buffered and made available at output PC_1.

If the ramp terminates before an R-input is present, an internal end of ramp (EOR) signal is produced.

These actions are illustrated in Fig. 3.

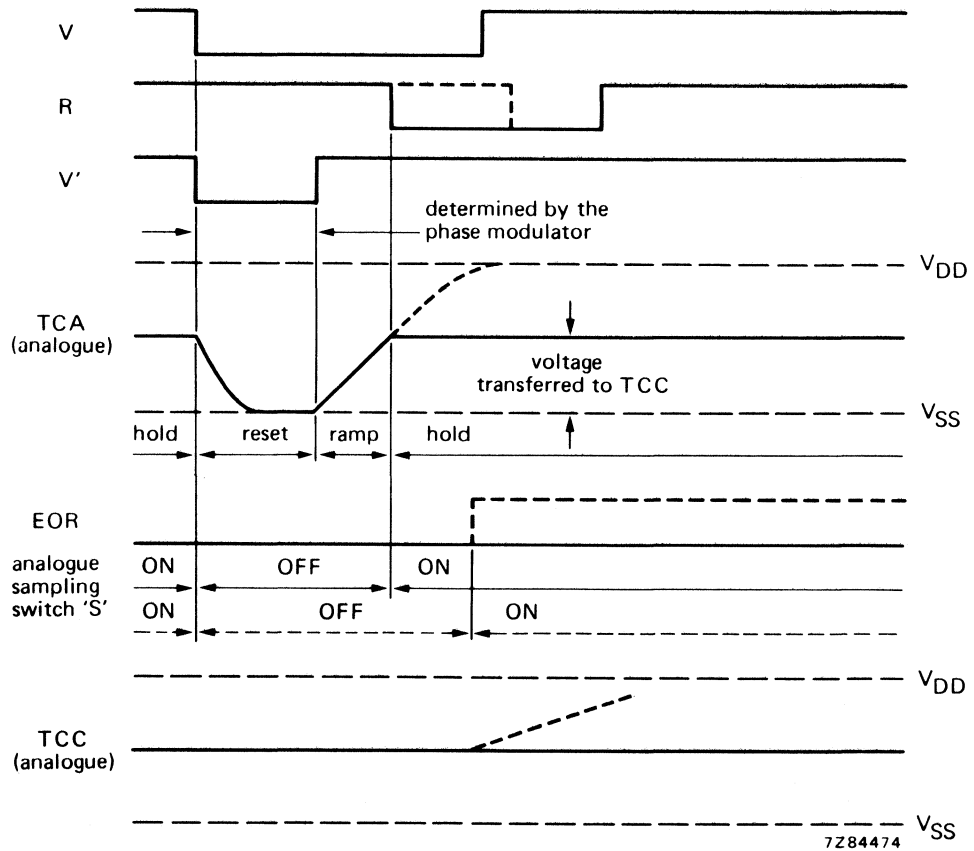


Fig. 3 Waveforms associated with PC1.

The resultant phase characteristic is shown in Fig. 4.

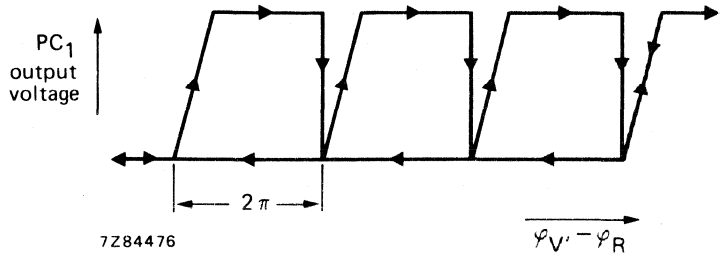


Fig. 4 Phase characteristic of PC_1.

PC1 is designed to have a high gain, typically 3200 V/cycle (at 12,5 kHz). This enables a low noise performance.

Phase comparator 2

Phase comparator 2 (PC2) has a wide range, which enables faster lock times to be achieved than otherwise would be possible. It has a linear ± 360° phase range, which corresponds to a gain of typically 5 V/cycle. This digital phase comparator has three stable states:

- reset state,
- V' leads R state,
- R leads V' state.

Conversion from one state to another takes place according to the state diagram of Fig. 5.

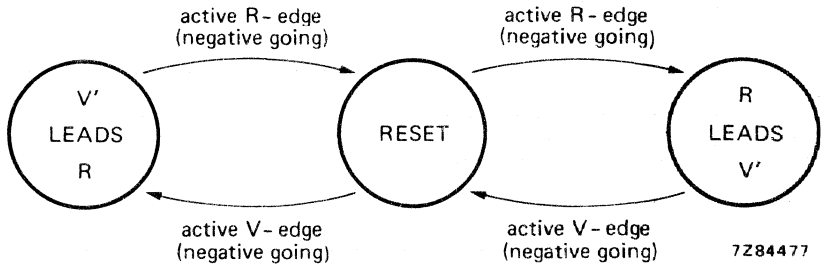


Fig. 5 State diagram of PC2.

Output PC_2 produces positive or negative-going pulses with variable width; they depend on the phase relationship of R and V'. The average output voltage is a linear function of the phase difference. Output PC_2 remains in the high impedance OFF-state in the region in which PC1 operates. The resultant phase characteristic is shown in Fig. 6.

FUNCTIONAL DESCRIPTION (continued)

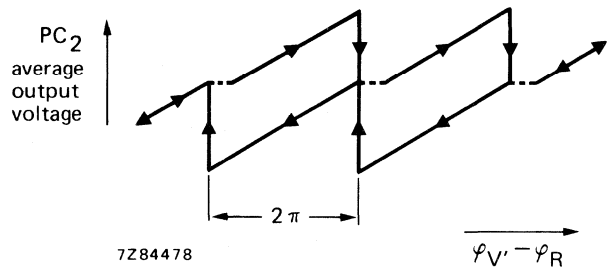


Fig. 6 Phase characteristic of PC_2.

Strobe function

The strobe function is intended for applications requiring extremely fast lock times. In normal operation the additional strobe input (STB) can be connected to the V-input and the circuit will function as described in the previous sections.

In single, phase-locked-loop type frequency synthesizers, the comparison frequency generally used is either the nominal channel spacing or a sub-multiple. PC2 runs at the higher frequency (a higher reference frequency must also be used), whilst strobing takes place on the lower frequency, thereby obtaining a decrease in lock time. In a system using the Universal Divider HEF4751V, the output OFS cycles on the lower frequency, the output OFF cycles on the higher frequency.

Out-of-lock function

There are a number of situations in which the system goes from the locked to the out-of-lock state (OL goes HIGH):

1. When V' leads R, however out of the range of PC1.
2. When R leads V'.
3. When an R-pulse is missing.
4. When a V-pulse is missing.
5. When two successive STB-commands occur, the first without corresponding V-signal.

Phase modulator

The phase modulator only uses one external capacitor, C_B at pin TCB. A negative-going transition at the V-input causes C_B to produce a positive-going linear ramp. When the ramp has reached a value almost equal to the modulation input voltage (at MOD), the ramp terminates, C_B discharges and a start signal to the C_A-ramp at TCA is produced. A linear phase modulation is reached in this way. If no modulation is required, the MOD-input must be connected to a fixed voltage of a certain positive value up to V_{DD}. Care must be taken that the V' pulse is never smaller than the minimum value to ensure that the external capacitor of PC1 (C_A) can be discharged during that time. Since the V' pulse width is directly related to the TCB ramp duration, there is a requirement for the minimum value of this ramp duration.

Reference oscillator

The reference oscillator normally operates with an external crystal as shown in Fig. 2. The internal circuitry can be used as a buffer amplifier in case an external reference should be required.

Reference divider

The reference divider consists of a binary divider with a programmable division ratio of 1 to 1024 and a prescaler with selectable division ratios of 1, 2, 10 and 100, according to the following tables:

- Binary divider

N (A_0 to A_9)	division ratio
0	1024
$0 \leqslant N \leqslant 1023$	N

- Prescaler

programming word (NS_0, NS_1)	division ratio
0	1
1	2
2	10
3	100

In this way suitable comparison frequencies can be obtained from a range of crystal frequencies. The divider can also be used as a 'stand alone' programmable divider by connecting input TRA to V_{DD}, which causes all internal analogue currents to be switched off.

Biasing circuitry

The biasing circuitry uses an external current source or resistor, which has to be connected between the TRA and V_{SS} pins. This circuitry supplies all analogue parts of the circuit. Consequently the analogue properties of the device, such as gain, charge currents, speed, power dissipation, impedance levels etc., are mainly determined by the value of the input current at TRA. The TRA input must be decoupled to V_{DD}, as shown in Fig. 7. The value of C_D has to be chosen such that the TRA input is 'clean', e.g. 10 nF at R_A = 68 kΩ.

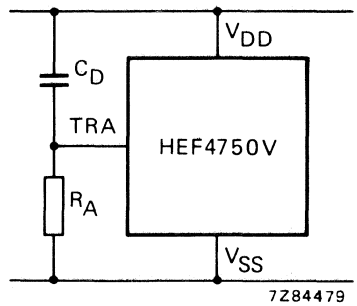


Fig. 7 Decoupling of input TRA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}		−0,5 to + 15	V
Voltage on any input	V_I		−0,5 to V_{DD} + 0,5	V
D.C. current into any input or output	± I	max.	10	mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max.	500	mW
Power dissipation per output for T_{amb} = 0 to 85 °C	P	max.	100	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Operating ambient temperature	T_{amb}		−40 to + 85	°C

D.C. CHARACTERISTICS at V_{DD} = 10 V ± 5%; voltages are referenced to V_{SS} = 0 V, unless otherwise specified; for definitions see note 1.

parameter	symbol	T_{amb} (°C									unit	notes
		−40			+ 25			+ 85				
		min.	typ.	max.	min.	typ.	max.	min.	typ.	max.		
Quiescent device current	I_{DD}	–	–	100	–	–	100	–	–	750	μA	2
Input current; logic inputs, MOD	± I_{IN}	–	–	300	–	–	300	–	–	1000	nA	3
Output leakage current at ½ V_{DD}												3, 4
TCA, hold-state	± I_Z	–	–	20	–	0,05	20	–	–	60	nA	
TCC, analogue switch OFF	± I_Z	–	–	20	–	0,05	20	–	–	60	nA	
PC_2, high impedance OFF-state	± I_Z	–	–	50	–	–	50	–	–	500	nA	
Logic input voltage												
LOW	V_{IL}	max. 0,3 V_{DD}									V	
HIGH	V_{IH}	min. 0,7 V_{DD}									V	
Logic output voltage												
LOW; at $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	50	–	–	50	–	–	50	mV	3
HIGH	V_{OH}	min. V_{DD}−50 mV									mV	3
Logic output current												
LOW; at V_{OL} = 0,5 V												3
outputs OL, PC_2, OUT	I_{OL}	5,5	–	–	4,6	–	–	3,6	–	–	mA	
output XTAL	I_{OL}	2,8	–	–	2,4	–	–	1,9	–	–	mA	

parameter	symbol	T_{amb} (°C)									unit	notes
		−40			+ 25			+ 85				
		min.	typ.	max.	min.	typ.	max.	min.	typ.	max.		
Logic output current HIGH; at $V_{OH} = V_{DD}-0,5$ V												3
outputs OL, PC_2, OUT	$-I_{OH}$	1,5	–	–	1,3	–	–	1,0	–	–	mA	
output XTAL	$-I_{OH}$	1,4	–	–	1,2	–	–	0,9	–	–	mA	
Output TCC sink current	I_O	–	–	–	–	2,1	–	–	–	–	mA	3,4,5
Output TCC source current	$-I_O$	–	–	–	–	1,9	–	–	–	–	mA	3,4,6
Internal resistance of TCC |output swing| ≤ 200 mV specified output range: 0,3 V_{DD} to 0,7 V_{DD}	R_i	–	–	–	–	0,7	–	–	–	–	kΩ	3,4
Output TCC voltage with respect to TCA input voltage	ΔV	–	0	–	–	0	–	–	0	–	V	3,4,7
Output PC_1 sink current	I_O	–	–	–	–	1,1	–	–	–	–	mA	3,4,8
Output PC_1 source current	$-I_O$	–	–	–	–	1,0	–	–	–	–	mA	3,4,9
Internal resistance of PC_1 |output swing| ≤ 200 mV specified output range: 0,3 V_{DD} to 0,7 V_{DD}	R_i	–	–	–	–	1,4	–	–	–	–	kΩ	3,4
Output PC_1 voltage with respect to TCC input voltage	ΔV	–	0	–	–	0	–	–	0	–	V	3,4,10
EOR generation $V_{EOR} = V_{DD}-V_{TCA}$	V_{EOR}	–	0,9	–	–	0,7	–	–	0,6	–	V	3,4,11
Source current; HIGH at $V_{OUT} = ½ V_{DD}$; output in ramp mode												3,4
TCA	I_O	–	–	–	–	13	–	–	–	–	mA	
TCB	I_O	–	–	–	–	2,5	–	–	–	–	mA	

A.C. CHARACTERISTICS

General note

The dynamic specifications are given for the circuit built-up with external components as given in Fig. 8, under the following conditions; for definitions see note 1; for definitions of times see Fig. 19; V_{DD} = 10 V ± 5%; T_{amb} = 25 °C; input transition times ⩽ 20 ns; R_A = 68 kΩ ± 30% (see also note 4); C_A = 270 pF; C_B = 150 pF; C_C = 1 nF; C_D = 10 nF; unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions	notes
Slew rate							
TCA	S_{TCA}	–	52	–	V/μs	R_A = minimum	12
TCA	S_{TCA}	–	28	–	V/μs	R_A = maximum	12
TCB	S_{TCB}	–	20	–	V/μs	R_A = minimum	12
TCB	S_{TCB}	–	10	–	V/μs	R_A = maximum	12
Ramp linearity							
TCA	l_{TCA}	–	2	–	%		13
TCB	l_{TCB}	–	2	–	%		13
Start of TCA-ramp delay	t_{CBCA}	–	200	–	ns		
Delay of TCA-hold	t_{RCA}	–	40	–	ns		
Delay of TCA-discharge	t_{VCA}	–	60	–	ns		
Start of TCB-ramp delay	t_{VCB}	–	60	–	ns		
TCB-ramp duration	t_{rCB}	–	250	–	ns	V_{MOD} = 4 V	
	t_{rCB}	–	350	–	ns	V_{MOD} = 6 V	
	t_{rCB}	–	450	–	ns	V_{MOD} = 8 V	
Required TCB min. ramp duration	t_{rCB}	–	150	–	ns		14
Pulse width							
V : LOW	t_{PWVL}	–	20	–	ns		
V : HIGH	t_{PWVH}	–	20	–	ns		
R : LOW	t_{PWRL}	–	20	–	ns		
R : HIGH	t_{PWRH}	–	20	–	ns		
STB : LOW	t_{PWSL}	–	20	–	ns		
STB : HIGH	t_{PWSH}	–	20	–	ns		
Fall time							
TCA	t_{fCA}	–	50	–	ns		
TCB	t_{fCB}	–	50	–	ns		
Prescaler input frequency	f_{PR}	–	30	–	MHz	all division ratios	
Binary divider frequency	f_{DIV}	–	30	–	MHz	all division ratios	
Crystal oscillator frequency	f_{OSC}	–	10	–	MHz		
Average power supply current						locked state	
with speed-up 1 : 10	I_P	–	3,6	–	mA		15
without speed-up	I_P	–	3,2	–	mA		16

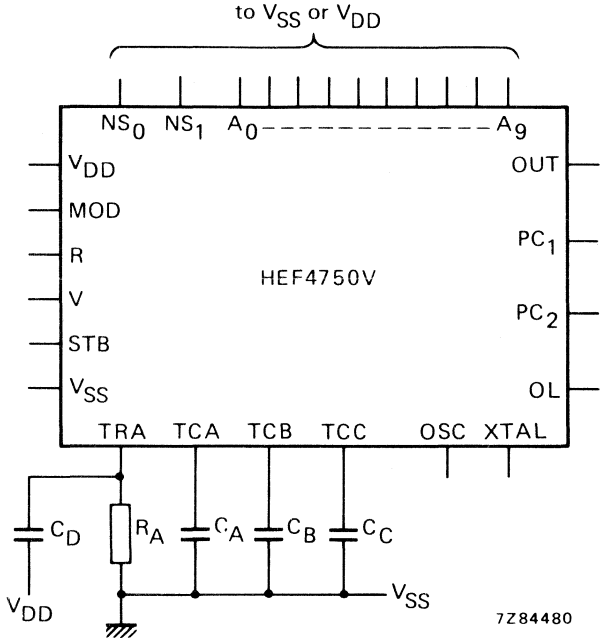


Fig. 8 Test circuit for measuring a.c. characteristics.

NOTES

1. Definitions:
   R_A = external biasing resistor between pins TRA and V_{SS}; 68 kΩ ± 30%.
   C_A = external timing capacitor for time/voltage converter, between pins TCA and V_{SS}.
   C_B = external timing capacitor for phase modulator, between pins TCB and V_{SS}.
   C_C = external hold capacitor between pins TCC and V_{SS}.
   C_D = decoupling capacitor between pins TRA and V_{DD}.
   Logic inputs: V, R, STB, A_0 to A_9, NS_0, NS_1, OSC.
   Logic outputs: OL, PC_2, XTAL, OUT.
   Analogue signals: TCA, TCB, TCC, TRA, PC_1, MOD.
2. TRA at V_{DD}; TCA, TCB, TCC and MOD at V_{SS}; logic inputs at V_{SS} or V_{DD}.
3. All logic inputs at V_{SS} or V_{DD}.
4. R_A connected; its value chosen such that I_{TRA} = 100 μA.
5. The analogue switch is in the ON position (see Fig. 9).

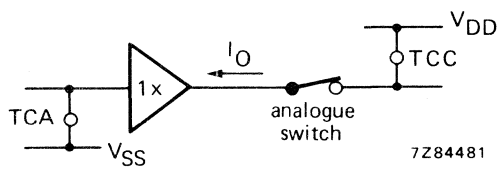


Fig. 9 Equivalent circuit for note 5.

NOTES (continued)

6. The analogue switch is in the ON position (see Fig. 10).

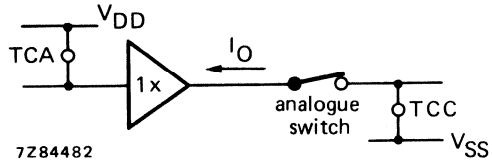


Fig. 10 Equivalent circuit for note 6.

7. This guarantees the d.c. voltage gain, combined with d.c.-offset.
Input condition: $0{,}3\ V_{DD} \leqslant V_{TCA} \leqslant 0{,}7\ V_{DD}$.
$\Delta V = V_{TCC} - V_{TCA}$.

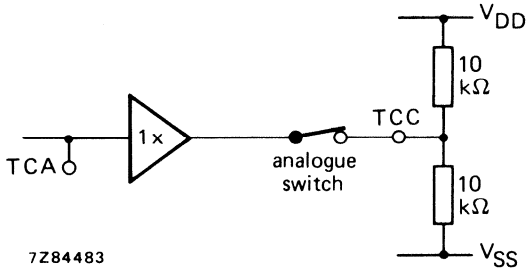


Fig. 11 Circuit for note 7.

8.

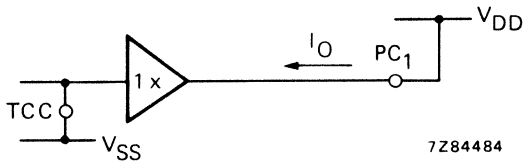


Fig. 12 Equivalent circuit for PC_1 sink current.

9.

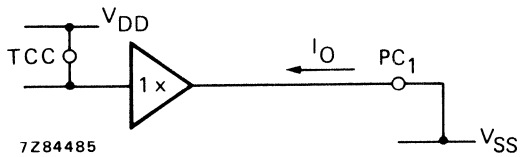


Fig. 13 Equivalent circuit for PC_1 source current.

10. This guarantees the d.c. voltage gain, combined with d.c.-offset.
Input condition: $0{,}3\ V_{DD} \leqslant V_{TCC} \leqslant 0{,}7\ V_{DD}$.
$\Delta V = V_{PC1} - V_{TCC}$.

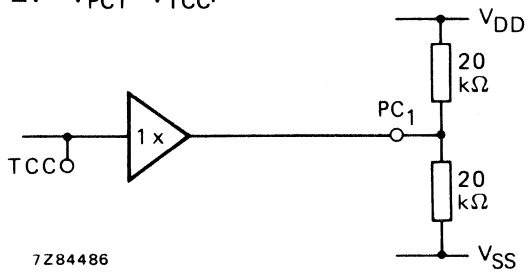


Fig. 14 Circuit for note 10.

11. Switching level at TCA, generating an EOR-signal, during increasing input voltage.
12.

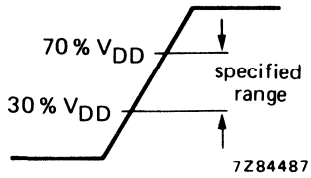


Fig. 15 Waveform at the output.

13. Definition of the ramp linearity at full swing.

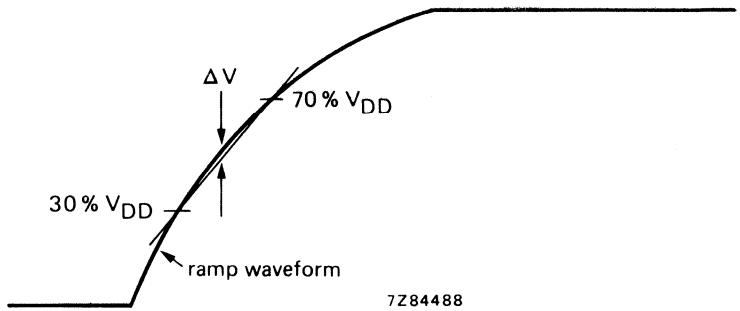


Fig. 16 ΔV is the maximum deviation of the ramp waveform to the straight line, which joins the 30% V_{DD} and 70% V_{DD} points.

$$\text{Linearity} = \frac{\Delta V}{\frac{1}{2} V_{DD}} \times 100\%.$$

14. The external components and modulation input voltage must be chosen such that this requirement will be fulfilled, to ensure that C_A is sufficiently discharged during that time.

NOTES (continued)

15. Circuit connections for power supply current specification, with speed-up 1 : 10. V and R are in the range of PC1, such that the output voltage at PC_1 is equal to 5 V.
    f_{OSC} = 5 MHz (external clock)
    f_{STB} = 12,5 kHz
    f_V = 125 kHz

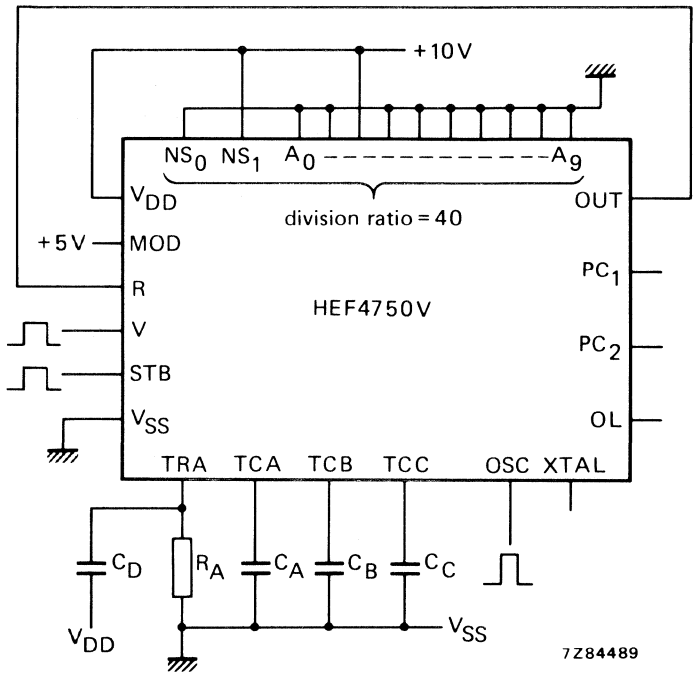


Fig. 17 Circuit for note 15.

16. Circuit connections for power supply current specification, without speed-up. V and R are in the range of PC1, such that the output voltage at PC_1 is equal to 5 V.
f_{OSC} = 5 MHz (external clock)
f_{STB} = 12,5 kHz
f_V = 12,5 kHz

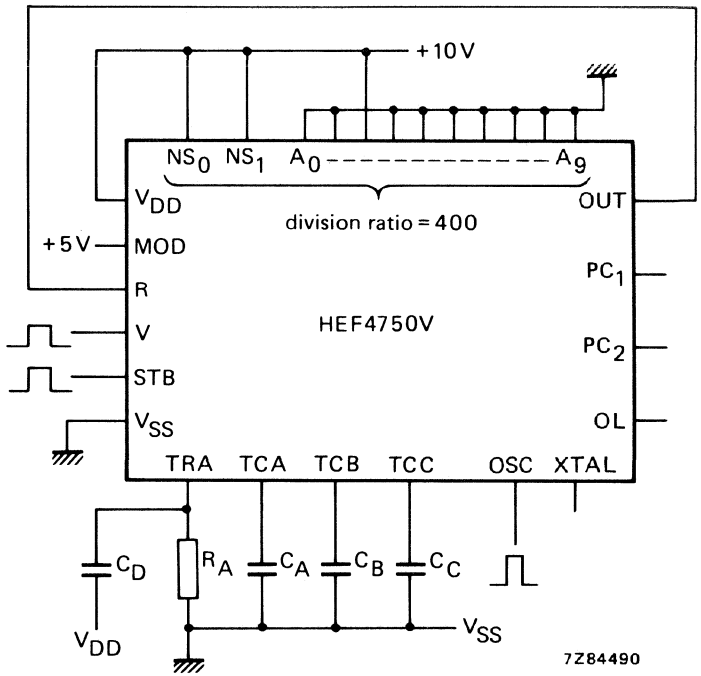
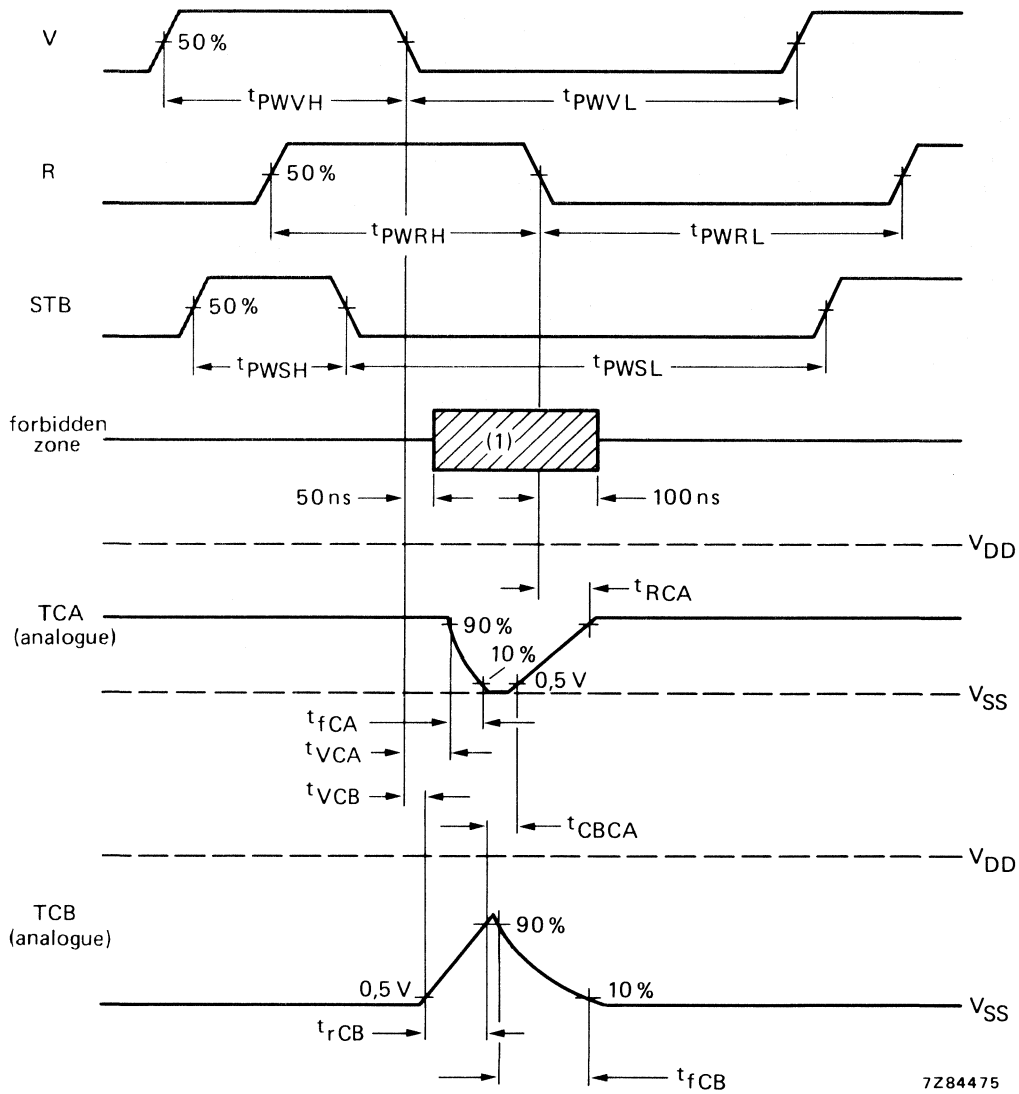


Fig. 18 Circuit for note 16.



(1) Forbidden zone in the *locked state* for the positive edge of V and R and both edges of STB.

Fig. 19 Waveforms showing times in the locked state.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

UNIVERSAL DIVIDER

The HEF4751V is a universal divider (U.D.) intended for use in high performance phase lock loop frequency synthesizer systems. It consists of a chain of counters operating in a programmable feedback mode. Programmable feedback signals are generated for up to three external (fast) ÷10/11 prescaler.

The system comprising one HEF4751V U.D. together with prescalers is a fully programmable divider with a maximum configuration of: 5 decimal stages, a programmable mode M stage ($1 \leqslant M \leqslant 16$, non-decimal fraction channel selection), and a mode H stage (H = 1 or 2, stage for half channel offset). Programming is performed in BCD code in a bit-parallel, digit-serial format.
To accommodate fixed or variable frequency offset, two numbers are applied in parallel, one being subtracted from the other to produce the internal programme.
The decade selection address is generated by an internal programme counter which may run continuously or on demand. Two or more universal dividers can be cascaded, each extra U.D. (in slave mode) adds two decades to the system. The combination retains the full programmability and features of a single U.D.
The U.D. provides a fast output signal FF at output OFF, which can have a phase jitter of ± 1 system input period, to allow fast frequency locking. The slow output signal FS at output OFS, which is jitter-free, is used for fine phase control at a lower speed.

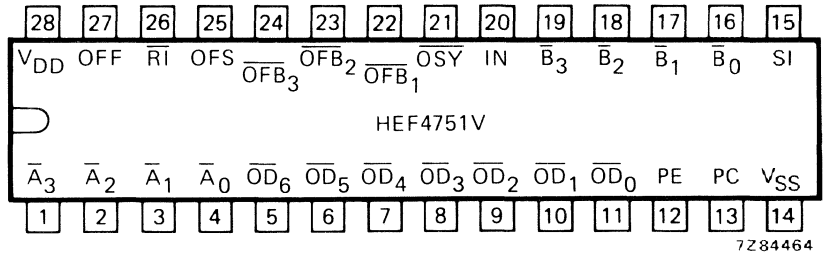


Fig. 1 Pinning diagram.

SUPPLY VOLTAGE

rating	recommended operating
−0,5 to +18	4,5 to 12,5 V

HEF4751VP : 28-lead DIL; plastic (SOT-117).
HEF4751VD: 28-lead DIL; ceramic (cerdip) (SOT-135A).
HEF4751VT : 28-lead mini-pack; plastic (SO-28; SOT-136A).

FAMILY DATA
I_{DD} LIMITS category LSI } see Family Specifications

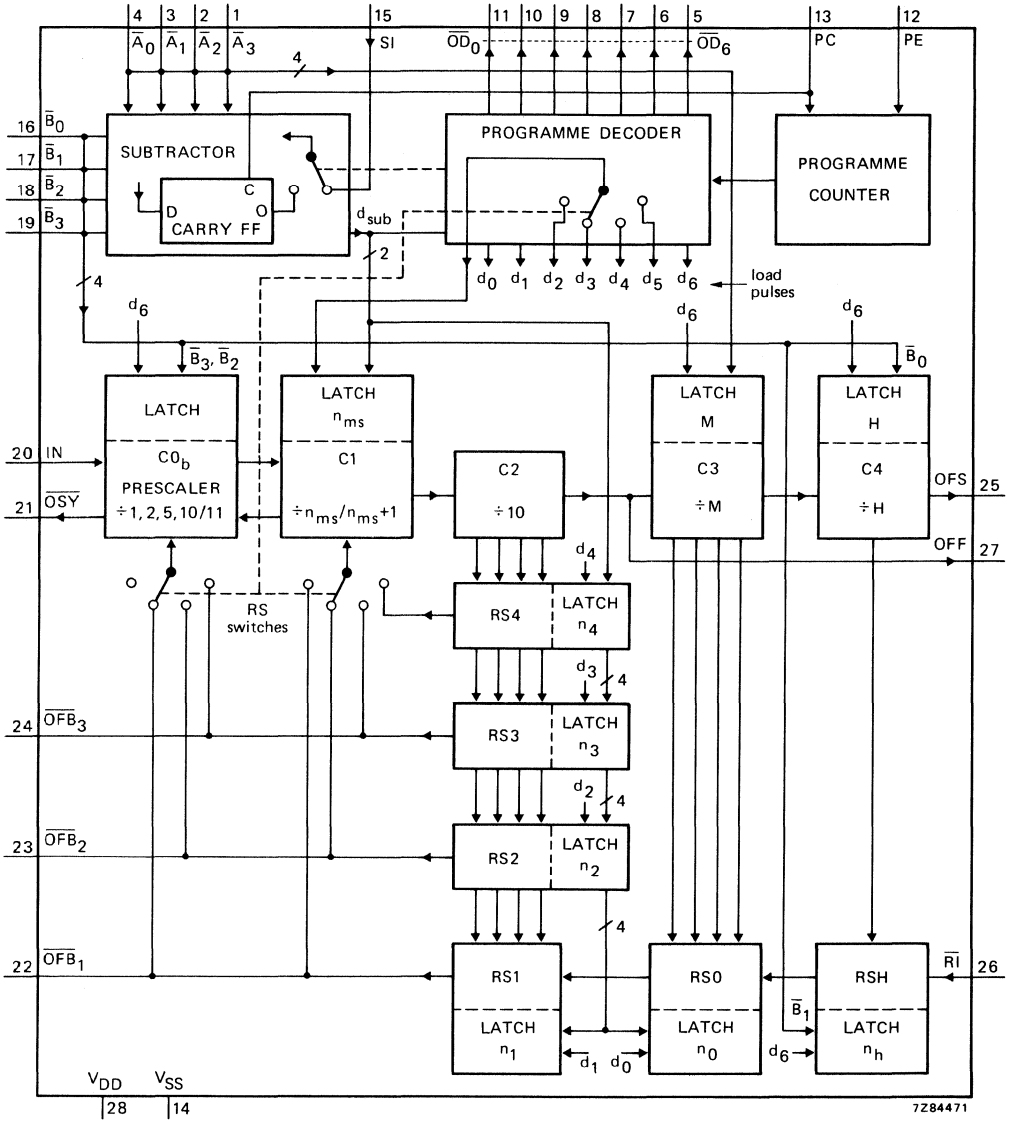


Fig. 2 Block diagram.

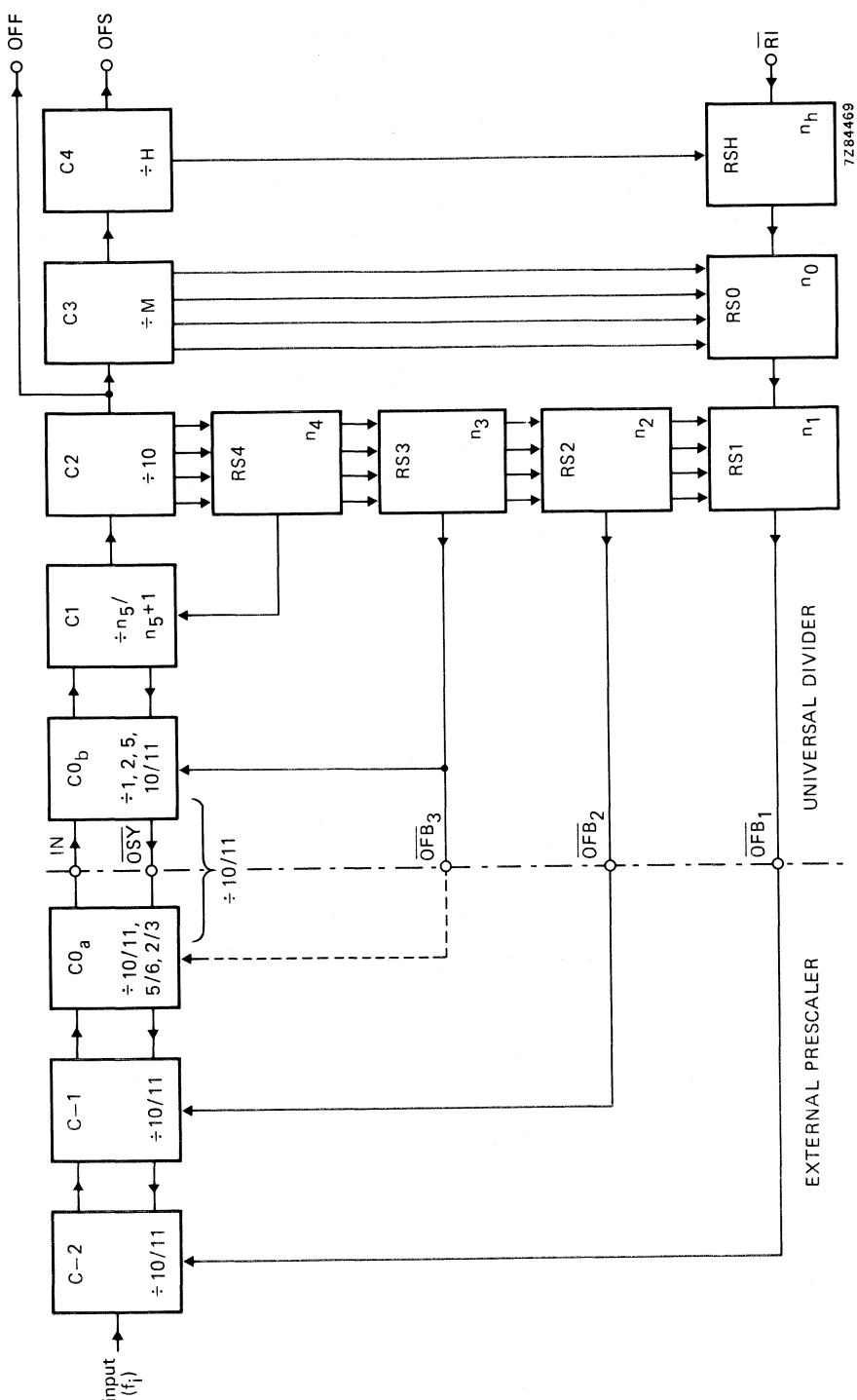


Fig. 3 The HEF4751V U.D. used in a system with 3 (fast) prescalers.
$1 \leqslant M \leqslant 16$; $1 \leqslant H \leqslant 2$; $n_5 > 0$; $f_i/f_{OFS} = \{(n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1)\, M + n_0\}\, H + n_h$.

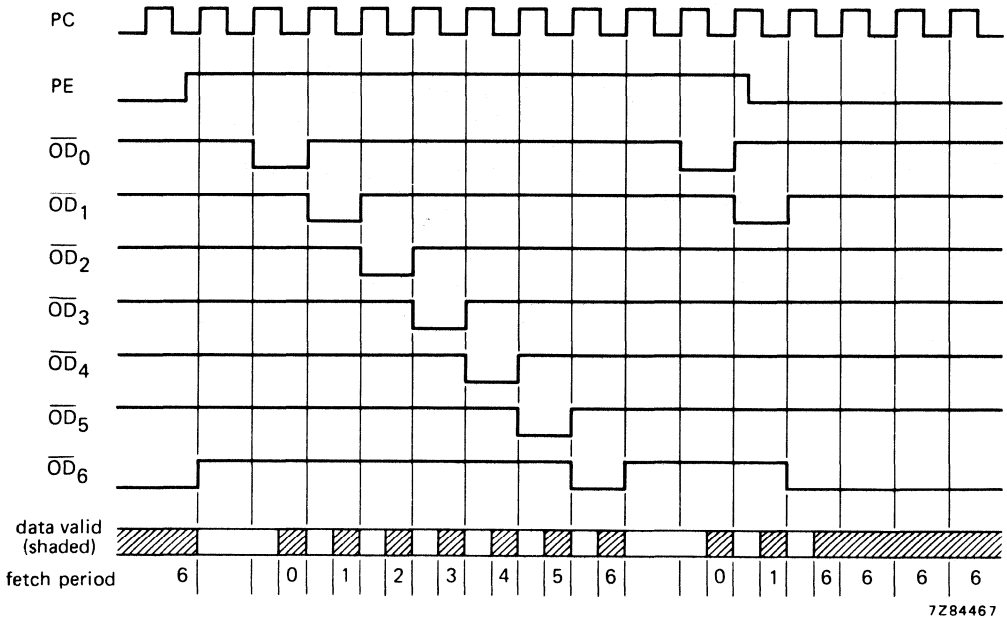


Fig. 4 Timing diagram showing programme data inputs.

Allocation of data input

fetch period	inputs								
	$\overline{A}_3$	$\overline{A}_2$	$\overline{A}_1$	$\overline{A}_0$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$	$\overline{B}_0$	SI
0	n_{0A}				n_{0B}				b_{in}
1	n_{1A}				n_{1B}				X
2	n_{2A}				n_{2B}				X
3	n_{3A}				n_{3B}				X
4	n_{4A}				n_{4B}				X
5	n_{5A}				n_{5B}				X
6	M				$C0_b$ control		½ channel control		X

Allocation of data input $\overline{B}_3$ to $\overline{B}_0$ during fetch period 6

$\overline{B}_3$	$\overline{B}_2$	$C0_b$ division ratio
L	L	1
L	H	2
H	L	5
H	H	10/11

$\overline{B}_1$	$\overline{B}_0$	½ channel configuration
L	L	H = 1
L	H	H = 2; n_h = 0
H	H	H = 2; n_h = 1
H	L	test state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

PROGRAMME DATA INPUT (see also Figs 3 and 4)

The programming process is timed and controlled by input PC and PE. When the programme enable (PE) input is HIGH, the positive edges of the programme clock (PC) signal step through the internal programme counter in a sequence of 8 states. Seven states define fetch periods, each indicated by a LOW signal at one of the corresponding data address outputs ($\overline{OD}_0$ to $\overline{OD}_6$). These data address signals may be used to address the external programme source. The data fetched from the programme source is applied to inputs $\overline{A}_0$ to $\overline{A}_3$ and $\overline{B}_0$ to $\overline{B}_3$. When PC is LOW in a fetch period an internal load pulse is generated, the data is valid during this time and has to be stable. When PE is LOW, the programming cyclus is interrupted on the first positive edge of PC. On the next negative edge at input PC fetch period 6 is entered. Data may enter asynchronously in fetch period 6.

Ten blocks in the U.D. need programme input signals (see Fig. 2). Four of these ($C0_b$, C3, C4 and RSH) are concerned with the configuration of the U.D. and are programmed in fetch period 6. The remaining blocks (RS0 to RS4 and C1) are programmed with number P, consisting of six internal digits n_0 to n_5.

$P = (n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1) \cdot M + n_0$

These digits are formed by a substractor from two external numbers A and B and a borrow-in (b_{in}).

$P = A - B - b_{in}$ or if this result is negative; $P = A - B - b_{in} + M \cdot 10^5$.

The numbers A and B, each consisting of six four bit digits n_{0A} to n_{5A} and n_{0B} to n_{5B}, are applied in fetch period 0 to 5 to the inputs $\overline{A}_0$ to $\overline{A}_3$ (data A) and $\overline{B}_0$ to $\overline{B}_3$ (data B) in binary coded negative logic.

$A = (n_{5A} \cdot 10^4 + n_{4A} \cdot 10^3 + n_{3A} \cdot 10^2 + n_{2A} \cdot 10 + n_{1A}) \cdot M + n_{0A}$.

$B = (n_{5B} \cdot 10^4 + n_{4B} \cdot 10^3 + n_{3B} \cdot 10^2 + n_{2B} \cdot 10 + n_{1B}) \cdot M + n_{0B}$.

Borrow-in (b_{in}) is applied via input SI in fetch period 0 (SI = HIGH: borrow, SI = LOW: no borrow).

Counter C1 is automatically programmed with the most significant non-zero digit (n_{ms}) from the internal digits n_5 to n_2 of number P. The counter chain C – 2 to C1 (see Fig. 3) is fully programmable by the use of pulse rate feedback.

Rate feedback is generated by the rate selectors RS4 to RS0 and RSH, which are programmed with digits n_4 to n_0 and n_h respectively. In fetch period 6 the fractional counter C3, half channel counter C4 and $C0_b$ are programmed and configured via data B inputs. Counter C3 is programmed in fetch period 6 via data A inputs in negative logic (except all HIGH is understood as: M = 16). The counter C0 is a side steppable 10/11 counter composed of an internal part $C0_b$ and an external part $C0_a$. $C0_b$ is configured via $\overline{B}_3$ and $\overline{B}_2$ to a division ratio of 1 or 2 or 5 or 10/11; $C0_a$ must have the complementary ratio 10/11 or 5/6 or 2/3 or 1 respectively. In the latter case $C0_b$ comprises the whole C0 counter with internal feedback, $C0_a$ is then not required.

The half channel counter C4 is enabled with $\overline{B}_0$ = HIGH and disabled with $\overline{B}_0$ = LOW. With C4 enabled, a half channel offset can be programmed with input $\overline{B}_1$ = HIGH, and no offset with $\overline{B}_1$ = LOW.

FEEDBACK TO PRESCALERS (see also Figs 5 and 6)

The counters C1, C0, C–1 and C–2 are side-steppable counters, i.e. its division ratio may be increased by one, by applying a pulse to a control terminal for the duration of one division cycle. Counter C2 has 10 states, which are accessible as timing signals for the rate selectors RS1 to RS4. A rate selector, programmed with n (n_1 to n_4 in the U.D.) generates n of 10 basic timing periods an active signal. Since $n \leqslant 9$, 1 of 10 periods is always non-active. In this period RS1 transfers the output of rate selector RS0, which is timed by counter C3 and programmed with n_0. Similarly, RS0 transfers RSH output during one period of C3. Rate selector RSH is timed by C4 and programmed with n_h. In one of the two states of C4, if enabled, or always, if C4 is disabled, RSH transfers the LOW active signal at input $\overline{RI}$ to RS0. If $\overline{RI}$ is not used it must be connected to HIGH. The feedback output signals of RS1, RS2 and RS3 are externally available as active LOW signals at outputs $\overline{OFB}_1$, $\overline{OFB}_2$ and $\overline{OFB}_3$.

Output $\overline{OFB}_1$ is intended for the prescaler at the highest frequency (if present), $\overline{OFB}_2$ for the next (if present) and $\overline{OFB}_3$ for the lowest frequency prescaler (if present). A prescaler needs a feedback signal, which is timed on one of its own division cycles in a basic timing period. The timing signal at $\overline{OSY}$ is LOW during the last U.D. input period of a basic timing period and is suitable for timing of the feedback for the last external prescaler. The synchronization signal for a preceding prescaler is the OR-function of the sync. input and sync. output of the following prescaler (all sync. signals active LOW).

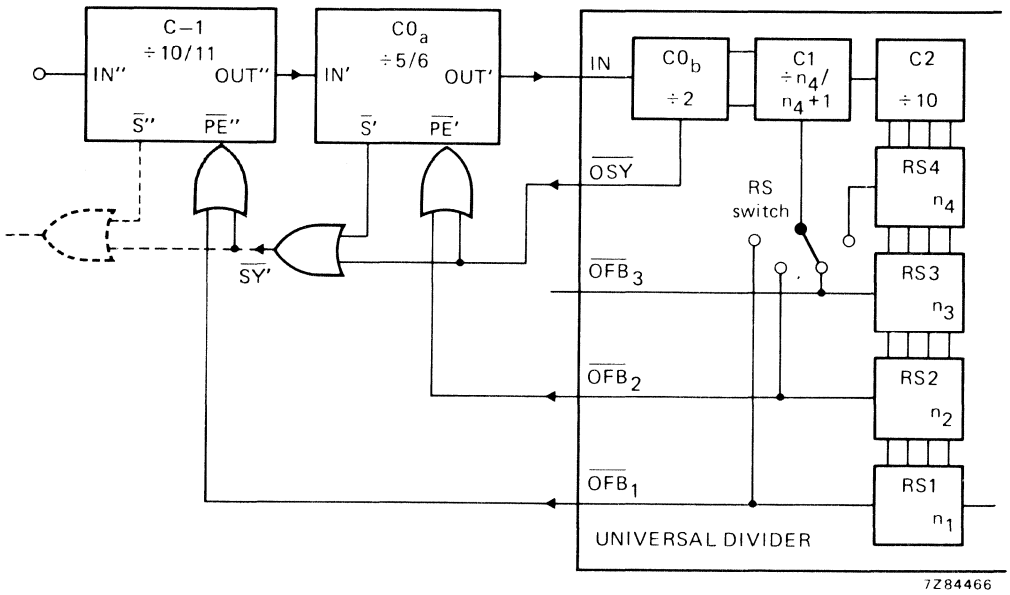


Fig. 5 Block diagram showing feedback to prescalers.

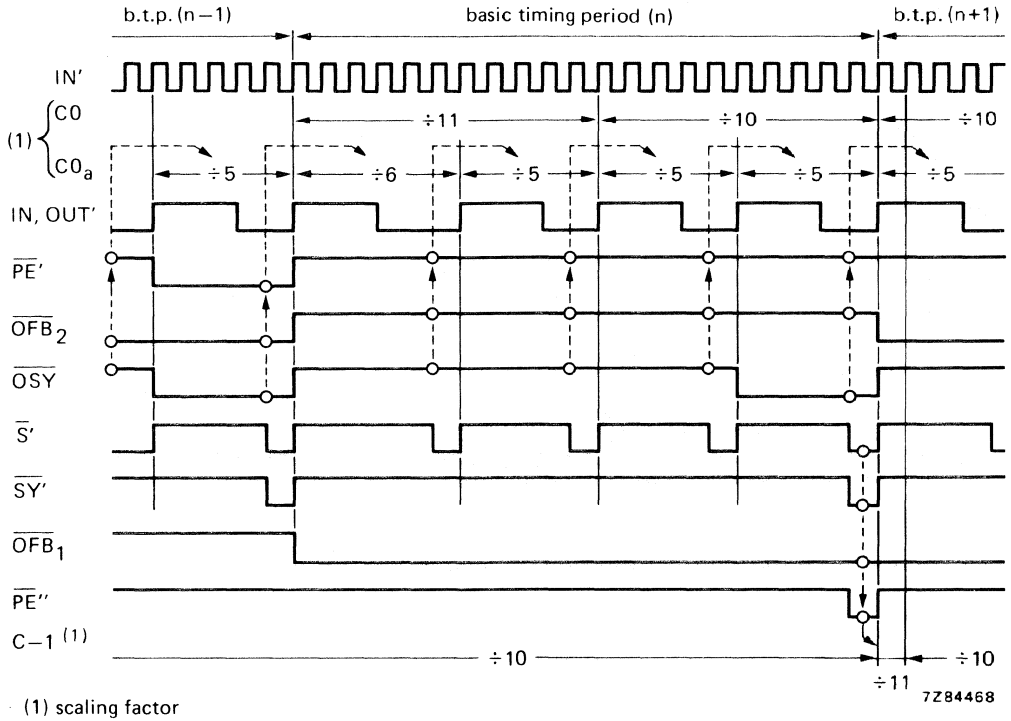


Fig. 6 Timing diagram showing signals occurring in Fig. 5.

CASCADING OF U.D.s (see also Fig. 8)

A U.D. is programmed into the 'slave' mode by the programme input data: $n_{2A} = 11$, $n_{2B} = 10$, $n_{3A} = n_{4A} = n_{3B} = n_{4B} = n_{5B} = 0$. A U.D. operating in the slave mode performs the function of two extra programmable stages C2' and C3' to a 'master' (not slave) mode operating U.D. More slave U.D.s may be used, every slave adding two lower significant digits to the system.

Output $\overline{OFB}_3$ is converted to the borrow output of the programme data subtractor, which is valid after fetch period 5. Input SI is the borrow input (both in master and in slave mode), which has to be valid in fetch period 0. Input SI has to be connected to output $\overline{OFB}_3$ of a following slave, if not present, to LOW. For proper transfer of the borrow from a lower to a higher significant U.D. subtractor, the U.D.s have to be programmed sequentially in order of significance or synchronously if the programme is repeated at least the number of U.D.s in the system.

Rate input $\overline{RI}$ and output OFS must be connected to rate output $\overline{OFB}_1$ and the input IN of the next slave U.D. The combination thus formed retains the full programmability and features of one U.D.

OUTPUT (see also Fig. 7)

The normal output of the U.D. is the slow output OFS, which consists of evenly spaced LOW pulses. This output is intended for accurate phase comparison. If a better frequency acquisition time is required, the fast output OFF can be used. The output frequency on OFF is a factor M · H higher than the frequency on OFS. However, phase jitter of maximum ±1 system input period occurs at OFF, since the division ratio of the counters preceding OFF are varied by slow feedback pulse trains from rate selectors following OFF.

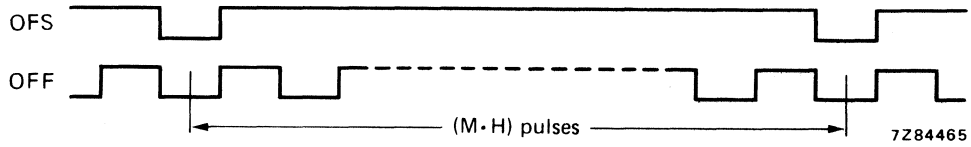


Fig. 7 Timing diagram showing output pulses.

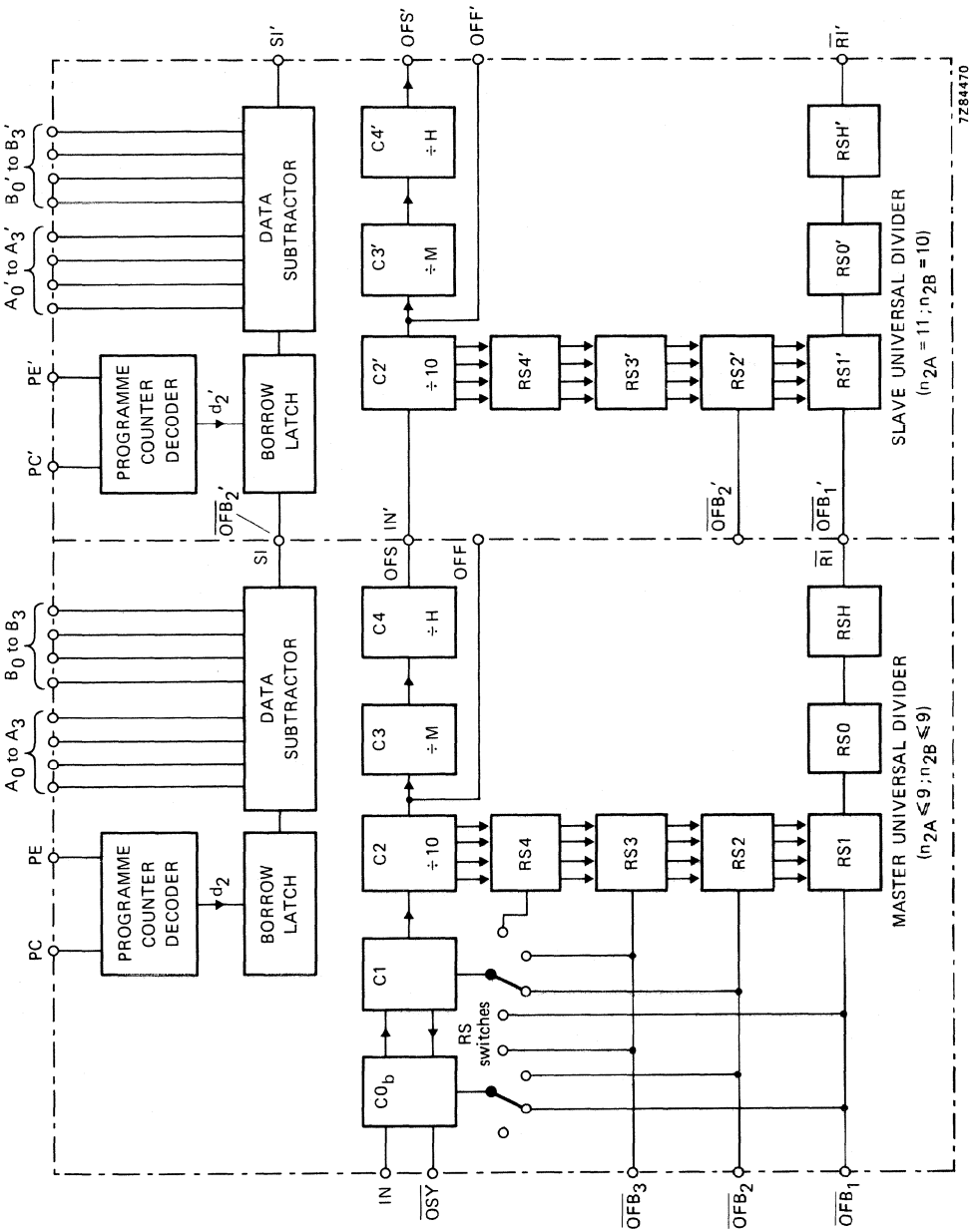


Fig. 8 Block diagram showing cascading of U.Ds.

D.C. CHARACTERISTICS V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output (sink) current LOW	4,75		0,4	I_{OL}	1,6		1,4		1,1		mA
	5		0,4		1,7		1,5		1,2		mA
	10		0,5		2,9		2,7		2,2		mA
Output (source) current HIGH	5	4,6		$-I_{OH}$	1,0		0,85		0,55		mA
	5	2,5			3,0		2,5		1,7		mA
	10	9,5			3,0		2,5		1,7		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	
Propagation delay IN → $\overline{OSY}$ HIGH to LOW	5	t_{PHL}		135	270	ns	C_L = 10 pF
	10			45	90	ns	
Output transition times							
HIGH to LOW	5	t_{THL}		30	60	ns	C_L = 50 pF
	10			12	25	ns	
LOW to HIGH	5	t_{TLH}		45	90	ns	C_L = 50 pF
	10			20	40	ns	
Maximum input frequency; IN	5	f_{max}	4	8		MHz	δ = 50%; $C0_b$ ratio > 1
	10		12	24		MHz	
Maximum input frequency; IN	5	f_{max}	2	4		MHz	δ = 50%; $C0_b$ ratio = 1
	10		6	12		MHz	
Maximum input frequency; PC	5	f_{max}	0,15	0,3		MHz	
	10		0,5	1,0		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. MOTOR CONTROL CIRCUIT

The HEF4752V is a circuit for a.c. motor speed control utilizing LOCMOS technology. The circuit synthesizes three 120° out of phase signals, of which the average voltage varies sinusoidally with time in the frequency range 0 to 200 Hz. The method employed is based upon the pulse width modulation principle, in order to achieve a sufficient accuracy of the output voltages over the whole frequency range. A pure digital waveform generation is used.

All outputs are of the push-pull type. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

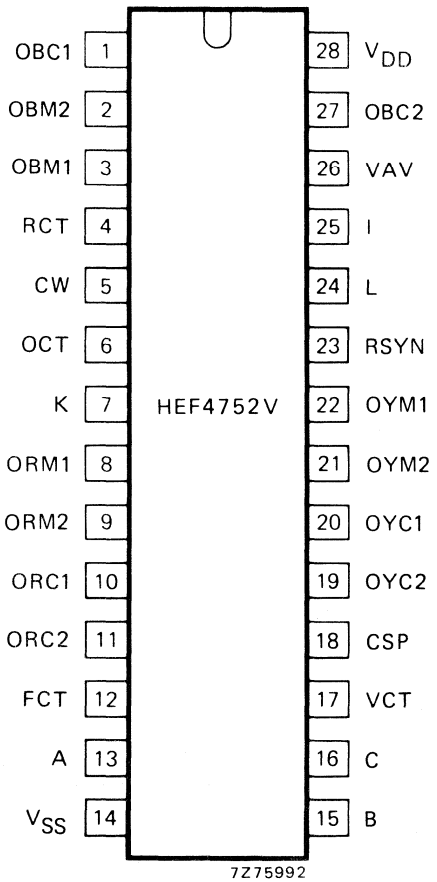


Fig. 1 Pinning diagram.

PINNING

Inputs; group I

24 = L	data	
25 = I	data	
7 = K	data	
5 = CW	data	
13 = A	data	
15 = B	data	
16 = C	data	

Inputs; group II

12 = FCT	frequency clock
17 = VCT	voltage clock
4 = RCT	reference clock
6 = OCT	output delay clock

Outputs; group I

23 = RSYN	R-phase synchronization
26 = VAV	average voltage
18 = CSP	current sampling pulses

Outputs; group II

8 = ORM1	R-phase main
9 = ORM2	R-phase main
10 = ORC1	R-phase commutation
11 = ORC2	R-phase commutation
22 = OYM1	Y-phase main
21 = OYM2	Y-phase main
20 = OYC1	Y-phase commutation
19 = OYC2	Y-phase commutation
3 = OBM1	B-phase main
2 = OBM2	B-phase main
1 = OBC1	B-phase commutation
27 = OBC2	B-phase commutation

SUPPLY VOLTAGE

	rating	recommended operating
HEF4752V	−0,5 to 18	4,5 to 12,5 V

HEF4752VP : 28-lead DIL; plastic (SOT-117).
HEF4752VD: 28-lead DIL; ceramic (cerdip) (SOT-135A).

FAMILY DATA see Family Specifications

D.C. CHARACTERISTICS V_{SS} = 0 V

parameter	V_{DD} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	unit	conditions
Quiescent device current	5	I_{DD}	–	50	–	50	–	375	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}
	10		–	100	–	100	–	750	μA	
Input leakage current	10	$\pm I_{IN}$	–	–	–	0,3	–	1	μA	V_I = 0 or 10 V
Input voltage HIGH	5	V_{IH}	3,5	–	3,5	–	3,5	–	V	inputs: group I
	10		7,0	–	7,0	–	7,0	–	V	
Input voltage LOW	5	V_{IL}	–	1,5	–	1,5	–	1,5	V	inputs: group I
	10		–	3,0	–	3,0	–	3,0	V	
Output voltage HIGH	5	V_{OH}	4,95	–	4,95	–	4,95	–	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1\ \mu A$
	10		9,95	–	9,95	–	9,95	–	V	
Output voltage LOW	5	V_{OL}	–	0,05	–	0,05	–	0,05	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1\ \mu A$
	10		–	0,05	–	0,05	–	0,05	V	
Input tripping level; input voltage increasing	5	V_{ti}	1,5	4,0	1,5	4,0	1,5	4,0	V	inputs: group II
	10		3,0	8,0	3,0	8,0	3,0	8,0	V	
Input tripping level; input voltage decreasing	5	V_{td}	1,0	3,5	1,0	3,5	1,0	3,5	V	inputs: group II
	10		2,0	7,0	2,0	7,0	2,0	7,0	V	
Output current LOW	5	I_{OL}	0,45	–	0,38	–	0,3	–	mA	V_{OL} = 0,4 V; outputs: groups I and II
	10		1,4	–	1,17	–	0,9	–	mA	V_{OL} = 0,5 V
Output current HIGH	5	$-I_{OH}$	0,3	–	0,25	–	0,2	–	mA	V_{OH} = 4,6 V; outputs: group I
	10		0,9	–	0,75	–	0,6	–	mA	V_{OH} = 9,5 V
Output current HIGH	5	$-I_{OH}$	0,9	–	0,75	–	0,6	–	mA	V_{OH} = 2,5 V; outputs: group I
Output current HIGH	5	$-I_{OH}$	0,6	–	0,5	–	0,4	–	mA	V_{OH} = 4,6 V; outputs: group II
	10		1,8	–	1,5	–	1,2	–	mA	V_{OH} = 9,5 V
Output current HIGH	5	$-I_{OH}$	1,8	–	1,5	–	1,2	–	mA	V_{OH} = 2,5 V; outputs: group II
Total supply current	10	I_{tot}	–	–	typ. 2		–	–	mA	$I_{OL} = I_{OH} = 0$; frequency applied to inputs; FCT = 700 kHz; VCT = 400 kHz; RCT = 400 kHz

APPLICATION INFORMATION

Figure 2 shows the functional block diagram of a 3-phase a.c. motor speed control system using a thyristorized inverter with variable frequency output. The inverter control signals are generated by the HEF4752V (PWM-IC). A special feature of the PWM (Pulse-Width Modulation) - IC is here, that the motor is supplied by sinnoidally modulated pulses, hence the resulting motor current will approach a sine-wave with a minimum on higher harmonics. In this way, an optimum speed drive with high performance is obtained.
Furthermore, the HEF4752V contains all logic circuitry required for this special waveform generation, so that the amount of control circuit components is reduced considerable. The speed drive system in Fig. 2 is controlled by the analogue control section.
The FCT and VCT clock pulse oscillators are driven in such a way, that a fast response speed control of the a.c. motor is obtained, depending on: the reference values for speed; motor voltage; motor current (Limited by the measured motor current via DCCT - d.c. current transformer -); the increasing value of V_{Cb} during braking action.

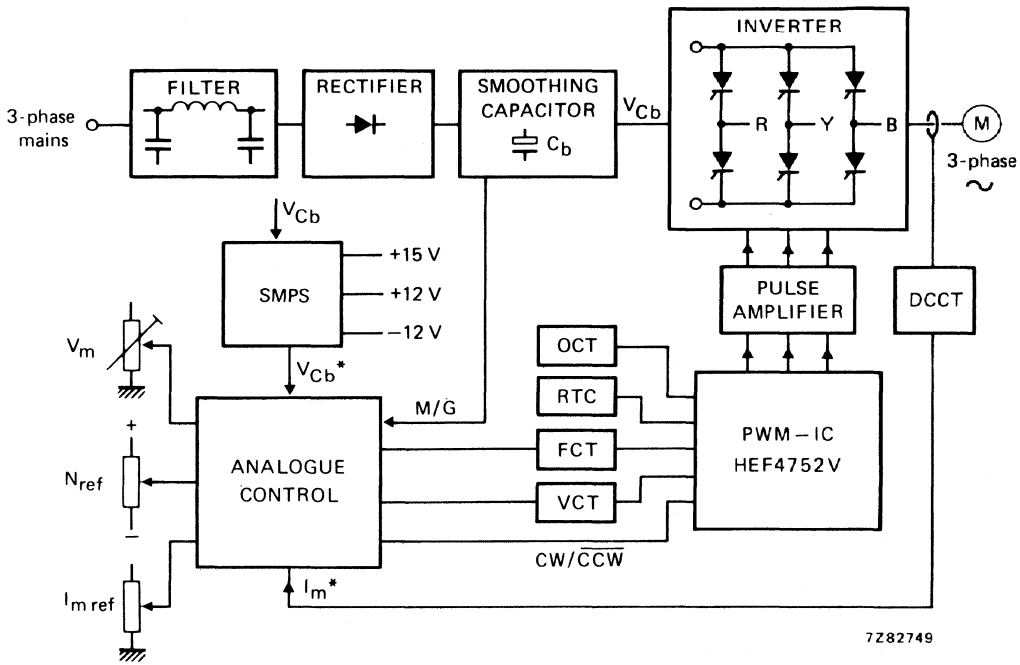


Fig. 2 PWM motor speed control system using HEF4752V.

MORE APPLICATION INFORMATION SUPPLIED ON REQUEST

UNIVERSAL TIMER MODULE

The HEF4753B is a universal timer module for counting and dividing as well as for event-recognition and manipulation of input sequences.
The following functions are included: synchronization and edge-detection of the input signal, programmable counter, clock divider with different lengths, operating mode decoder, control logic and output multiplexer.
Depending on the operating mode and the application, the circuit works as a presettable 8-bit counter with transient-pulse suppression, pulse duration selector divider, counter, positive or negative edge delaying module or low-frequency control circuit.
All manipulation possibilities depend on a time scaling, which is adjustable by the 8-bit programmable counter and the system clock. The system clock can be divided internally by 1, 16, 256 or 4096 as input clock for the counter. In all cases the manipulated input sequence appears at the only output OUT.

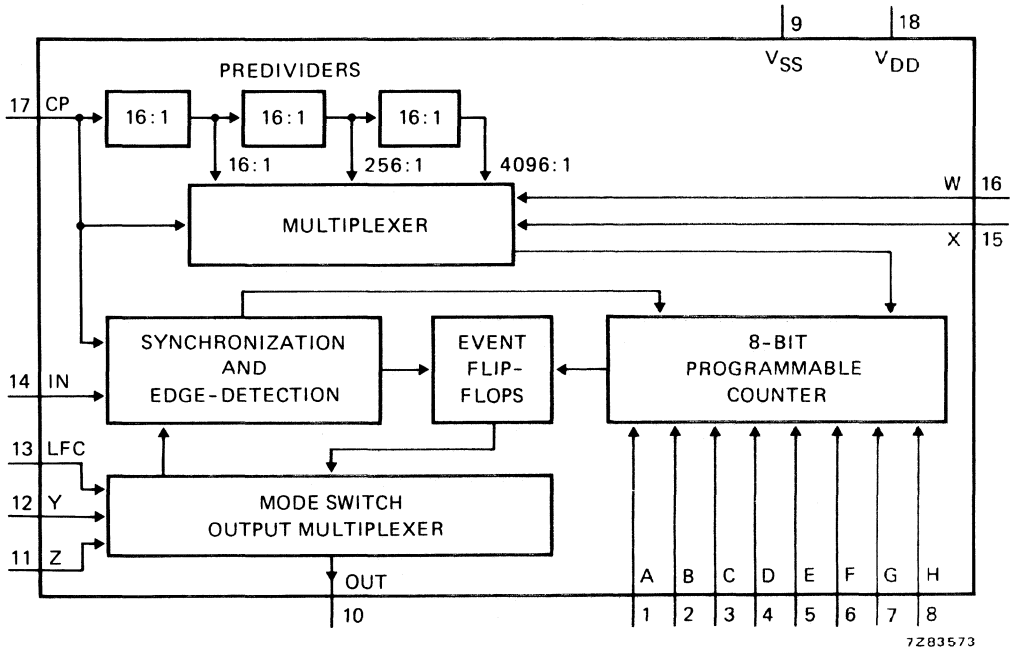
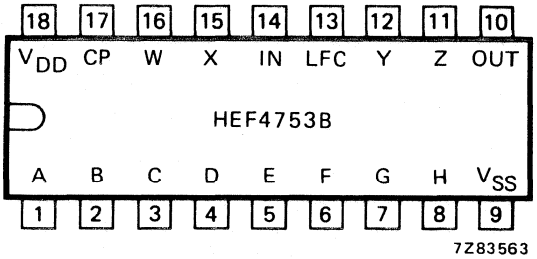


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications



HEF4753BP: 18-lead DIL; plastic (SOT-102).
HEF4753BD: 18-lead DIL; ceramic (cerdip) (SOT-133B).

Fig. 2 Pinning diagram.

FUNCTION TABLES

inputs			operating mode
LFC	Y	Z	
L	L	H	counter
L	H	L	divider
H	H	L	delayed LOW to HIGH edge
H	L	H	delayed HIGH to LOW edge
H	H	H	transient pulse suppression
L	H	H	frequency recognition
LFC	L	L	digital pulse duration selector

H = HIGH state (the more positive voltage).
L = LOW state (the less positive voltage).

Programmable 8-bit counter *

inputs active LOW	value
A	1
B	2
C	4
D	8
E	16
F	32
G	64
H	128

12-bit predivider

W	X	clock for programmable counter CP/X
L	L	X = 1
L	H	X = 16
H	L	X = 256
H	H	X = 4096

* All inputs A to H HIGH is not allowed.

FUNCTIONAL DESCRIPTION

Clock divider and decoder

The clock signal at input CP is, at its original frequency, the system clock, but it also drives the programmable counter. The counter input frequency can be predivided by the factors 1/16, 1/256 and 1/4096, depending on the logic state of inputs W and X (according to the function tables above).

8-bit programmable counter

The 8 inputs A to H are the set inputs of the 8 counter flip-flops. The setting is triggered by an edge of the input signal (at input IN) depending on of the chosen mode.

Event flip-flops, synchronization and edge-detection

The event flip-flops are used to recognize the positive and/or negative edge of the input signal at IN. Parts of the flip-flops are used together with the programmable 8-bit counter as a retriggerable mono-flop, which defines the time scaling for event recognition.
The input IN is synchronized by the clock signal CP.

Mode switch and output multiplexer

This function switches the chosen output to the output (OUT) and gives the mode of which the edge at input IN has to be detected. The inputs Z, Y and LFC give 7 modes +1, that means in mode 'Digital Filter' the input LFC can be HIGH or LOW.

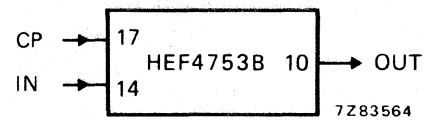
OPERATING MODES

The circuit has 6 operating modes which are activated by the logic state of inputs LFC, Y and Z. An extra mode is possible by using two circuits which are connected such so they function as a digital band-filter.

1. Counter mode (LFC = LOW; Y = LOW; Z = HIGH)

In this mode the output OUT should be connected to input IN. If not, only one counter cycle starts after a transition at input IN (see Fig. 3 and note 1).

A	B	C	D	E	F	G	H	W	X	LFC	Y	Z
H	H	L	H	H	H	H	H	L	L	L	L	H



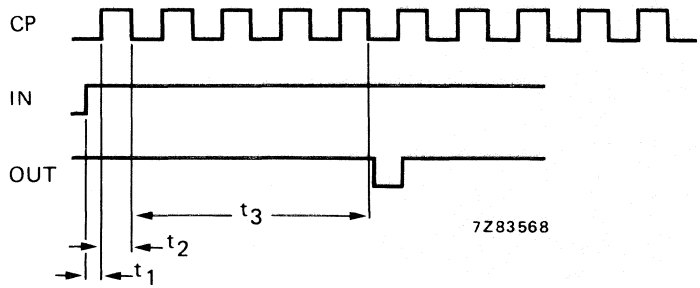


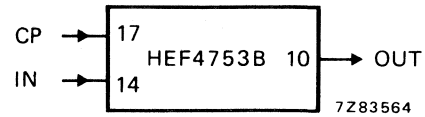
Fig. 3 Timing diagram for counter mode; t_1 = delay until set of 8-bit counter; t_2 = delay to set 8-bit counter; t_3 = predefined delay by programming.

OPERATING MODES (continued)

2. Divider mode (LFC = LOW; Y = HIGH; Z = LOW)

In this mode the output OUT should be connected to input IN. If not, only one counter cycle starts after a transition at input IN (see Fig. 4 and note 1).

A	B	C	D	E	F	G	H	W	X	LFC	Y	Z
L	L	H	H	H	H	H	H	L	L	L	H	L



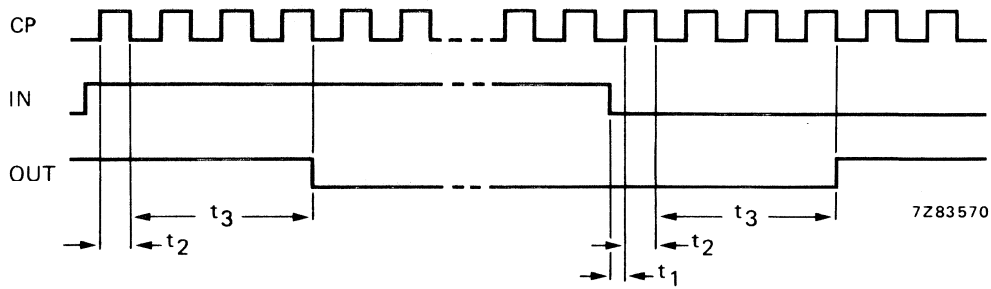
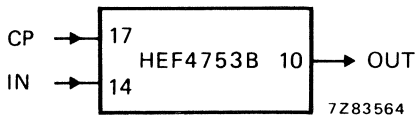


Fig. 4 Timing diagram for divider mode; t_1 = delay until set of 8-bit counter; t_2, t_3 see Fig. 3.

3. Delayed LOW to HIGH edge mode; see note 2 (LFC = HIGH; Y = HIGH; Z = LOW)

A	B	C	D	E	F	G	H	W	X	LFC	Y	Z
H	L	H	H	H	H	H	H	L	L	H	H	L



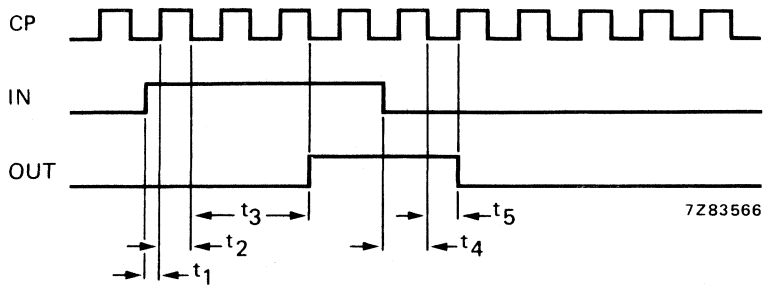


Fig. 5 Timing diagram for delayed LOW to HIGH edge mode; t_1 = delay until set of 8-bit counter; t_2 = delay to set 8-bit counter; t_3 = predefined delay by programming; t_4 = delay until next negative clock edge; t_5 = delay until next positive clock edge.

4. Delayed HIGH to LOW edge mode; see note 2 (LFC = HIGH; Y = LOW; Z = HIGH)

A	B	C	D	E	F	G	H	W	X	LFC	Y	Z
H	L	H	H	H	H	H	H	L	L	H	L	H

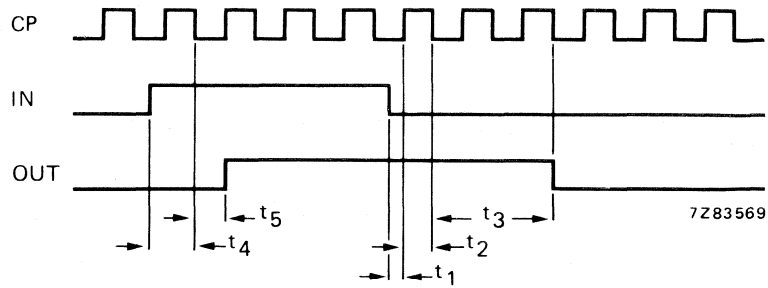
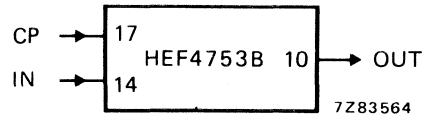


Fig. 6 Timing diagram for delayed HIGH to LOW edge mode; for t_1 to t_5 see Fig. 5.

5. Transient pulse suppression and pulse delaying mode; see note 2 (LFC = Y = Z = HIGH)

In this mode the circuit is working as a digital low-pass filter. An undisturbed pulse will only be delayed (see Fig. 7).

A	B	C	D	E	F	G	H	W	X	LFC	Y	Z
L	L	H	H	H	H	H	H	L	L	H	H	H



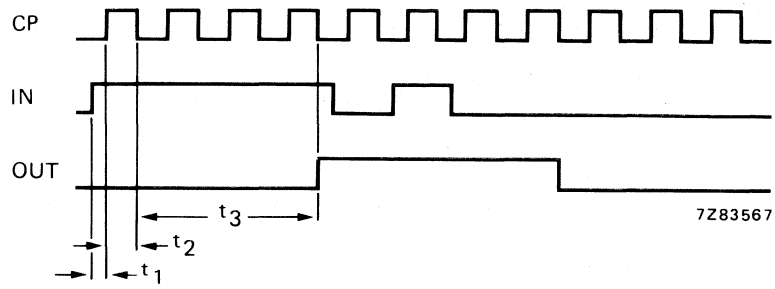


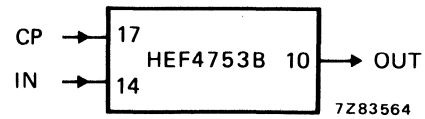
Fig. 7 Timing diagram for transient pulse suppression and pulse delaying mode; for t_1, t_2 and t_3 see Fig. 5.

OPERATING MODES (continued)

6. Frequency recognition mode (LFC = LOW; Y = HIGH; Z = HIGH)

The incoming signal must be symmetrical within the limits as given by the specified delay time in note 2, to achieve lower or higher frequency detection (see Fig. 8).

A	B	C	D	E	F	G	H	W	X	LFC	Y	Z
L	H	L	H	H	H	H	H	L	L	L	H	H



Minimum dividing number is 3.

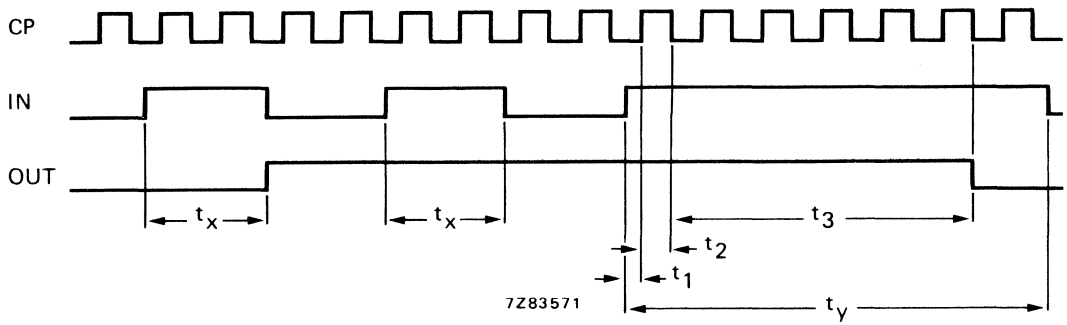


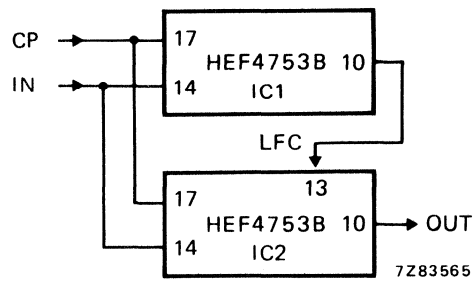
Fig. 8 Timing diagram for frequency recognition mode; t_x = time shorter than t_3 (OUT = H); t_y = time greater than t_3 (OUT = L); for t_1, t_2 and t_3 see Fig. 5.

7. Digital pulse duration selector mode (Y = Z = LOW)

This mode is a combination of two circuits, both used for frequency recognition. Both circuits are driven by the same clock and same input signal, but programmed for different frequencies. The LFC input of the low-frequency circuit is set to logic LOW, the output is connected to the LFC input of the high-frequency circuit, whose output (OUT) is the 'filter' output. The delay time depends on the same facts as given in note 2. For timing diagram see Fig. 9.

A	B	C	D	E	F	G	H	W	X	LFC	Y	Z	
L	L	L	H	H	H	H	H	L	L	L	H	H	IC1
L	L	H	H	H	H	H	H	L	L	OUT (IC1)	L	L	IC2

Minimum dividing number is 3.



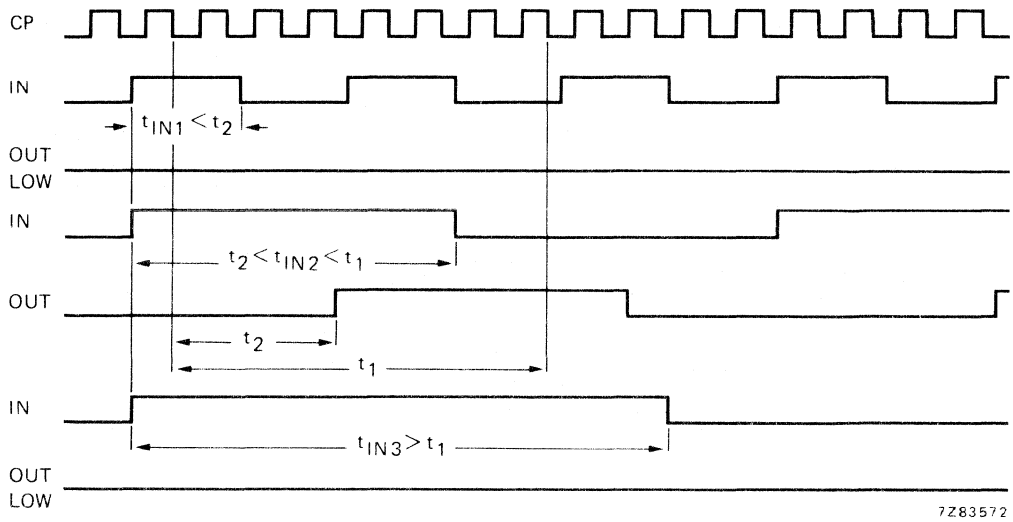


Fig. 9 Timing diagram for digital pulse duration selector mode; t_{IN1}, t_{IN2} and t_{IN3} are the IN input pulse durations; t_1 = predefined delay by programming IC1; t_2 = predefined delay by programming IC2.

Notes to operating modes

1. The number of clocks for one cycle in the counter and divider mode is:
   a. Contents of programmable counter plus one if X = W = LOW.
   b. Contents of programmable counter multiplied by 16, 256 or 4096 if X and/or W = HIGH.
2. The delay in the modes 3, 4, 6 and 7, and the delay which is identical to the maximum duration of the transient pulse in mode 5 depend on the optional divided clock frequency, the input conditions of the 8-bit presetable counter and in addition, different times of propagation delays, jitter and maximum one half of a clock frequency period.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output (sink)	4,75		0,4		2,7	–	2,3	–	1,8	–	mA
current LOW	10		0,5	I_{OL}	9,5	–	8,0	–	6,3	–	mA
(pin 10)	15		1,5		24,0	–	20,0	–	16,0	–	mA
Output (source)	5	4,6			0,6	–	0,5	–	0,4	–	mA
current HIGH	10	9,5		$-I_{OH}$	1,8	–	1,5	–	1,2	–	mA
(pin 10)	15	13,5			6,0	–	5,0	–	4,0	–	mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays	5			420	850	ns	
CP ⟶ OUT	10	t_{PHL}		180	360	ns	
HIGH to LOW	15			120	250	ns	
	5			450	900	ns	
LOW to HIGH	10	t_{PLH}		200	400	ns	
	15			140	280	ns	
Output transition	5			30	60	ns	
times	10	t_{THL}		15	30	ns	
HIGH to LOW	15			10	20	ns	
	5			60	120	ns	
LOW to HIGH	10	t_{TLH}		30	60	ns	
	15			20	40	ns	
Input rise and	5						
fall times	10	t_r, t_f	no limit				
pins 13, 14, 17	15						
Maximum clock	5		3	6		MHz	
pulse frequency	10	f_{max}	7	14		MHz	
pin 17; δ = 50%	15		8	17		MHz	

	V_{DD} V	typical formula for P (μW)	where
			f_i = input freq. (MHz)
			f_o = output freq. (MHz)
Dynamic power	5	$1\,800\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
dissipation per	10	$8\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	$\Sigma\ (f_o C_L)$ = sum of outputs
package (P)	15	$19\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	V_{DD} = supply voltage (V)

18-ELEMENT BAR GRAPH LCD DRIVER

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_C) in a pointer or thermometer mode.

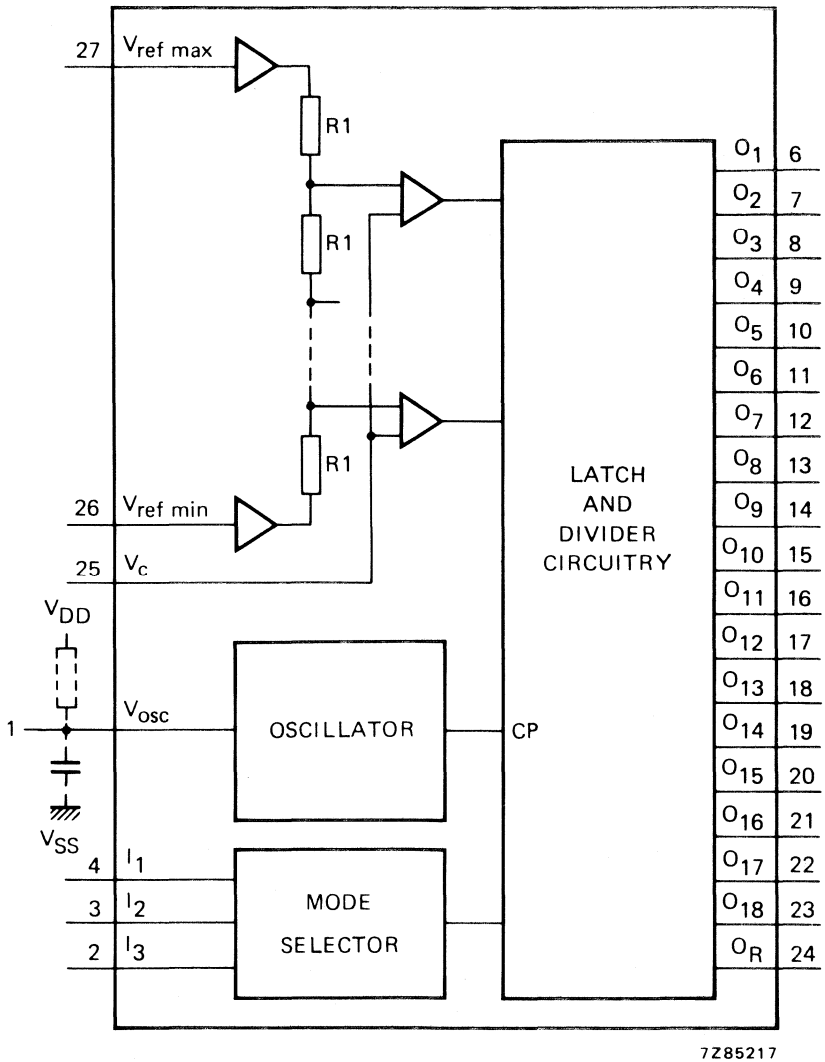


Fig. 1 Functional diagram.

FAMILY DATA see Family Specifications

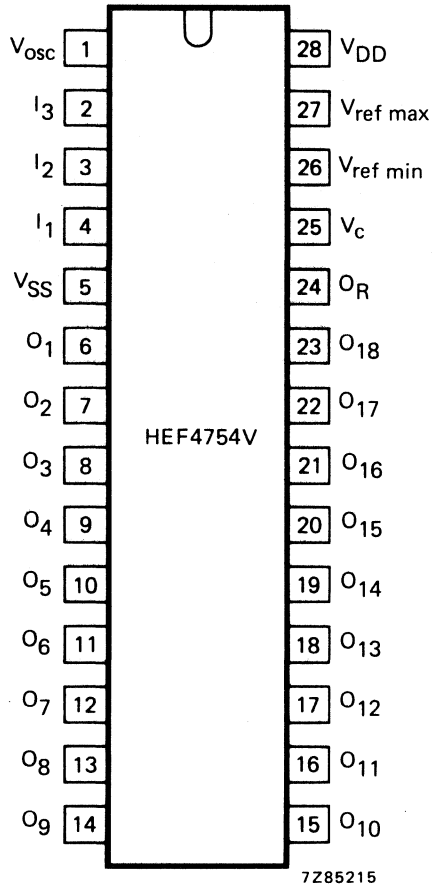


Fig. 2 Pinning diagram.

PINNING

V_{osc}	oscillator terminal
V_c	control voltage input
$V_{ref\ min}$, $V_{ref\ max}$	reference voltage inputs
I_1	thermometer/pointer (choice select input)
I_2	peak value; reset/9 or 18 bars (choice select input)
I_3	reset; repetitively reset (choice select input)
O_1 to O_{18}	bar outputs
O_R	back plate output

HEF4754VP : 28-lead DIL; plastic (SOT-117).
HEF4754VD: 28-lead DIL; ceramic (cerdip) SOT-135A).
HEF4754VT : 28-lead mini-pack; plastic (SO-28; SOT-136A).

FUNCTION TABLE

I_1	I_2	I_3	mode
L	L	X	pointer; 18 bars
L	H	X	pointer; 9 bars
H	L	X	thermometer; no peak value
H	H	L	thermometer; peak value, repetitively reset
H	H	H	thermometer; peak value, manually reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

GENERAL DESCRIPTION

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode. The first bar lights up when V_c is smaller than $V_{T(bar)2}$ (see equation [3] below).

In the pointer mode, the circuit can drive 9 or 18 bars; in the thermometer mode, the circuit also drives the peak value indication. This can be reset or repetitively reset, after 1,5 to 2 seconds.

The circuit has analogue and digital parts. The analogue part consists of 17 comparators, with their non-inverting inputs connected together and coupled to the control input V_c. The inverting inputs of the comparators are connected in succession to the nodes of an 18-part resistor divider. The distance between the switching levels of the comparators is defined by the voltage difference across this divider. The extremities of the resistor divider are coupled via high-input amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The digital part has one reference output (O_R) to drive the back plate, and 18 outputs (O_1 to O_{18}) to drive each bar. Three latches and some gates are incorporated for each bar output. An on-chip oscillator (1024 Hz) with external R and C drives the circuit. The outputs are driven at 64 Hz. The select inputs I_1 to I_3 are provided with an on-chip pull-up element, and they may therefore be left floating (equals HIGH state).

LINEARITY

V_{DD} = 10 V; $V_{ref\ max}$ = 9,5 V; $V_{ref\ min}$ = 0,5 V; T_{amb} = 25 °C

ΔV_1 = 250 mV (this is the tolerance of the step voltage).

$$V_{step} = V_{step}' + \Delta V_1 \qquad [1]$$

V_{step}' is the (internal) voltage drop across the resistor-ladder network.

$$V_{step}' = \frac{(V_{ref\ max} \pm \Delta V_2) - (V_{ref\ min} \pm \Delta V_2)}{18} \qquad [2]$$

ΔV_2 is the maximum offset voltage spread of the on-chip voltage follower.

ΔV_2 = 250 mV.

The linearity is guaranteed for $V_{DD} > 10$ V.
The monotony between V_{DD} = 5 V and 10 V is guaranteed. During ramping-up of the input voltage a maximum of two bars might be activated simultaneously.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(bar)n}$;

$$V_{T(bar)n} = (V_{ref\ min} \pm \Delta V_2{}^*) + \{ (n-1)\ V_{step}' \pm \Delta V_1 \}, \text{ in which} \qquad [3]$$

n = number of bars; $2 \leqslant n \leqslant 18$.

For n = 1 (first bar) see text above.

* For ΔV_2 the same sign (+ or −) should be used as in equation [2].

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to + 18	V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5	V
D.C. current into any input or output	$\pm I_I$	max. 10	mA
Storage temperature	T_{stg}	−25 to + 125	°C
Operating ambient temperature	T_{amb}	−20 to + 85	°C

NOTES (to D.C. CHARACTERISTICS)

1. $V_{ref\ min}$ = 0,5 V; $V_{ref\ max}$ = 9,5 V; $V_{osc} = V_c$ = 0 V; I_1, I_2 and I_3 at V_{DD}.
2. Pin under test at V_{SS} or V_{DD}, all other inputs simultaneously at V_{SS} or V_{DD}.
3. I_O = 0; all inputs at V_{SS} or V_{DD}.
4. At V_{DD} = 5 V: V_{OH} = 4,5 V.
   At V_{DD} = 10 V: V_{OH} = 9,5 V.
   At V_{DD} = 15 V: V_{OH} = 13,5 V.
5. At V_{DD} = 5 V: V_{OL} = 0,4 V; inputs at V_{SS} or V_{DD}.
   At V_{DD} = 10 V: V_{OL} = 0,5 V; inputs at V_{SS} or V_{DD}.
   At V_{DD} = 15 V: V_{OL} = 1,5 V; inputs at V_{SS} or V_{DD}.
6. $V_{ref\ min} + 4\ V < V_{ref\ max}$.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C)								notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Quiescent device current	5	I_{DD}	–	–	–	–	–	–	–	μA	
	10		–	–	–	–	1000	–	–	μA	1
	15		–	–	–	–	1600	–	–	μA	
Input leakage current (except select inputs)	5	$\pm I_{IN}$	–	–	–	–	100	–	–	nA	
	10		–	–	–	–	100	–	–	nA	2
	15		–	–	–	–	100	–	–	nA	
Input voltage HIGH select inputs	5	V_{IH}	3,5	–	3,5	–	–	3,5	–	V	
	10		7,0	–	7,0	–	–	7,0	–	V	
	15		11,0	–	11,0	–	–	11,0	–	V	
Input voltage LOW select inputs	5	V_{IL}	–	1,5	–	–	1,5	–	1,5	V	
	10		–	3,0	–	–	3,0	–	3,0	V	
	15		–	4,0	–	–	4,0	–	4,0	V	
Output voltage HIGH	5	V_{OH}	4,99	–	4,99	–	–	4,95	–	V	
	10		9,99	–	9,99	–	–	9,95	–	V	3
	15		–	–	14,99	–	–	–	–	V	
Output voltage LOW	5	V_{OL}	–	0,01	–	–	0,01	–	0,05	V	
	10		–	0,01	–	–	0,01	–	0,05	V	3
	15		–	0,01	–	–	0,01	–	0,05	V	
Output current HIGH	5	$-I_{OH}$	0,36	–	0,3	–	–	0,24	–	mA	
	10		0,80	–	0,7	–	–	0,56	–	mA	4
	15		3,0	–	2,8	–	–	2,60	–	mA	
Output current LOW	5	I_{OL}	0,34	–	0,3	–	–	0,24	–	mA	
	10		1,00	–	0,9	–	–	0,72	–	mA	5
	15		4,40	–	4,0	–	–	3,20	–	mA	
Input voltage control input V_c	5	V_{IC}	–	–	0	–	5	–	–	V	
	10		–	–	0	–	10	–	–	V	6
	15		–	–	0	–	15	–	–	V	
Max. input voltage $V_{ref\,max}$ input	5	V_{IRmax}	–	–	4,5	–	4,5	–	–	V	
	10		–	–	4,5	–	9,5	–	–	V	6
	15		–	–	4,5	–	14,5	–	–	V	
Min. input voltage $V_{ref\,min}$ input	5	V_{IRmin}	–	–	0,5	–	0,5	–	–	V	
	10		–	–	0,5	–	5,5	–	–	V	6
	15		–	–	0,5	–	10,5	–	–	V	
Operating supply current	10	I_{DD}	–	–	–	750	–	–	–	μA	Fig. 3

For notes see opposite page.

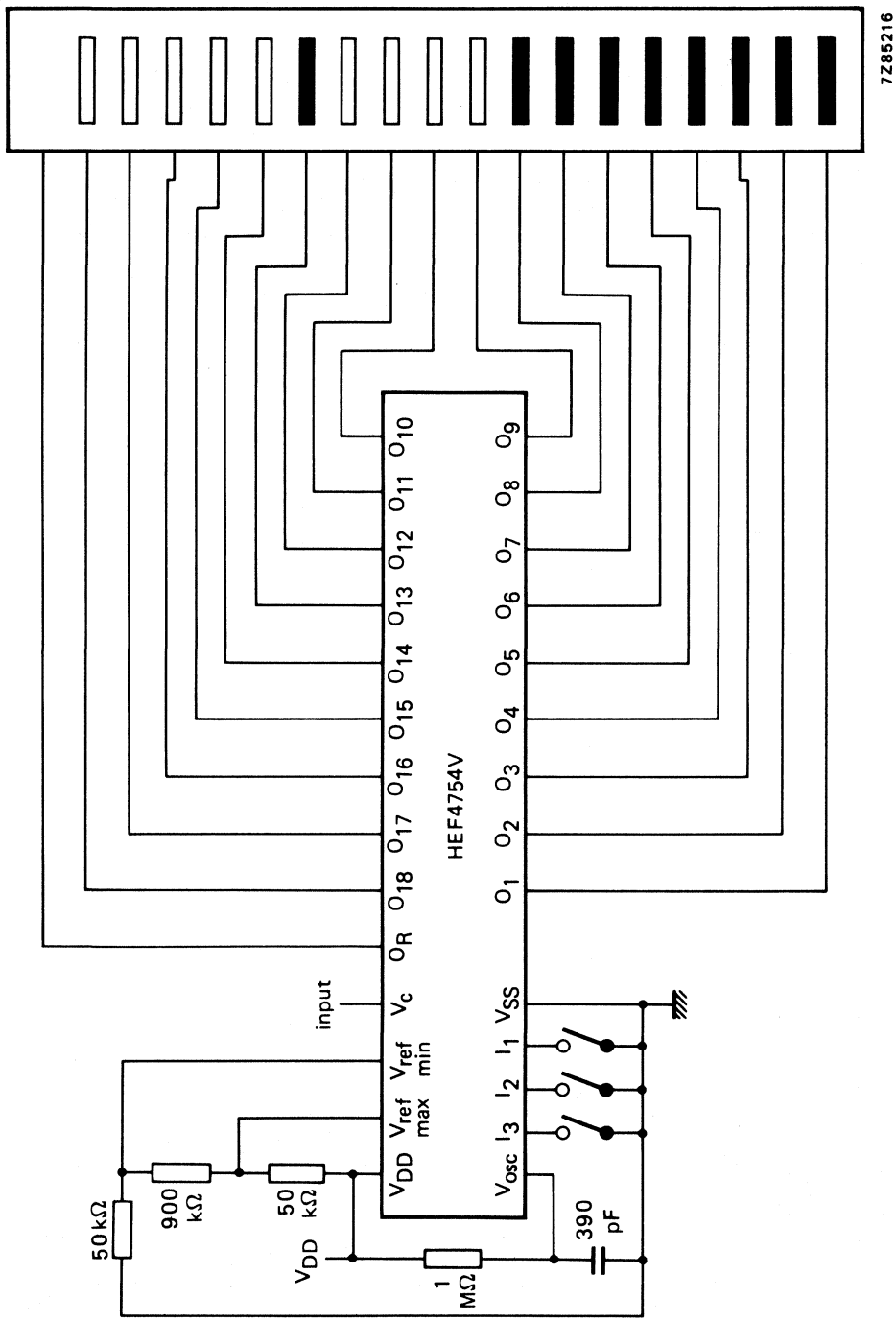


Fig. 3 Typical operating set-up.

TRANSCEIVER FOR SERIAL DATA COMMUNICATION

The HEF4755V transceiver is a circuit for serial data communication. It provides maximum transmission security and effectiveness. Therefore, in addition to the normal precautions, it contains a programmable digital bit-check, a programmable CRC (Cyclic Redundancy Check; Hamming distance 4 or 6) and format protection.

The circuit has 8 possible operating modes:

- synchronous
  - error checking only
  - receiving
  - transmitting
  - receiving with data out and transmitting the same message
- asynchronous
  - error checking only
  - receiving
  - transmitting
  - receiving with data out and transmitting of a regenerated message.

FEATURES

- Transmission rate:

V_{DD}	synchronous	asynchronous
5 V	0,8 Mbaud	31 kbaud
7 V	1,6 Mbaud	62 kbaud
10 V	3,2 Mbaud	125 kbaud

- Inputs: standard LOCMOS
- Outputs: TTL compatible (1 TTL load)
- Operating ambient temperature range: −40 to + 85 °C
- Transmit or receive a serial binary data stream
- Start bit generation and recognition
- Format protection and checking
- Redundancy byte generation and checking
- Digital bit check
- Error recognition and error distinguishing
- 8-bit parallel input/output transfer

SUPPLY VOLTAGE/CURRENT

	rating	recommended operating	
V_{DD}	−0,5 to + 15	4,75 to 12,6	V
I_{SS}	30	–	mA

FAMILY DATA

I_{DD} LIMITS catagory LSI } see Family Specification

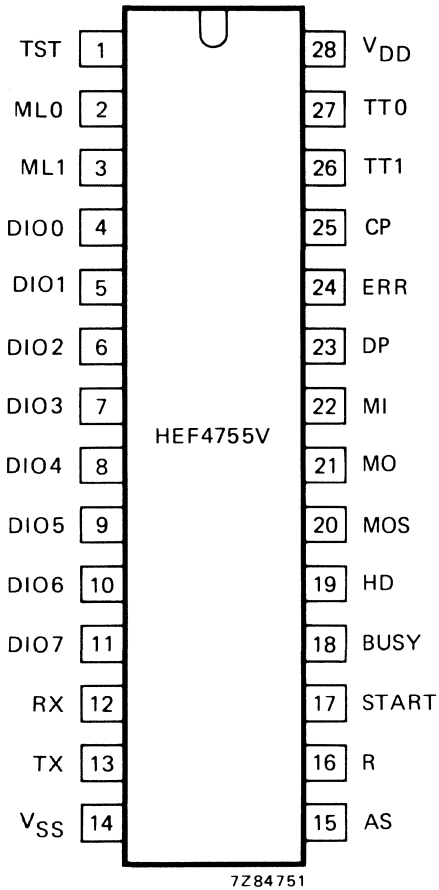


Fig. 1 Pinning diagram.

HEF4755VP: 28-lead DIL; plastic (SOT-117).
HEF4755VD: 28-lead DIL; ceramic (cerdip) (SOT-135A).
HEF4755VT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

PINNING

1	TST	Test pin; during normal use connected to V_{SS}. When TST is HIGH (V_{DD}), internal check points are connected to the data bus.
2 3	ML0 ML1	Input code for message length (see Table 1).
4 to 11	DIO0 to DIO7	Bidirectional data bus.
12	RX	Mode input: receive (see Table 2)
13	TX	Mode input: transmit (see Table 2)
15	AS	Mode input: asynchronous (see Table 2)
16	R	Reset; a positive signal resets all internal registers.
17	START	Input start in transmitting mode; synchronization input (from MOS) in synchronous receiving mode.
18	BUSY	Output busy; active during receiving or transmitting a message.
19	HD	Hamming distance; determines the length of the redundancy byte: LOW = 7 bit (HD = 4) HIGH = 15 bit (HD = 6)
20	MOS	Output message synchronization used in synchronous mode.
21	MO	Message output.
22	MI	Message input.
23	DP	Output data pulse; take-over pulse for data on the data bus.
24	ERR	Output error; an active output means that at least 1 transmission error is recognized.
25	CP	Clock input; in synchronous mode equal to the transmission bit rate.
26 27	TT1 TT0	Programming of the permissible time tolerance in bit distortion (see Table 3).
28	V_{DD}	Positive supply voltage; 4,5 V to 12,5 V (is the logic HIGH level).
14	V_{SS}	Ground (is the logic LOW level).

Table 1 Input code for message length

ML0	ML1	message length
H	H	6 data bytes
L	H	4 data bytes
H	L	2 data bytes
L	L	variable length depends on format byte

Table 2 Input code for input mode

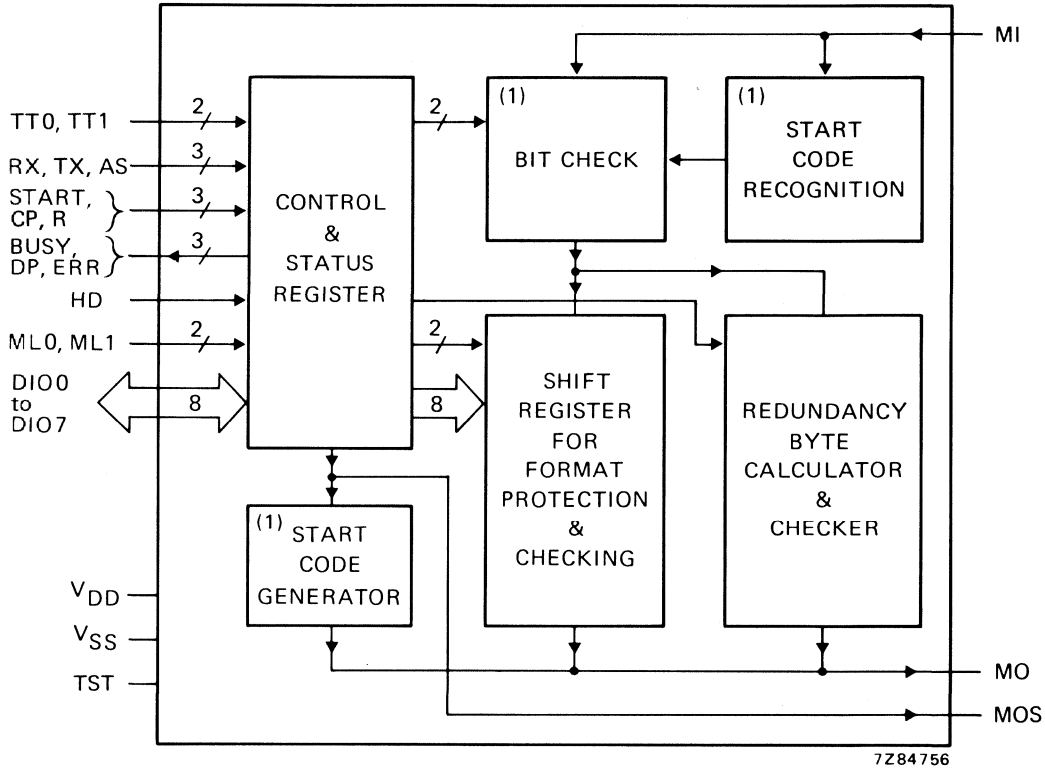
RX	TX	AS	
L	L	L	status register connected to the data bus for error recognition
H	L	L	receiving in synchronous mode
L	H	L	transmitting in synchronous mode
H	H	L	receiving messages (without redundancy bit); data parallel out; calculating of redundancy byte; transmitting data with redundancy byte in synchronous mode
L	L	H	only bit check in asynchronous mode; no data output on data bus
H	L	H	receiving in asynchronous mode
L	H	H	transmitting in asynchronous mode
H	H	H	receiving and transmitting of a regenerated message in the asynchronous mode

Table 3 Permissible time tolerance in bit distortion

TT1	TT0	permitted distortion (dt/T)
L	L	$6/32 \approx 19\%$
L	H	$8/32 = 25\%$
H	L	$10/32 \approx 31\%$
H	H	$12/32 \approx 37\%$

H = HIGH state (the most positive voltage)
L = LOW state (the least positive voltage)

DEVELOPMENT DATA



(1) Only used in the asynchronous mode.

Fig. 2 Block diagram.

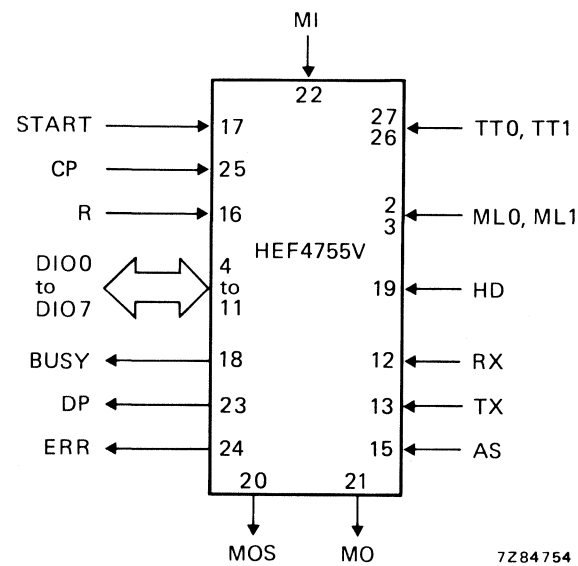


Fig. 3 Functional diagram.

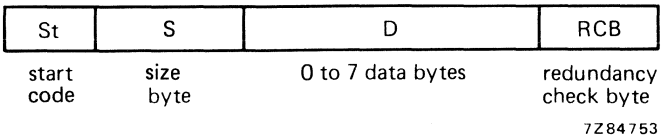
FUNCTIONAL DESCRIPTION

General

The HEF4755V is used for protected-bit serial data communication. This protection makes it necessary to subdivide the serial data stream into data blocks called messages.

Messages

In the synchronous mode the HEF4755V will transmit or receive a message as follows:



The first bit of a transmitted message is the start-bit which cannot be mis interpreted. It instructs the receiver, that information transfer has started and it defines the time-window for the following bits. The start-bit is only necessary in the asynchronous mode and it is omitted in the synchronous mode. The first byte contains the number of data bytes that will follow. This byte is checked by the receiver and if a discrepancy is found, the receiver reports a code-error. This first byte is called 'size'.
The number of data bytes can also be fixed by wiring of the transmitter as well as the receiver. In this case the size byte is omitted.
There is no protocol on the information of the data bytes, so the maximum number of informations per message is $2^{56} \approx 10^{17}$.
The redundancy check byte secures the data bytes against transmission errors. This byte is calculated in parallel to the data stream and it is send as last byte by the transmitter. The receiver calculates its own redundancy byte and compares it with the received one. If there is a discrepancy, the receiver reports a code error.

Code protection

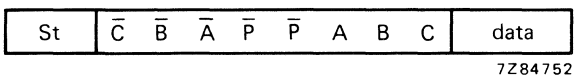
Size

The coding of the size byte is as follows:

DIO0 = C
DIO1 = B
DIO2 = A
DIO3 = P

$$n = C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$$
$$= \overline{C \oplus B \oplus A}$$

The information is transmitted as follows:



With this, a hamming distance of 4 is obtained.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Redundancy byte

The redundancy byte completes the data bytes with 15 (7) bits as a code word. If only one bit in the information has changed during the transmission, the two code words will differ by at least 6 (4) bit positions. So a change of up to 5 (3) bits will always be observed, even every odd number of false bits will be recognized. The HEF4755V has a programmable redundancy bit calculator which carries out this protection (the numbers given in parentheses are valid for the alternative possibility).
If the transmission line carries extreme noise, this kind of message protection is less effective. In this case, the message is protected by checking bit-per-bit in a smaller time scale (see 'bit protection' below).

Bit protection

The HEF4755V checks every received bit within the time window defined by the start-bit. The programmed time tolerance (19%, 25%, 31% and 37%) determines that the bit protection circuit decides after 32 samples which bit is a true logic HIGH or LOW level, or an error. In the latter case, there are too many samples HIGH to obtain a LOW and, too many samples LOW to obtain a HIGH.

Transmitting

In the transmitting mode the HEF4755V uses the data pulse signal (DP, pin 23) to take 8 bits from the data bus. These parallel bits are shifted serially to the message output (MO).

Receiving

In the receiving mode the HEF4755V receives serial bits at the message input (MI). The circuit checks the message for transmission errors and, with every data pulse, 8 bits are transferred in parallel to the data bus. Every recognized error is stored and the error output is activated. The kind of error can be recognized by reading the status register over the data bus.

Asynchronous and synchronous mode

If only one transmission line is available, then the receiver waits for the start-bit, synchronizes itself on the start bit and receives all the data bits of one message. This is called the *asynchronous mode.* By using 3 transmission lines, the circuit can go to the *synchronous mode.* In this case it is possible to transmit also the clock signal (CP) and message synchronization signal (MOS) in parallel with the data bits. The start bit and the bit check are omitted. In the synchronous mode the maximum transmission speed is 32 times the maximum speed in the asynchronous mode.

In asynchronous receive mode a reset pulse is necessary between two messages. It is possible to derive this reset pulse from the busy signal by using hardware. The duration of the START-pulse at the transmitter must always be shorter than the message to be transferred. A good procedure for achieving this is to use the BUSY-signal to end the START-pulse. The recovery time between two messages must be at least two bit periods. During this time, the line must remain stable to prevent generation of an error. This must be ensured with external hardware/software.

In the synchronous receive mode, the duration of the START-pulse at the transmitter must always be shorter than the message to be transferred. A good procedure for achieving this is to use the BUSY-signal to end the START-pulse. A continuous START-signal will cause malfunction. The recovery time between two messages must be at least one bit period. During this time, the message line must remain stable. A good way to achieve this is to use the trailing-edge of the BUSY-signal to generate a START-signal. In practice, if data is delivered to the transmitter fast enough, START can be $\overline{\text{BUSY}}$. If the lines have different delays, the message line should have the longest delay. If it is not certain which line has the longest delay it is possible to phase-shift the clock signal of the receiver by inverting it. This is only possible with point-to-point lines.

DEVELOPMENT DATA TA

D.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	conditions
Outputs							
Output voltage LOW	4,75 to 12,6	V_{OL}	–	–	0,4	V	I_{OL} = 1,8 mA
	4,75	V_{OL}	–	–	0,4	V	I_{OL} = 2,3 mA; T_{amb} = 25 °C
Output voltage HIGH	4,75 to 12,6	V_{OH}	V_{DD}−1	–	–	V	$-I_{OH}$ = 1,1 mA
	4,75	V_{OH}	V_{DD}−1	–	–	V	$-I_{OH}$ = 1,4 mA; T_{amb} = 25 °C
Inputs/outputs							
As outputs							
Output voltage LOW	4,75 to 12,6	V_{OL}	–	–	0,4	V	I_{OL} = 1,8 mA
	4,75	V_{OL}	–	–	0,4	V	I_{OL} = 2,3 mA; T_{amb} = 25 °C
Output voltage HIGH	4,75 to 12,6	V_{OH}	V_{DD}−1	–	–	V	$-I_{OH}$ = 1,1 mA
	4,75	V_{OH}	V_{DD}−1	–	–	V	$-I_{OH}$ = 1,4 mA; T_{amb} = 25 °C
Output leakage current HIGH	12,6	I_{OZH}	–	–	20	μA	V_{OH} = 12,6 V
	12,6	I_{OZH}	–	–	5	μA	V_{OH} = 12,6 V; T_{amb} = 25 °C
LOW		$-I_{OZL}$	–	–	20	μA	V_{OL} = 0 V
		$-I_{OZL}$	–	–	5	μA	V_{OL} = 0 V; T_{amb} = 25 °C
As inputs							
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3 V_{DD}	V	
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7 V_{DD}	–	V_{DD}	V	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	conditions
Asynchronous mode							AS at V_{DD}
Clock pulse width LOW	5	t_{WCPL}	500			ns	
	10		125			ns	
HIGH	5	t_{WCPH}	500			ns	
	10		125			ns	
START pulse width HIGH	5	t_{WSH}	0,9			μs	
	10		0,22			μs	
Set-up time $D_n \rightarrow$ CP	5	t_{su}	1,4			μs	
	10		0,35			μs	
Hold time CP $\rightarrow$ D_n	5	t_{hold}	0			μs	
	10		0			μs	
Reset (R) pulse width HIGH	5	t_{WRH}	1			μs	
	10		0,25			μs	
Synchronous mode							AS at V_{SS}
Clock pulse width LOW	5	t_{WCPL}	625			ns	
	10		150			ns	
HIGH	5	t_{WCPH}	625			ns	
	10		150			ns	
Set-up time START $\rightarrow$ CP	5	t_{su}	0,6			μs	
	10		0,15			μs	
Hold time CP $\rightarrow$ START	5	t_{hold}	300			ns	
	10		75			ns	
Set-up time $D_n \rightarrow$ CP	5	t_{su}	600			ns	
	10		150			ns	
Hold time CP $\rightarrow$ D_n	5	t_{hold}	0			ns	
	10		0			ns	
Reset (R) pulse width HIGH	5	t_{WRH}	1			μs	
	10		0,25			μs	

Note

Measured between output voltage levels of 0,8 V and 2 V.

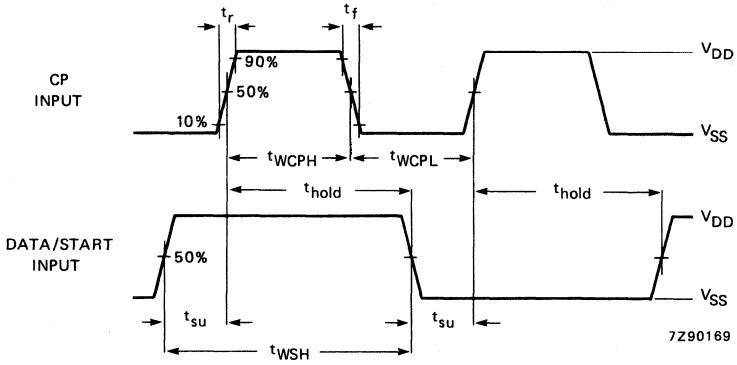


Fig. 4 Waveforms showing the clock, data and start timing.

DEVELOPMENT DATA

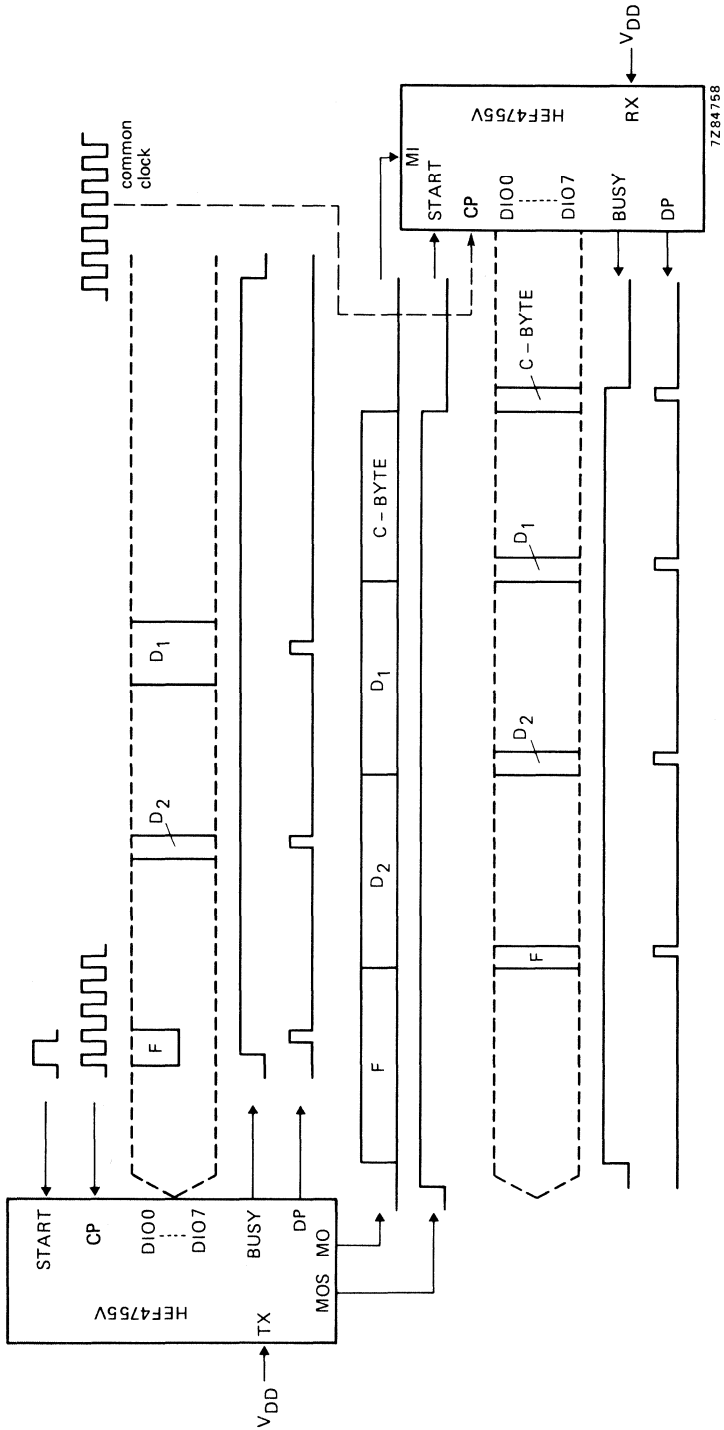


Fig. 5 Function/timing diagram when using the HEF4755V in the asynchronous mode where the byte number per message is variable and the hamming distance is 4.

DEVELOPMENT DATA

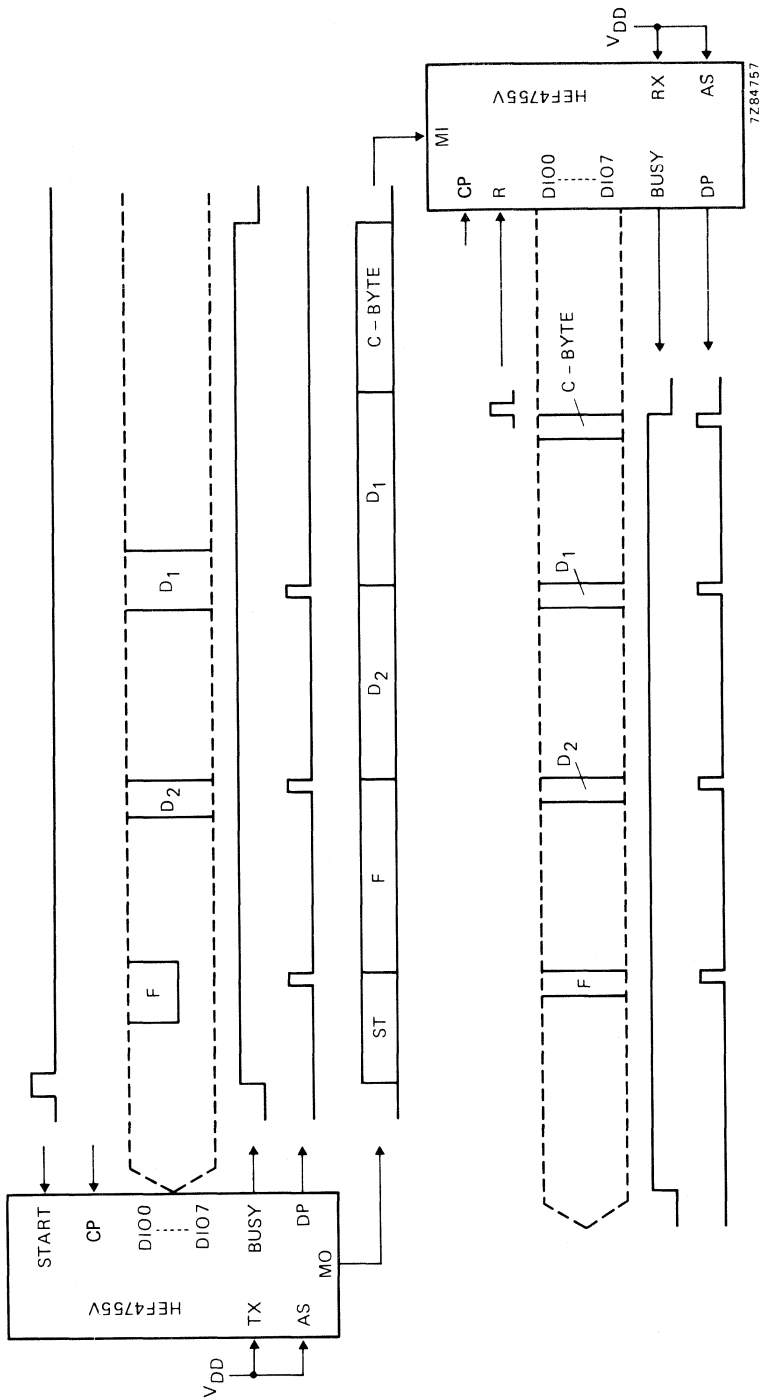


Fig. 6 Function/timing diagram when using the HEF4755V in the asynchronous mode where the byte number per message is variable and the hamming distance is 4.

3-STATE HEX NON-INVERTING BUFFER

The HEF40097B is a hex non-inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs ($\overline{EO}_4$ and $\overline{EO}_2$). A HIGH on $\overline{EO}_4$ causes four of the six buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions and a HIGH on $\overline{EO}_2$ causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions.

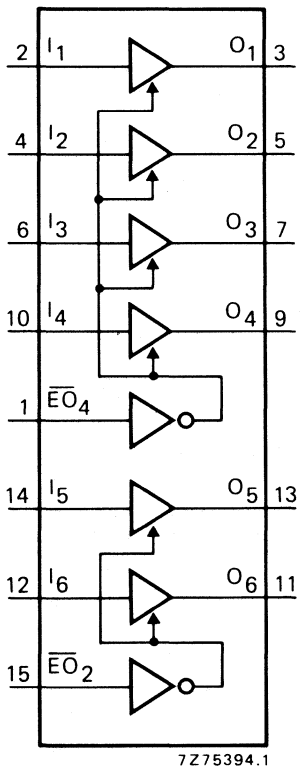


Fig. 1 Functional diagram.

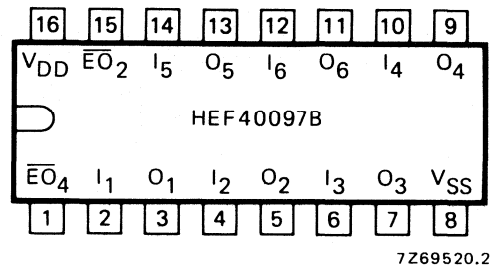


Fig. 2 Pinning diagram.

HEF40097BP : 16-lead DIL; plastic (SOT-38Z).
HEF40097BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40097BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

I_1 to I_6	buffer inputs
$\overline{EO}_4$, $\overline{EO}_2$	enable inputs (active LOW)
O_1 to O_6	buffer outputs (active HIGH)

FAMILY DATA

I_{DD} LIMITS category BUFFERS

see Family Specifications

Products approved to CECC 90 104-090.

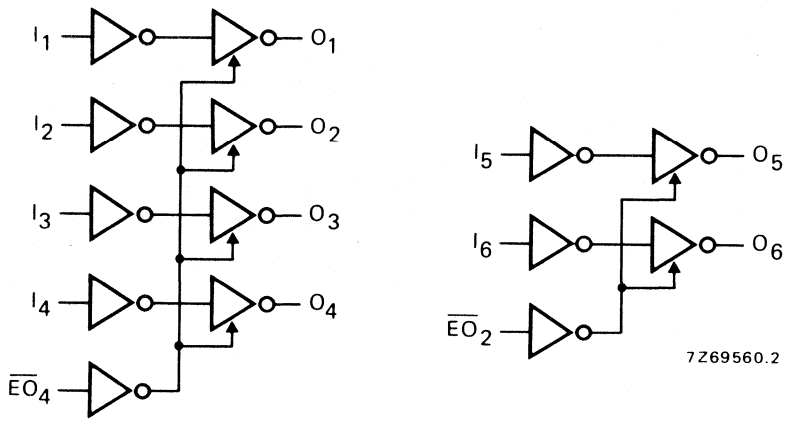


Fig. 3 Logic diagram.

D.C. CHARACTERISTICS

V_{SS} = 0 V

HEF	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output current HIGH	5	4,6		$-I_{OH}$	1,2		1,0		0,8		mA
	10	9,5			3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current LOW	4,75		0,4	I_{OL}	3,5		2,9		2,3		mA
	10		0,5		12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

HEC	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −55 min.	−55 max.	+25 min.	+25 max.	+125 min.	+125 max.	
Output current HIGH	5	4,6		$-I_{OH}$	1,25		1,0		0,6		mA
	10	9,5			4,0		3,2		2,1		mA
	15	13,5			12,5		10,0		6,7		mA
HIGH	5	2,5		$-I_{OH}$	4,0		3,2		2,1		mA
Output current LOW	4,75		0,4	I_{OL}	3,6		2,9		1,9		mA
	10		0,5		12,5		10,0		6,7		mA
	15		1,5		25,0		20,0		13,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		70	140	ns	60 ns + (0,20 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	26 ns + (0,08 ns/pF) C_L
	15		25	50	ns	22 ns + (0,06 ns/pF) C_L
	5		60	120	ns	45 ns + (0,30 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	19 ns + (0,13 ns/pF) C_L
	15		20	40	ns	16 ns + (0,09 ns/pF) C_L
Output transition times	5		30	60	ns	15 ns + (0,30 ns/pF) C_L
HIGH to LOW	10	t_{THL}	15	30	ns	10 ns + (0,11 ns/pF) C_L
	15		10	20	ns	7 ns + (0,07 ns/pF) C_L
	5		35	70	ns	10 ns + (0,50 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	20	40	ns	8 ns + (0,24 ns/pF) C_L
	15		15	30	ns	6 ns + (0,18 ns/pF) C_L
3-state propagation delays						
Output disable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow O_n$	5		45	95	ns	
HIGH	10	t_{PHZ}	35	70	ns	
	15		30	60	ns	
	5		60	120	ns	
LOW	10	t_{PLZ}	35	70	ns	
	15		25	55	ns	
Output enable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow O_n$	5		75	150	ns	
HIGH	10	t_{PZH}	35	70	ns	
	15		30	60	ns	
	5		95	190	ns	
LOW	10	t_{PZL}	40	80	ns	
	15		30	65	ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	5 400 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	25 200 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	96 500 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

3-STATE HEX INVERTING BUFFER

The HEF40098B is a hex inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs ($\overline{EO}_4$ and $\overline{EO}_2$). A HIGH on $\overline{EO}_4$ causes four of the six buffer elements to assume a high impedance or OFF-state regardless of the other input conditions and a HIGH on $\overline{EO}_2$ causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state regardless of the other input conditions.

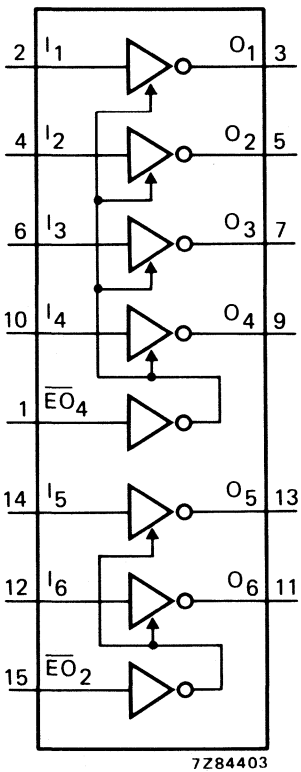


Fig. 1 Functional diagram.

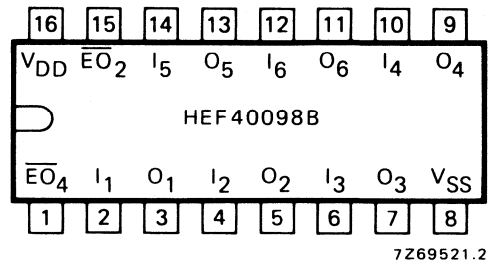


Fig. 2 Pinning diagram.

HEF40098BP : 16-lead DIL; plastic (SOT-38Z).
HEF40098BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40098BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

I_1 to I_6	buffer inputs
$\overline{EO}_4$, $\overline{EO}_2$	enable inputs (active LOW)
O_1 to O_6	buffer outputs (active LOW)

FAMILY DATA

I_{DD} LIMITS category BUFFERS } see Family Specifications

Products approved to CECC 90 104-091.

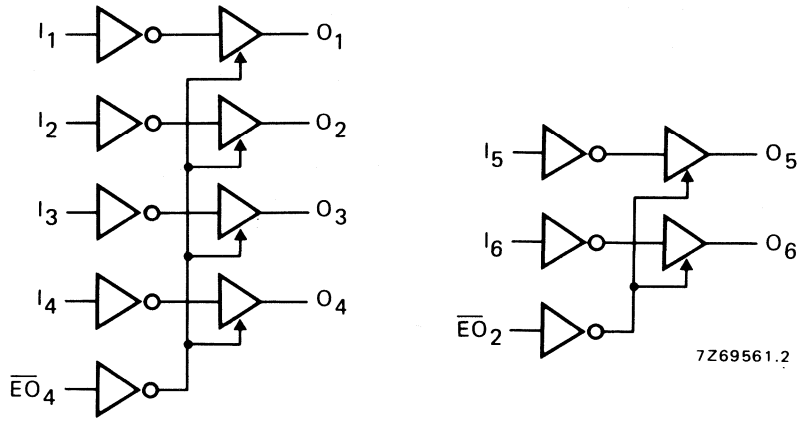


Fig. 3 Logic diagram.

D.C. CHARACTERISTICS

V_{SS} = 0 V

HEF	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output current HIGH	5	4,6			1,2		1,0		0,8		mA
	10	9,5		$-I_{OH}$	3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current LOW	4,75		0,4		3,5		2,9		2,3		mA
	10		0,5	I_{OL}	12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

HEC	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −55 min.	−55 max.	+25 min.	+25 max.	+125 min.	+125 max.	
Output current HIGH	5	4,6			1,25		1,0		0,6		mA
	10	9,5		$-I_{OH}$	4,0		3,2		2,1		mA
	15	12,5			12,5		10,0		6,7		mA
HIGH	5	2,5		$-I_{OH}$	4,0		3,2		2,1		mA
Output current LOW	4,75		0,4		3,6		2,9		1,9		mA
	10		0,5	I_{OL}	12,5		10,0		6,7		mA
	15		1,5		25,0		20,0		13,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		80	160	ns	70 ns + (0,20 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	31 ns + (0,08 ns/pF) C_L
	15		25	50	ns	22 ns + (0,06 ns/pF) C_L
	5		65	130	ns	50 ns + (0,30 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	24 ns + (0,13 ns/pF) C_L
	15		25	50	ns	23 ns + (0,05 ns/pF) C_L
Output transition times						
	5		30	60	ns	15 ns + (0,30 ns/pF) C_L
HIGH to LOW	10	t_{THL}	15	30	ns	10 ns + (0,11 ns/pF) C_L
	15		10	20	ns	7 ns + (0,07 ns/pF) C_L
	5		35	70	ns	10 ns + (0,50 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	20	40	ns	8 ns + (0,24 ns/pF) C_L
	15		15	30	ns	6 ns + (0,18 ns/pF) C_L
3-state propagation delays						
Output disable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow O_n$	5		45	85	ns	
HIGH	10	t_{PHZ}	35	65	ns	
	15		30	60	ns	
	5		65	135	ns	
LOW	10	t_{PLZ}	40	80	ns	
	15		35	70	ns	
Output enable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow O_n$	5		70	140	ns	
HIGH	10	t_{PZH}	35	75	ns	
	15		30	65	ns	
	5		90	185	ns	
LOW	10	t_{PZL}	40	85	ns	
	15		35	70	ns	

	V_{DD} V	typical formula for P (μW)	where
			f_i = input freq. (MHz)
			f_o = output freq. (MHz)
Dynamic power dissipation per package (P)	5	5 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	C_L = load cap. (pF)
	10	22 800 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	$\Sigma(f_o C_L)$ = sum of outputs
	15	81 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	V_{DD} = supply voltage (V)

HEX INVERTING SCHMITT TRIGGER

Each circuit of the HEF40106B functions as an inverter with Schmitt-trigger action. The Schmitt-trigger switches at different points for the positive and negative-going input signals. The difference between the positive-going voltage (V_P) and the negative-going voltage (V_N) is defined as hysteresis voltage (V_H).

This device may be used for enhanced noise immunity or to "square up" slowly changing waveforms.

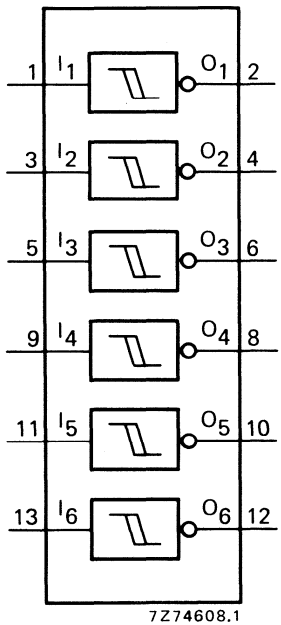


Fig. 1 Functional diagram.

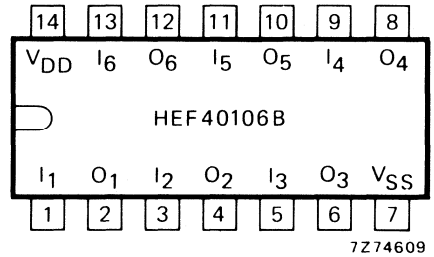


Fig. 2 Pinning diagram.

HEF40106BP : 14-lead DIL; plastic (SOT-27).
HEF40106BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF40106BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

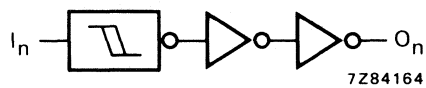


Fig. 3 Logic diagram (one inverter).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C

	V_{DD} V	symbol	min.	typ.	max.	
Hysteresis voltage	5	V_H	0,5	0,8		V
	10		0,7	1,3		V
	15		0,9	1,8		V
Switching levels positive-going input voltage	5	V_P	2	3,0	3,5	V
	10		3,7	5,8	7	V
	15		4,9	8,3	11	V
negative-going input voltage	5	V_N	1,5	2,2	3	V
	10		3	4,5	6,3	V
	15		4	6,5	10,1	V

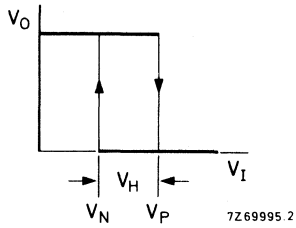


Fig. 4 Transfer characteristic.

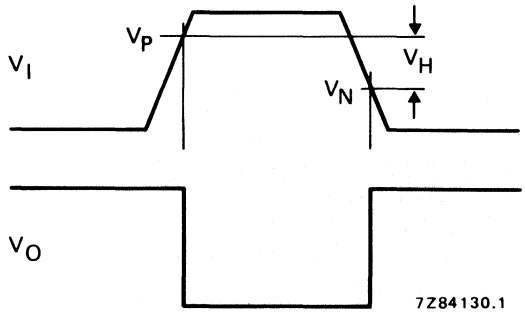


Fig. 5 Waveforms showing definition of V_P, V_N and V_H, where V_N and V_P are between limits of 30% and 70%.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2 300 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	9 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	20 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

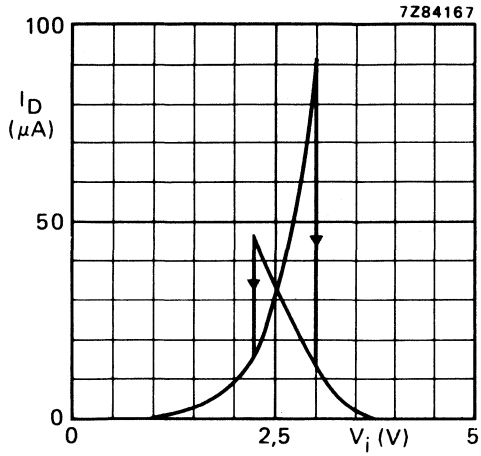


Fig. 6 Typical drain current as a function of input voltage; V_{DD} = 5 V; T_{amb} = 25 °C.

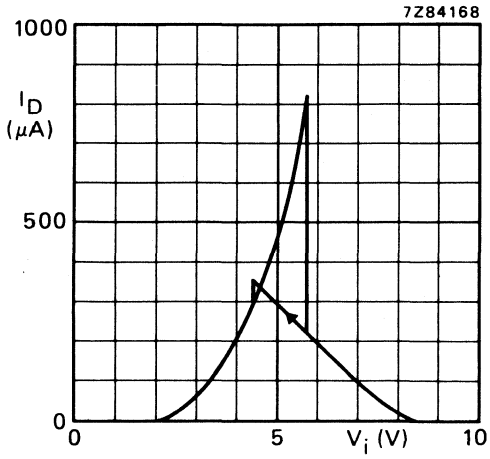


Fig. 7 Typical drain current as a function of input voltage; V_{DD} = 10 V; T_{amb} = 25 °C.

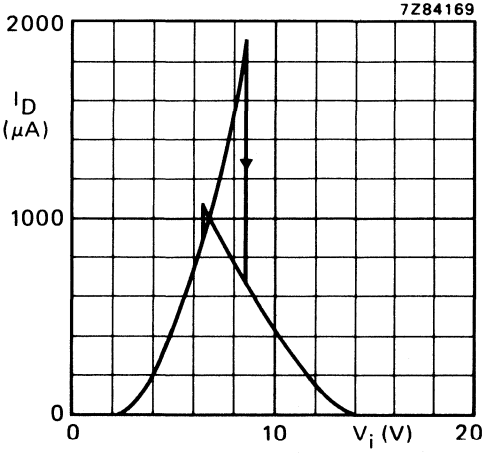


Fig. 8 Typical drain current as a function of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

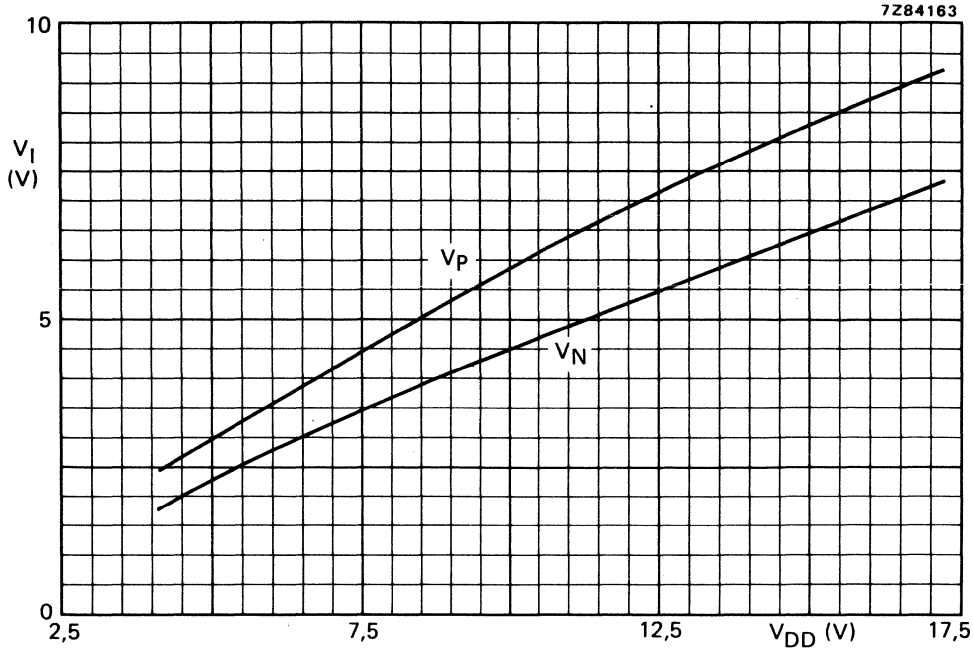


Fig. 9 Typical switching levels as a function of supply voltage V_{DD}; T_{amb} = 25 °C.

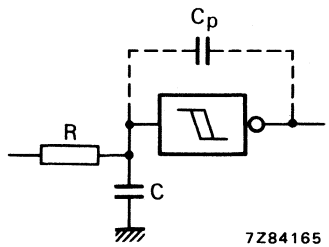


Fig. 10 Schmitt trigger driven via a high impedance (R > 1 kΩ).

If a Schmitt trigger is driven via a high impedance (R > 1 kΩ) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD}-V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

C_p is the external parasitic capacitance between input and output; the value depends on the circuit board layout.

APPLICATION INFORMATION

Some examples of applications for the HEF40106B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

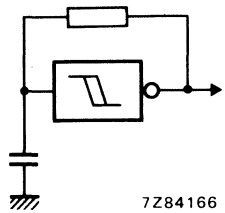


Fig. 11 The HEF40106B used as an astable multivibrator.

4-BIT SYNCHRONOUS DECADE COUNTER WITH ASYNCHRONOUS RESET

The HEF40160B is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), an overriding asynchronous master reset ($\overline{MR}$), four parallel data inputs (P_0 to P_3), three synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous (except for the $\overline{MR}$ input) and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 regardless of the levels of CEP and CET inputs.

When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise, no change occurs in the state of the counter. TC is HIGH when the state of the counter is 9 ($O_0 = O_3$ = HIGH, $O_1 = O_2$ = LOW) and when CET is HIGH. A LOW on $\overline{MR}$ sets all outputs (O_0 to O_3 and TC) LOW, independent of the state of all other inputs. Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET and $\overline{PE}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.

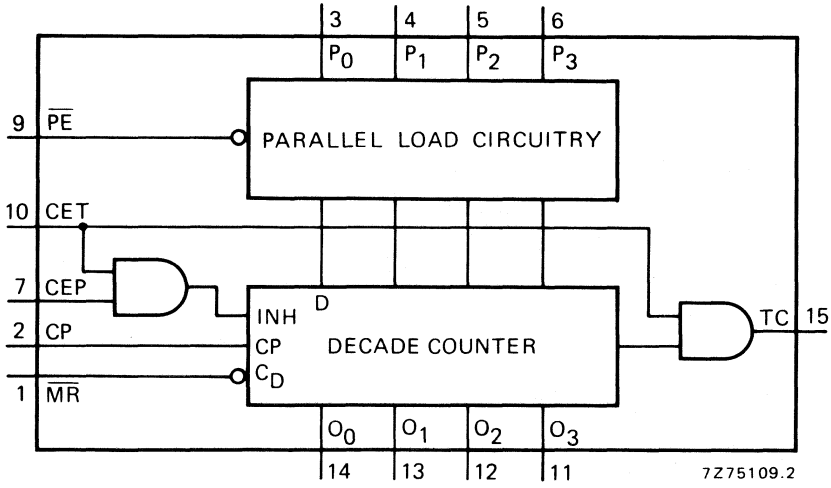


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Products approved to CECC 90 104-093.

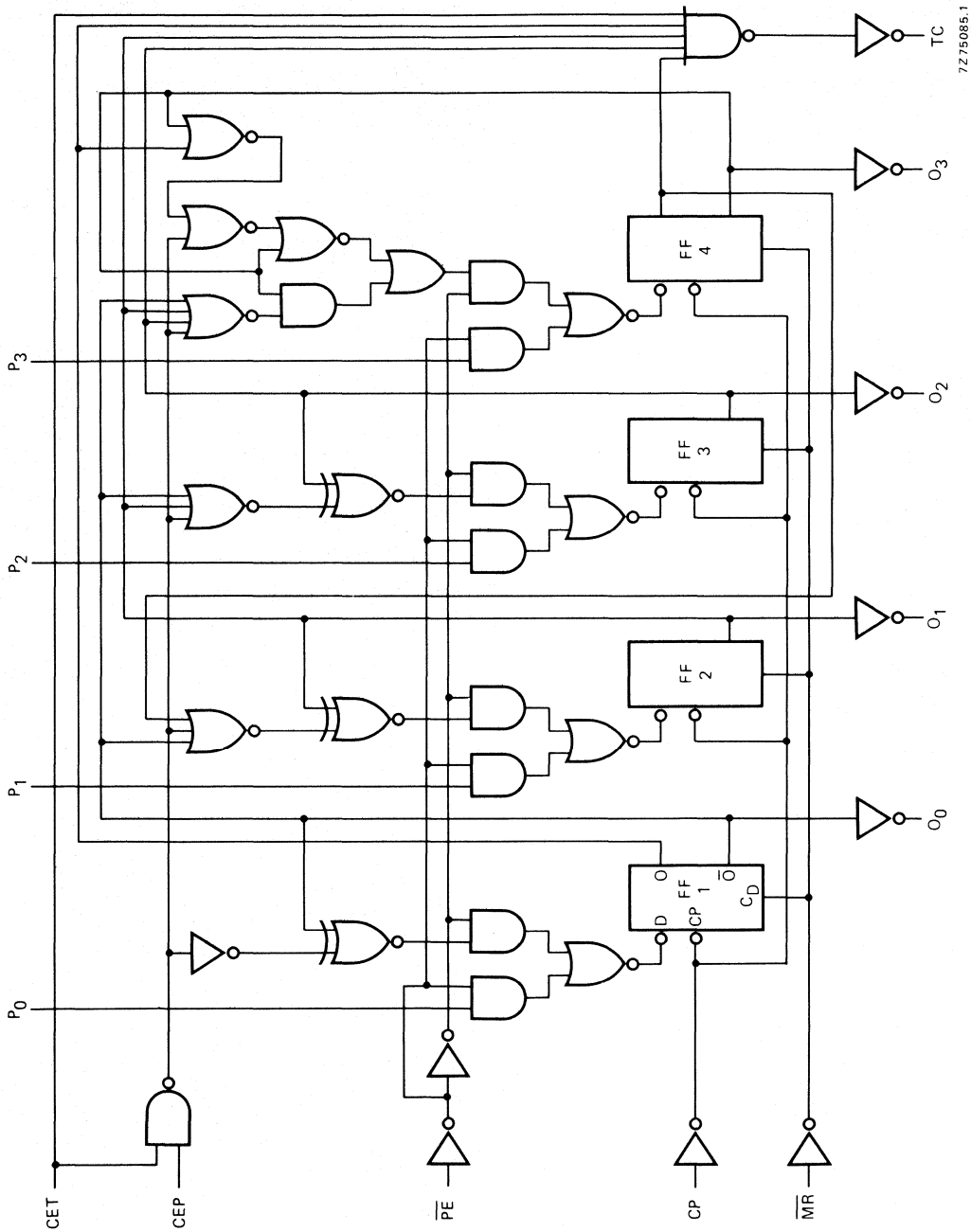


Fig. 2 Logic diagram.

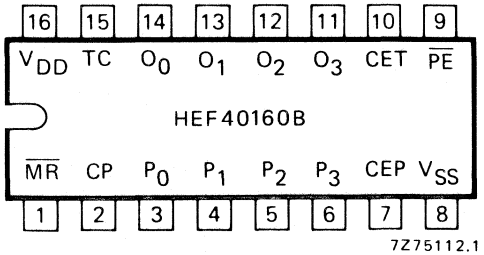


Fig. 3 Pinning diagram.

HEF40160BP : 16-lead DIL; plastic (SOT-38Z).
HEF40160BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40160BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

SYNCHRONOUS MODE SELECTION

$\overline{PE}$	CEP	CET	mode
L	X	X	preset
H	L	X	no change
H	X	L	no change
H	H	H	count

$\overline{MR}$ = HIGH

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3$

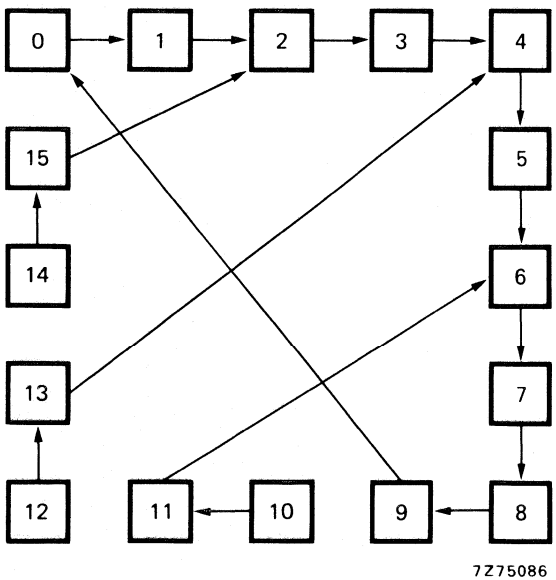


Fig. 4 State diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET → TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			120	245	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → TC	5			145	295	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	85	ns	37 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms Figs 5, 6, 7 and 8
	10		40	20		ns	
	15		30	15		ns	
Minimum $\overline{MR}$ pulse width; LOW	5	t_{WMRL}	100	50		ns	
	10		40	20		ns	
	15		30	15		ns	
Recovery time for $\overline{MR}$	5	t_{RMR}	25	0		ns	
	10		15	0		ns	
	15		10	0		ns	
Set-up times $P_n \longrightarrow CP$	5	t_{su}	110	55		ns	
	10		40	20		ns	
	15		30	15		ns	
$\overline{PE} \longrightarrow CP$	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
CEP, CET $\longrightarrow$ CP	5	t_{su}	260	130		ns	
	10		100	50		ns	
	15		70	35		ns	
Hold times $P_n \longrightarrow CP$	5	t_{hold}	20	−35		ns	
	10		10	−10		ns	
	15		5	−10		ns	
$\overline{PE} \longrightarrow CP$	5	t_{hold}	15	−45		ns	
	10		5	−15		ns	
	15		5	−10		ns	
CEP, CET $\longrightarrow$ CP	5	t_{hold}	25	−105		ns	
	10		15	−35		ns	
	15		10	−25		ns	
Maximum clock pulse frequency	5	f_{max}	2,5	5		MHz	
	10		7	14		MHz	
	15		9	18		MHz	

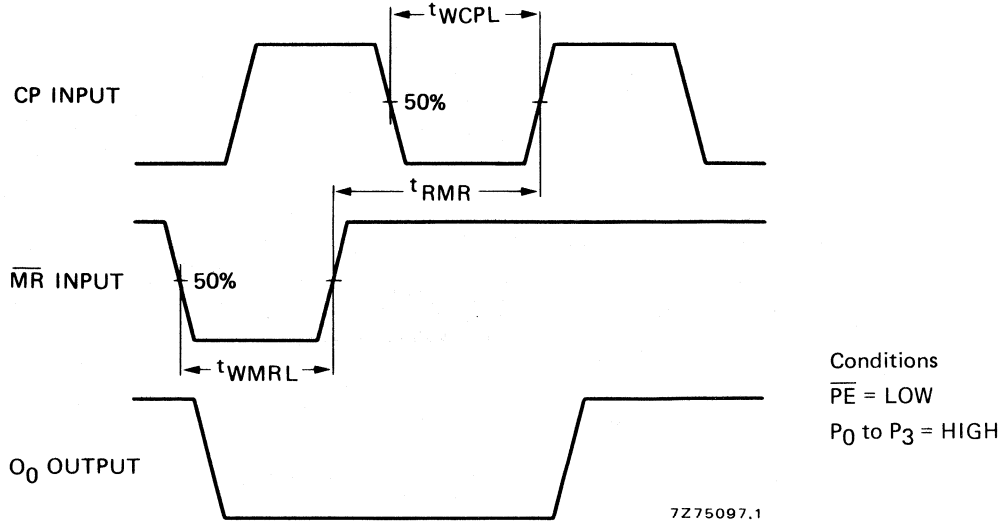


Fig. 5 Waveforms showing minimum CP and $\overline{MR}$ pulse widths and $\overline{MR}$ to CP recovery time.

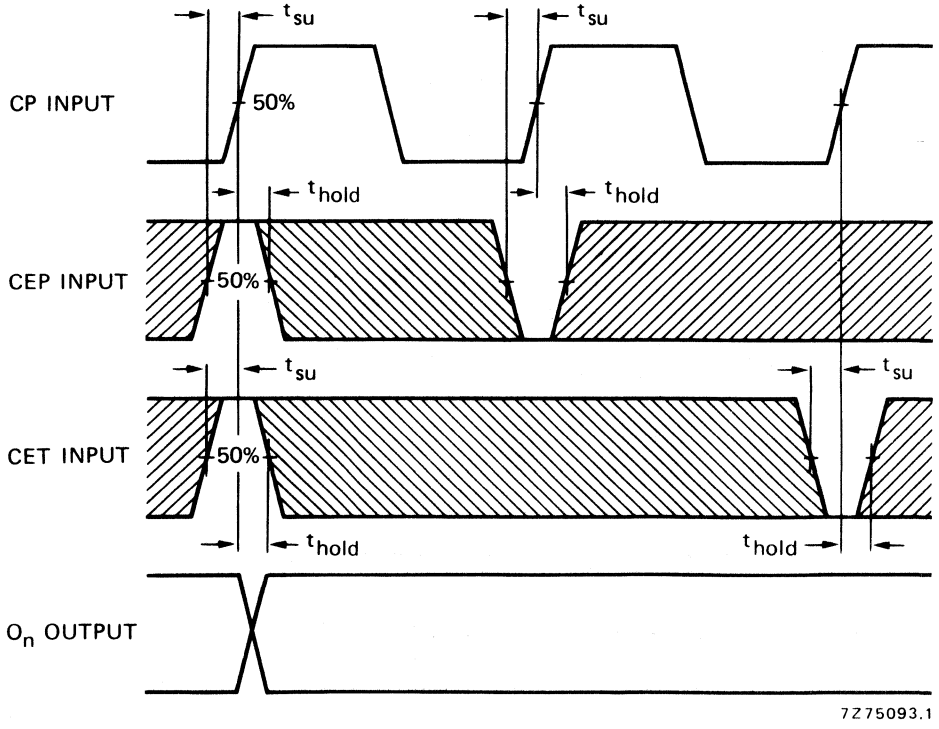
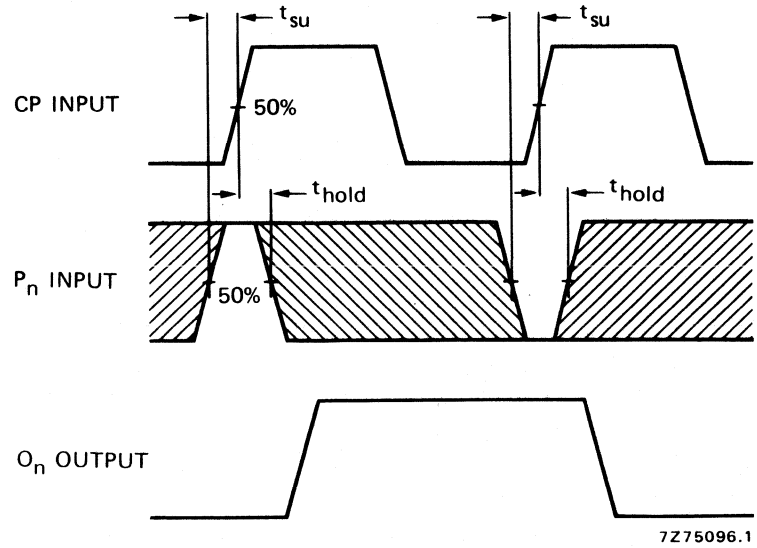


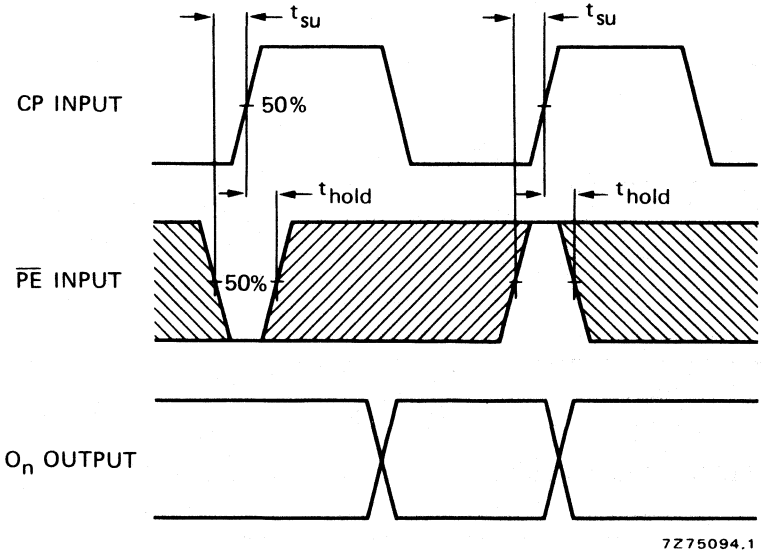
Fig. 6 Waveforms showing set-up times and hold times for CEP and CET inputs.

Conditions: $\overline{PE}$ = $\overline{MR}$ = HIGH.



Conditions
$\overline{PE}$ = LOW
$\overline{MR}$ = HIGH

Fig. 7 Waveforms showing set-up times and hold times for P_n inputs.



Condition
$\overline{MR}$ = HIGH

Fig. 8 Waveforms showing set-up times and hold times for $\overline{PE}$ inputs.

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

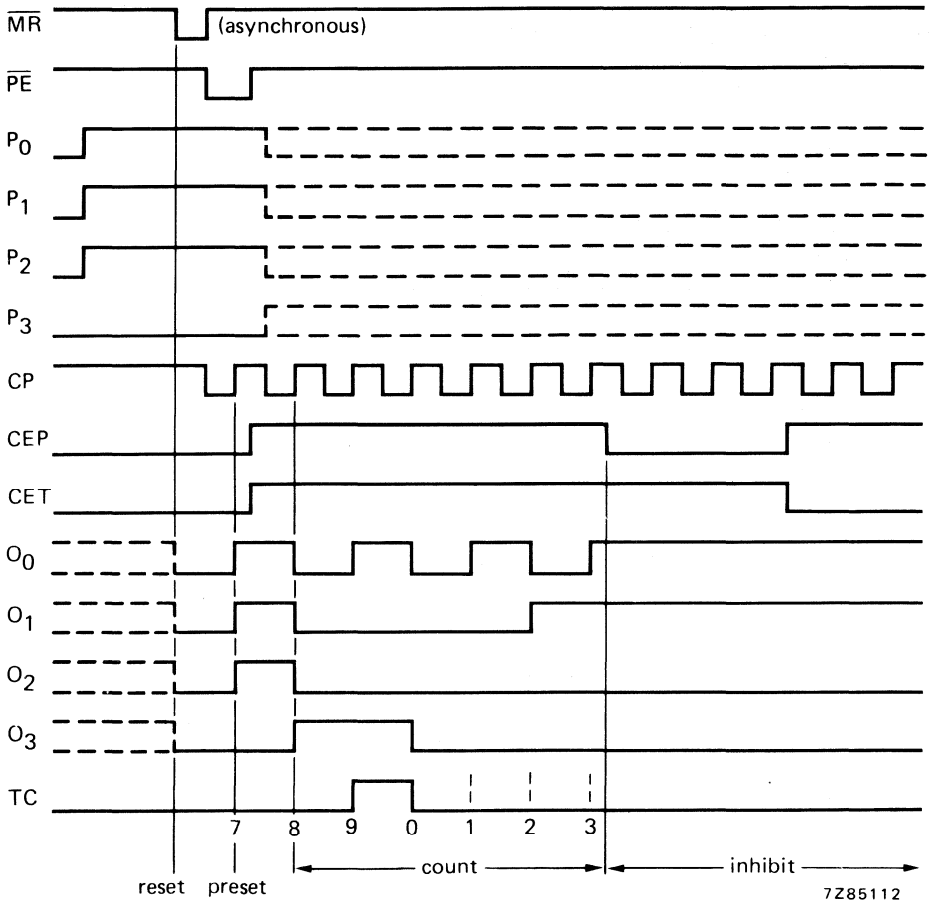
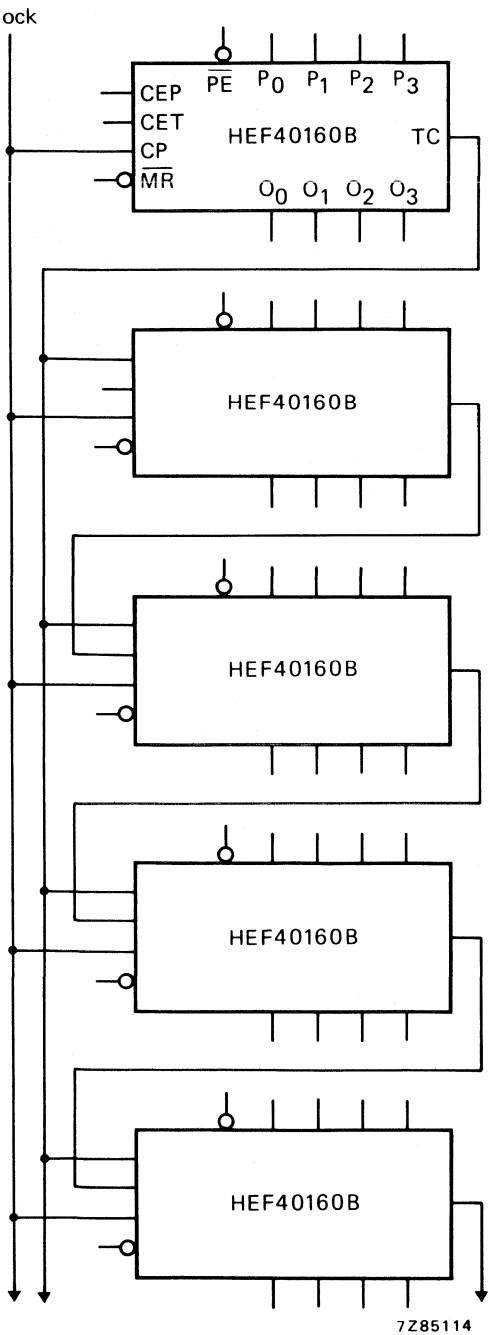


Fig. 9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40160B is:

- Programmable decade counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig. 10 Synchronous multi-stage counting scheme.

4-BIT SYNCHRONOUS BINARY COUNTER WITH ASYNCHRONOUS RESET

The HEF40161B is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), an overriding asynchronous master reset (MR), four parallel data inputs (P_0 to P_3), three synchronous mode control inputs (parallel enable (PE), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous (except for the $\overline{MR}$ input) and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 regardless of the levels of CEP and CET inputs.

When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise, no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_1 to O_3 = HIGH) and when CET is HIGH. A LOW on $\overline{MR}$ sets all outputs (O_0 to O_3 and TC) LOW, independent of the state of all other inputs. Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET and $\overline{PE}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.

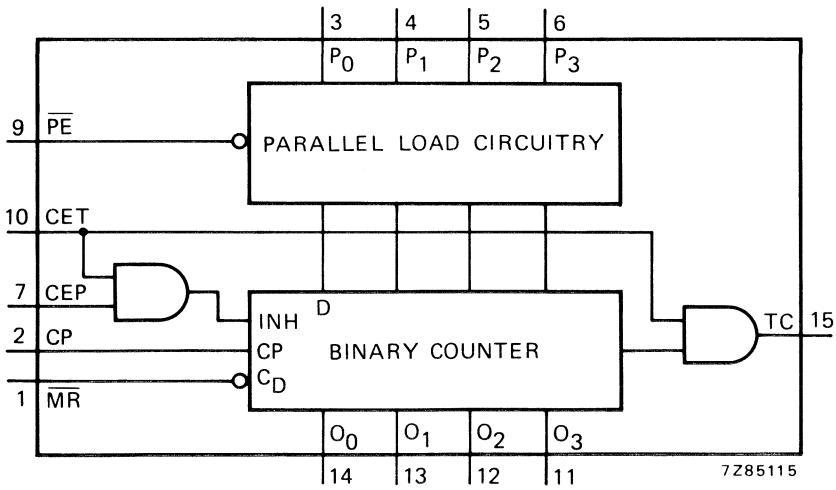


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI | see Family Specifications

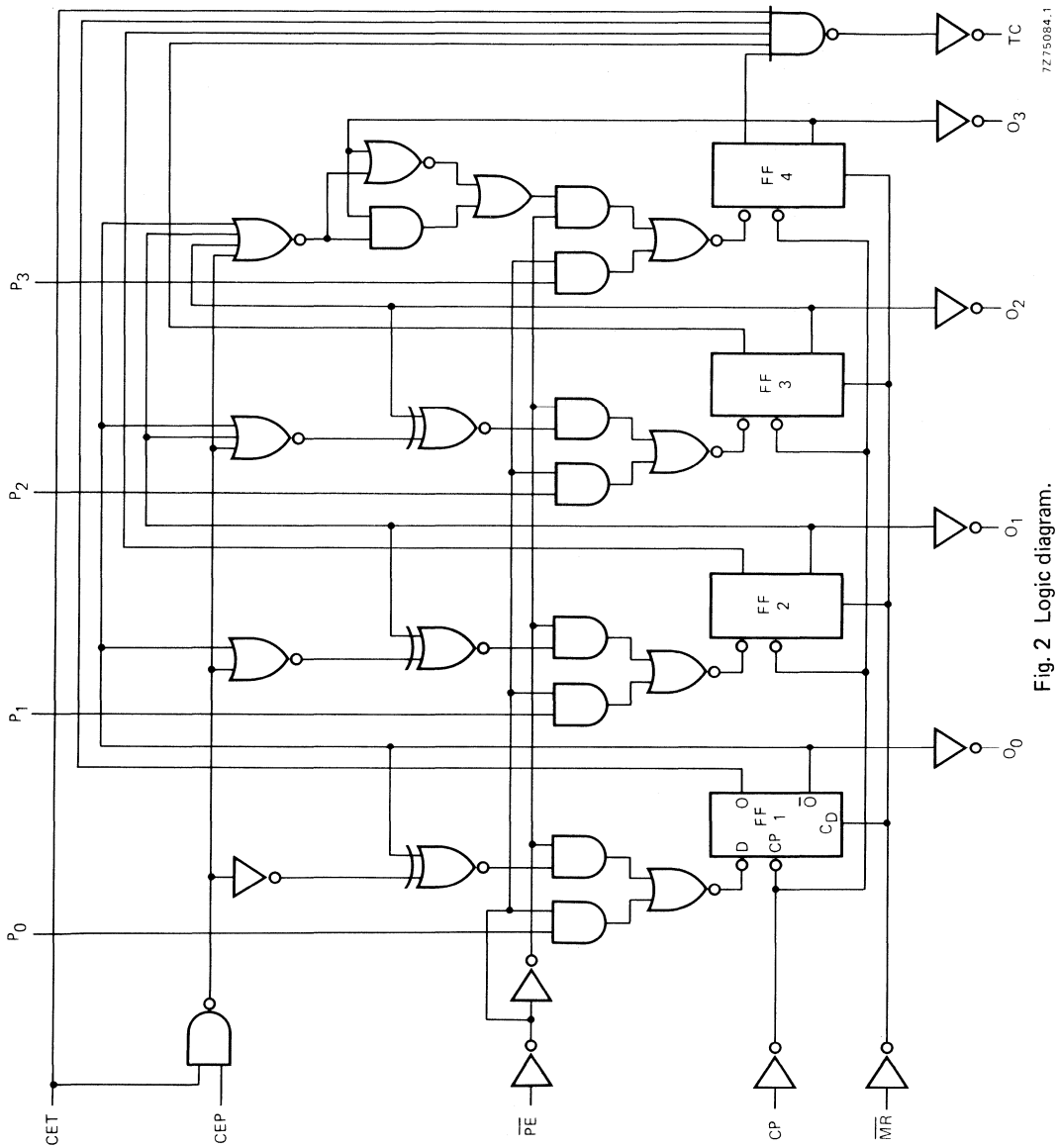


Fig. 2 Logic diagram.

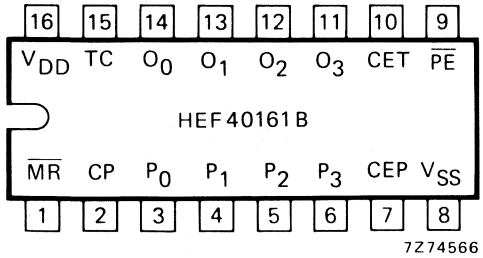


Fig. 3 Pinning diagram.

HEF40161BP : 16-lead DIL; plastic (SOT-38Z).
HEF40161BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40161BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

SYNCHRONOUS MODE SELECTION

$\overline{PE}$	CEP	CET	mode
L	X	X	preset
H	L	X	no change
H	X	L	no change
H	H	H	count

$\overline{MR}$ = HIGH

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot O_1 \cdot O_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3$

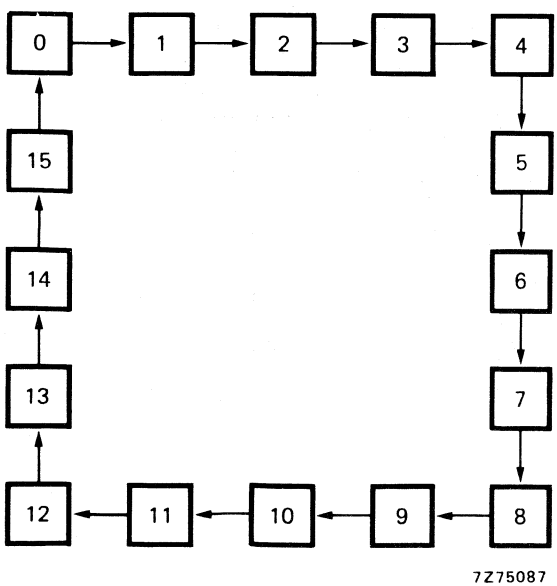


Fig. 4 State diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 200 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5 600 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	16 000 f_i + Σ($f_o C_L$) x V_{DD}^2	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET → TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			120	245	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → TC	5			145	295	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	85	ns	37 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms Figs 5, 6, 7 and 8
	10		40	20		ns	
	15		30	15		ns	
Minimum $\overline{MR}$ pulse width; LOW	5	t_{WMRL}	100	50		ns	
	10		40	20		ns	
	15		30	15		ns	
Recovery time for $\overline{MR}$	5	t_{RMR}	25	0		ns	
	10		15	0		ns	
	15		10	0		ns	
Set-up times $P_n \longrightarrow CP$	5	t_{su}	110	55		ns	
	10		40	20		ns	
	15		30	15		ns	
$\overline{PE} \longrightarrow CP$	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
CEP, CET $\longrightarrow$ CP	5	t_{su}	260	130		ns	
	10		100	50		ns	
	15		70	35		ns	
Hold times $P_n \longrightarrow CP$	5	t_{hold}	20	−35		ns	
	10		10	−10		ns	
	15		5	−10		ns	
$\overline{PE} \longrightarrow CP$	5	t_{hold}	15	−45		ns	
	10		5	−15		ns	
	15		5	−10		ns	
CEP, CET $\longrightarrow$ CP	5	t_{hold}	25	−105		ns	
	10		15	−35		ns	
	15		10	−25		ns	
Maximum clock pulse frequency	5	f_{max}	2,5	5		MHz	
	10		7	14		MHz	
	15		9	18		MHz	

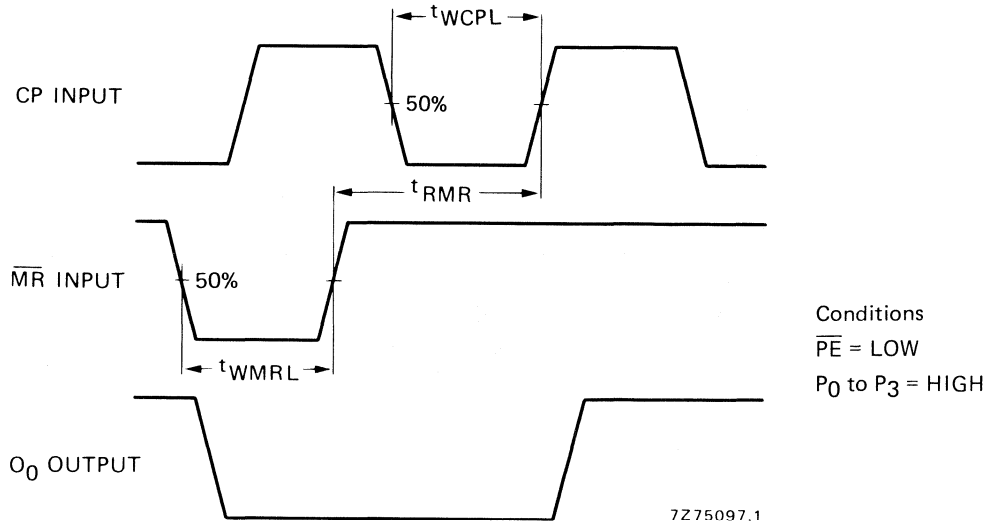


Fig. 5 Waveforms showing minimum CP and $\overline{MR}$ pulse widths and $\overline{MR}$ to CP recovery time.

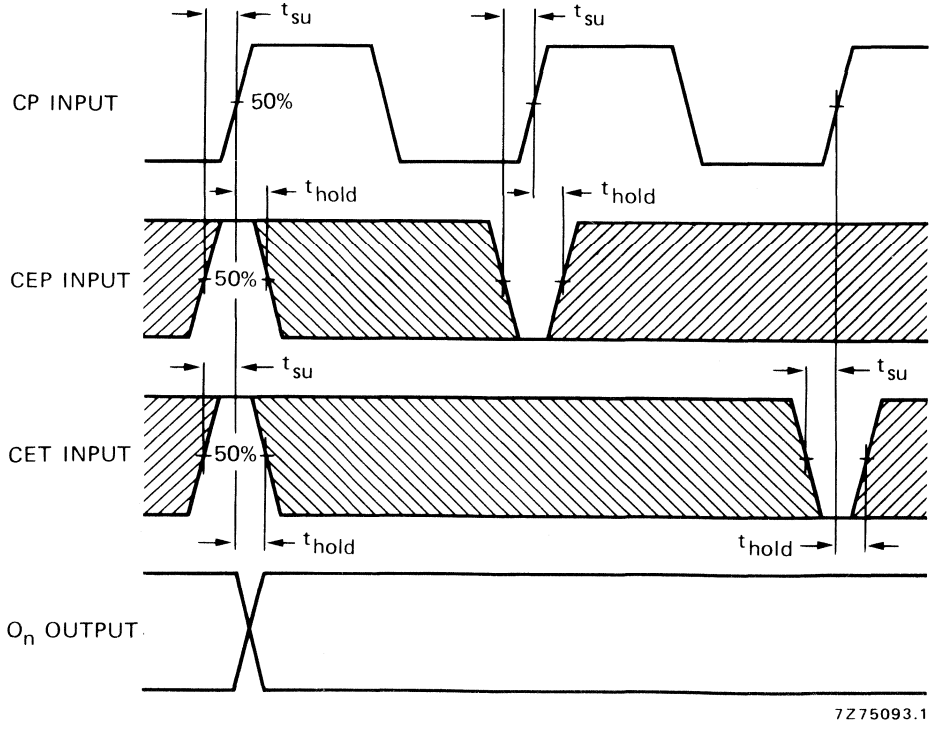
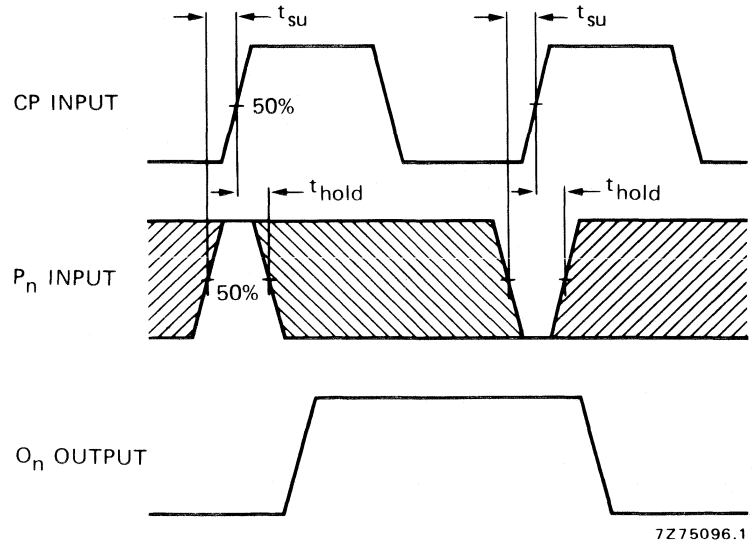
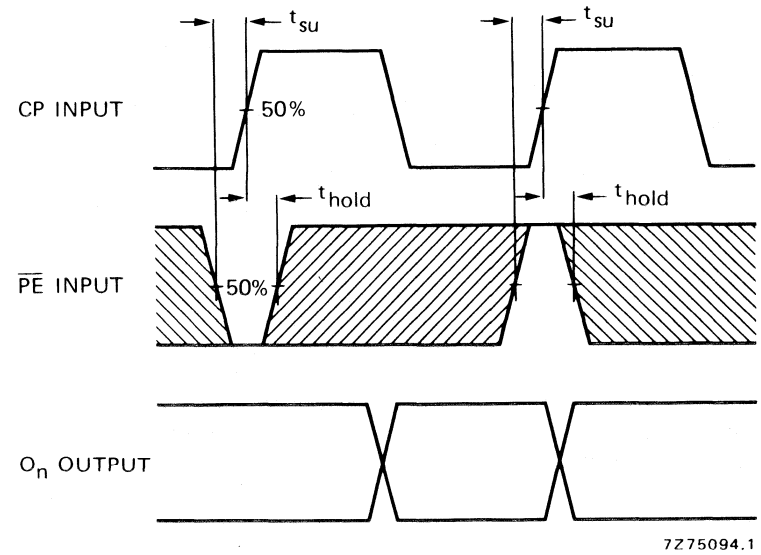


Fig. 6 Waveforms showing set-up times and hold times for CEP and CET inputs.
Condition: $\overline{PE}$ = $\overline{MR}$ = HIGH.



Conditions
$\overline{PE}$ = LOW
$\overline{MR}$ = HIGH

Fig. 7 Waveforms showing set-up times and hold times for P_n inputs.



Condition
$\overline{MR}$ = HIGH

Fig. 8 Waveforms showing set-up times and hold times for $\overline{PE}$ input.

Note
Set-up and hold times are shown as positive values but may be specified as negative values.

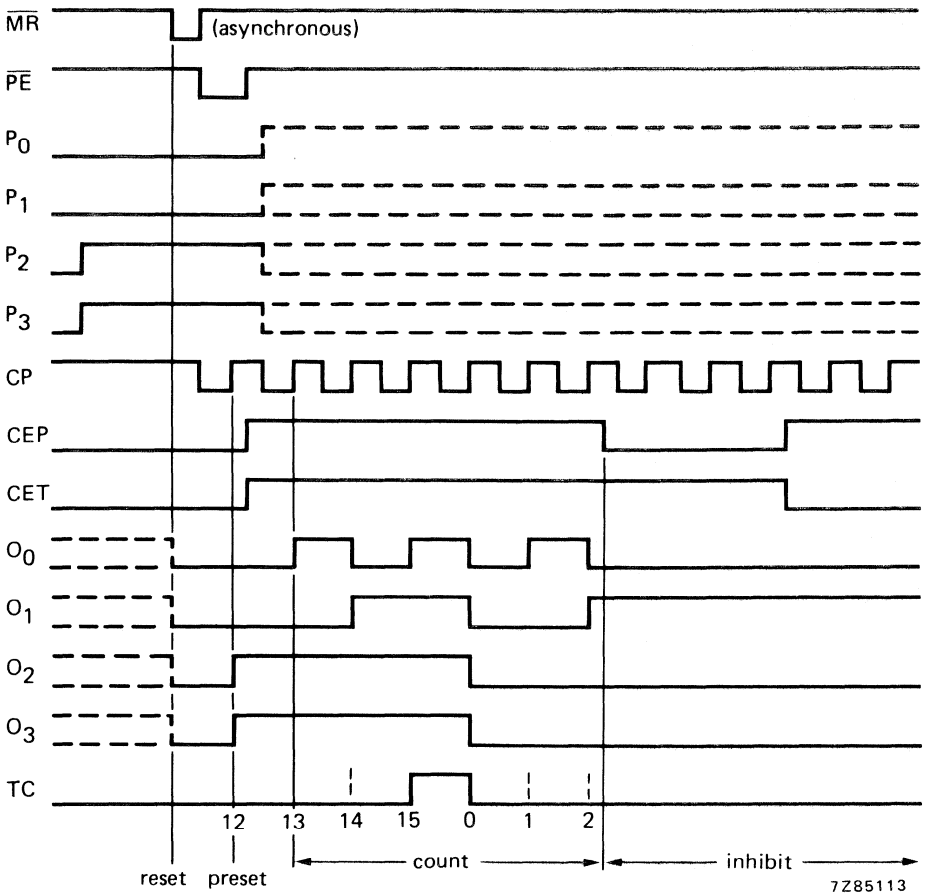
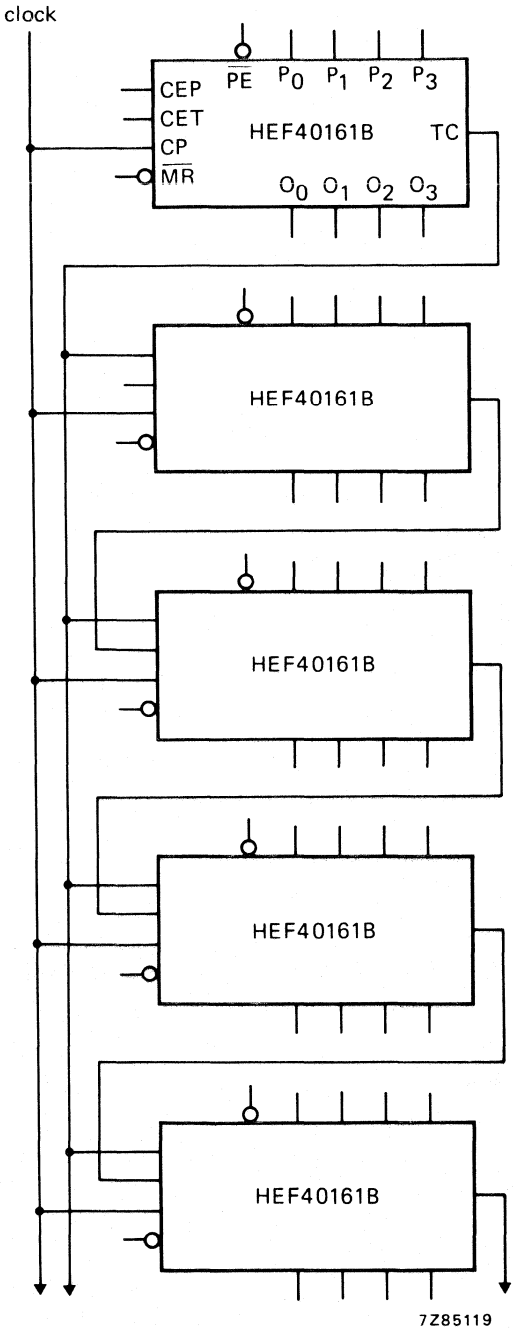


Fig. 9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40161B is:

- Programmable binary counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig. 10 Synchronous multi-stage counting scheme.

4-BIT SYNCHRONOUS DECADE COUNTER WITH SYNCHRONOUS RESET

The HEF40162B is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), four synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP), count enable trickle (CET) and synchronous reset ($\overline{SR}$)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is synchronous and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3. When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise no change occurs in the state of the counter. TC is HIGH when the state of the counter is 9 ($O_0 = O_3$ = HIGH, $O_1 = O_2$ = LOW) and when CET is HIGH. A LOW on $\overline{SR}$ sets all outputs (O_0 to O_3 and TC) LOW on the next LOW to HIGH transition of CP, independent of the state of all other synchronous mode control inputs (CEP, CET and $\overline{PE}$). Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET, $\overline{PE}$ and $\overline{SR}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.

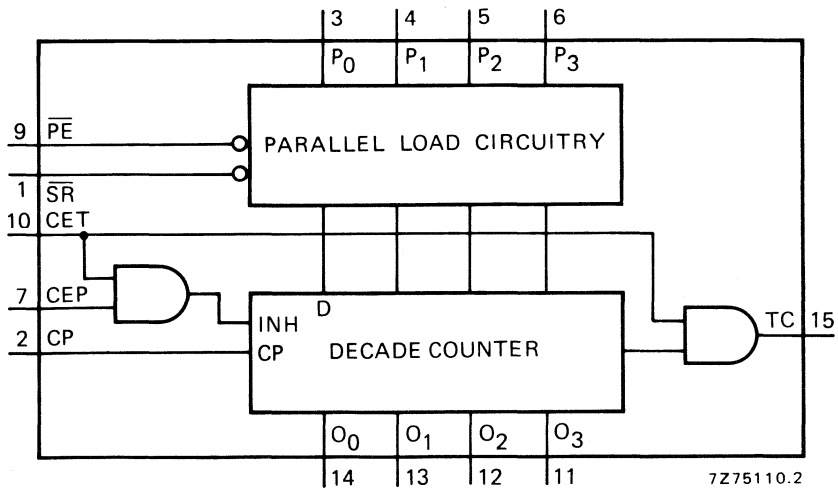


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

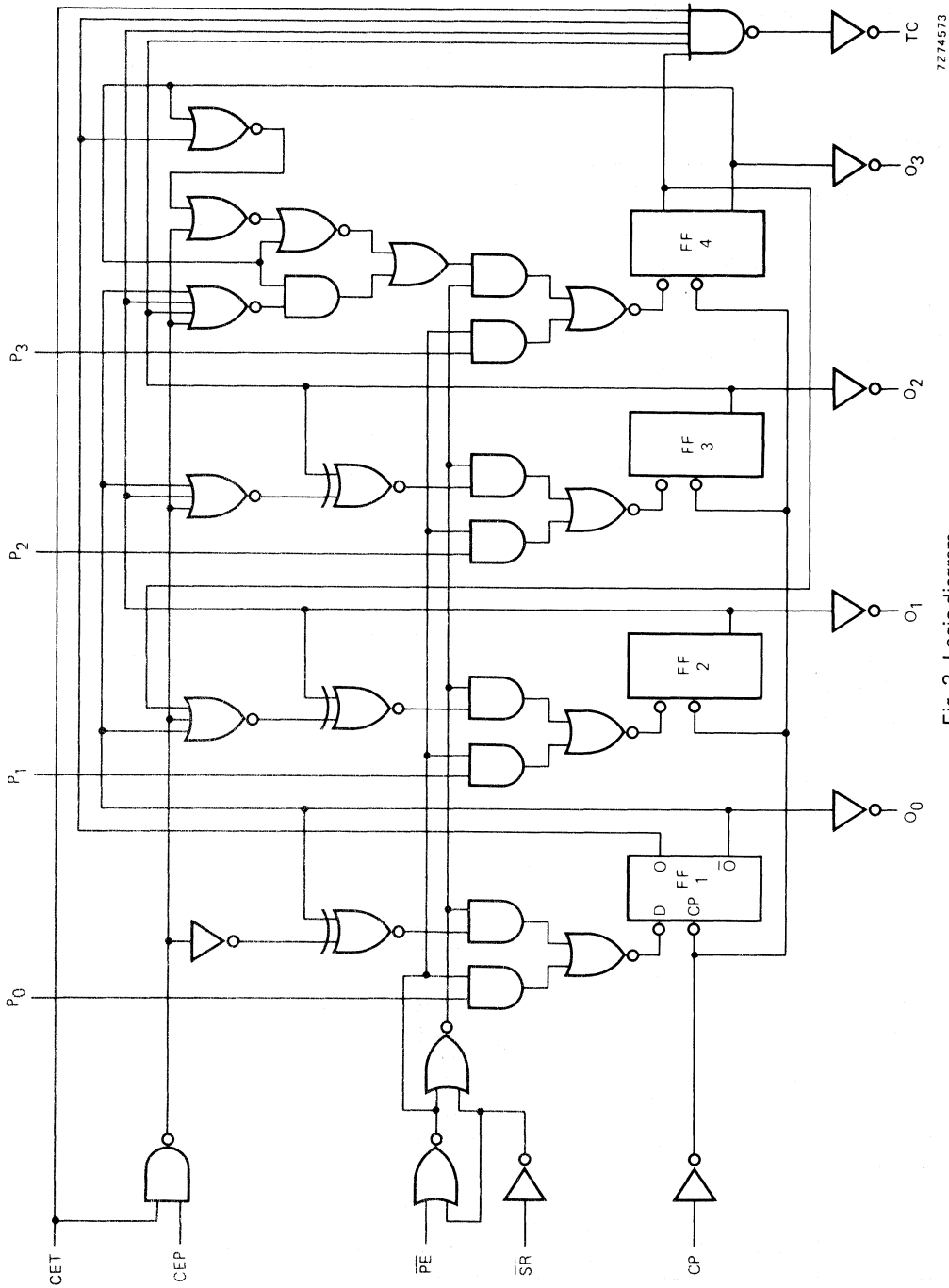


Fig. 2 Logic diagram.

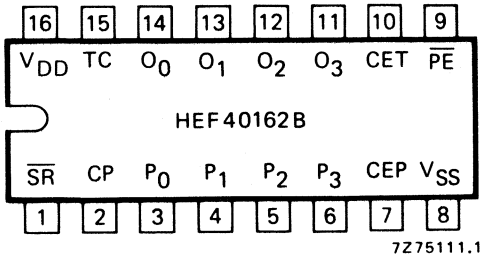


Fig. 3 Pinning diagram.

PINNING

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{SR}$	synchronous reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

HEF40162BP : 16-lead DIL; plastic (SOT-38Z).
HEF40162BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40162BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

SYNCHRONOUS MODE SELECTION

$\overline{SR}$	$\overline{PE}$	CEP	CET	mode
H	L	X	X	preset
H	H	L	X	no change
H	H	X	L	no change
H	H	H	H	count
L	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3$

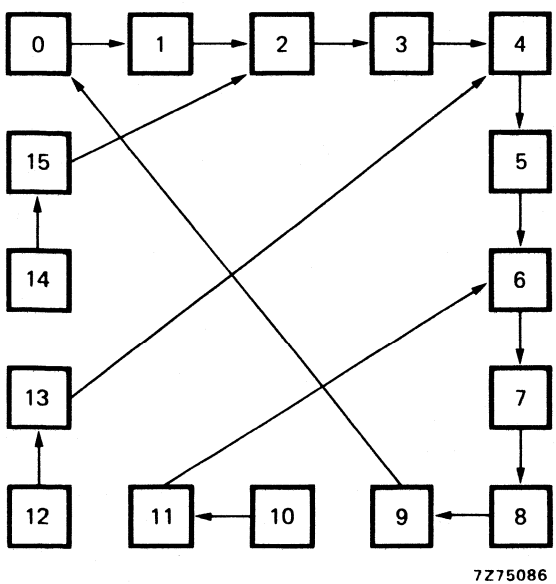


Fig. 4 State diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

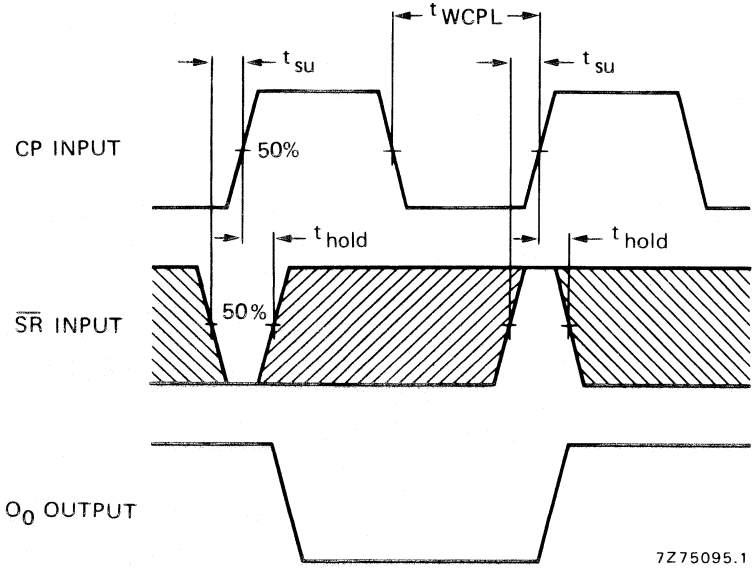
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET → TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms Figs 5, 6, 7 and 8
	10		40	20		ns	
	15		30	15		ns	
Set-up times							
$P_n \rightarrow CP$	5	t_{su}	110	55		ns	
	10		40	20		ns	
	15		30	15		ns	
$\overline{PE} \rightarrow CP$	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
CEP, CET $\rightarrow$ CP	5	t_{su}	260	130		ns	
	10		100	50		ns	
	15		70	35		ns	
$\overline{SR} \rightarrow CP$	5	t_{su}	50	25		ns	
	10		20	10		ns	
	15		15	10		ns	
Hold times							
$P_n \rightarrow CP$	5	t_{hold}	20	−35		ns	
	10		10	−10		ns	
	15		5	−10		ns	
$\overline{PE} \rightarrow CP$	5	t_{hold}	15	−45		ns	
	10		5	−15		ns	
	15		5	−10		ns	
CEP, CET $\rightarrow$ CP	5	t_{hold}	25	−105		ns	
	10		15	−35		ns	
	15		10	−25		ns	
$\overline{SR} \rightarrow CP$	5	t_{hold}	15	−10		ns	
	10		5	−5		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5	f_{max}	2,5	5		MHz	
	10		7	14		MHz	
	15		9	18		MHz	



Conditions
$\overline{PE}$ = LOW
P_0 to P_3 = HIGH

Fig. 5 Waveforms showing set-up times and hold times for $\overline{SR}$ input and minimum CP pulse width.

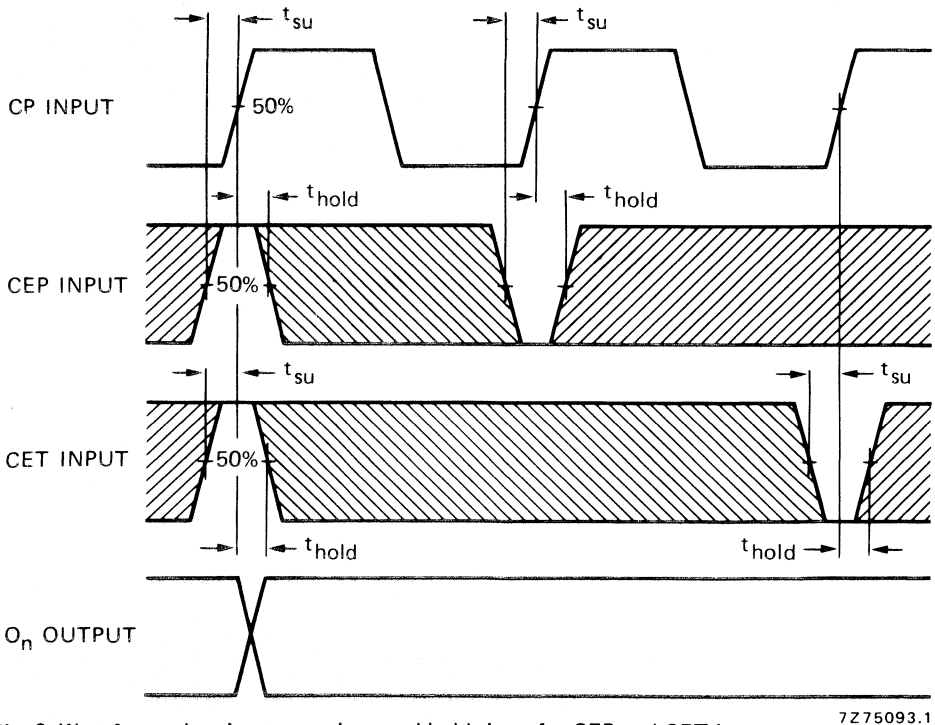


Fig. 6 Waveforms showing set-up times and hold times for CEP and CET inputs.

Condition: $\overline{PE}$ = $\overline{SR}$ = HIGH.

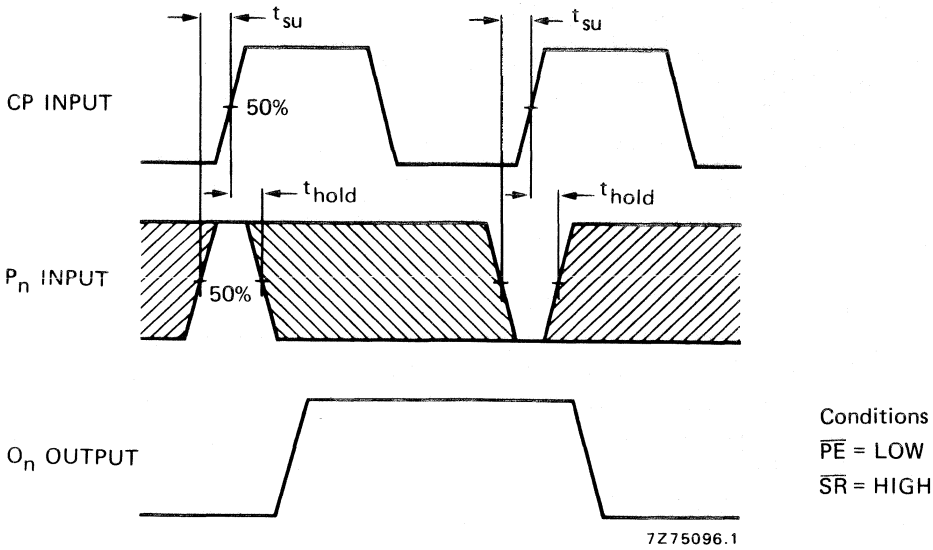


Fig. 7 Waveforms showing set-up times and hold times for P_n inputs.

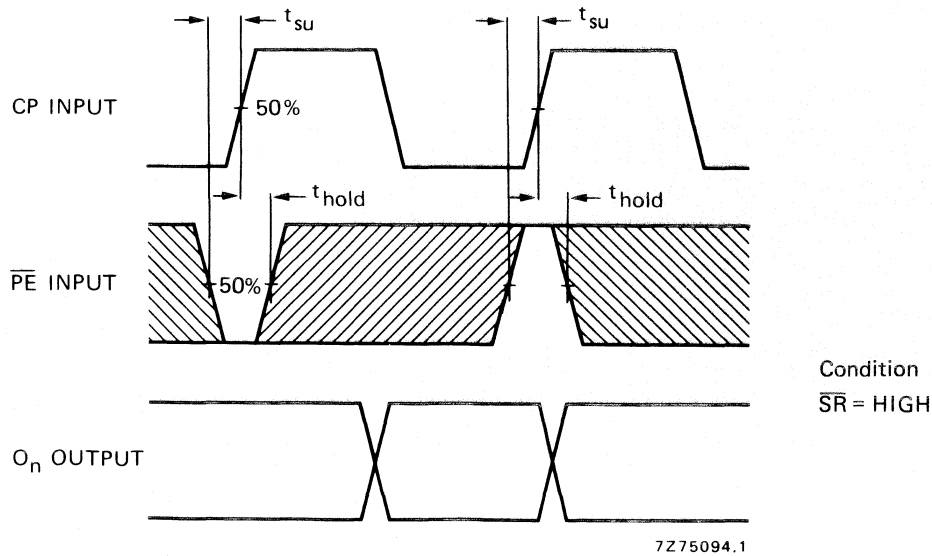


Fig. 8 Waveforms showing set-up times and hold times for $\overline{PE}$ input.

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

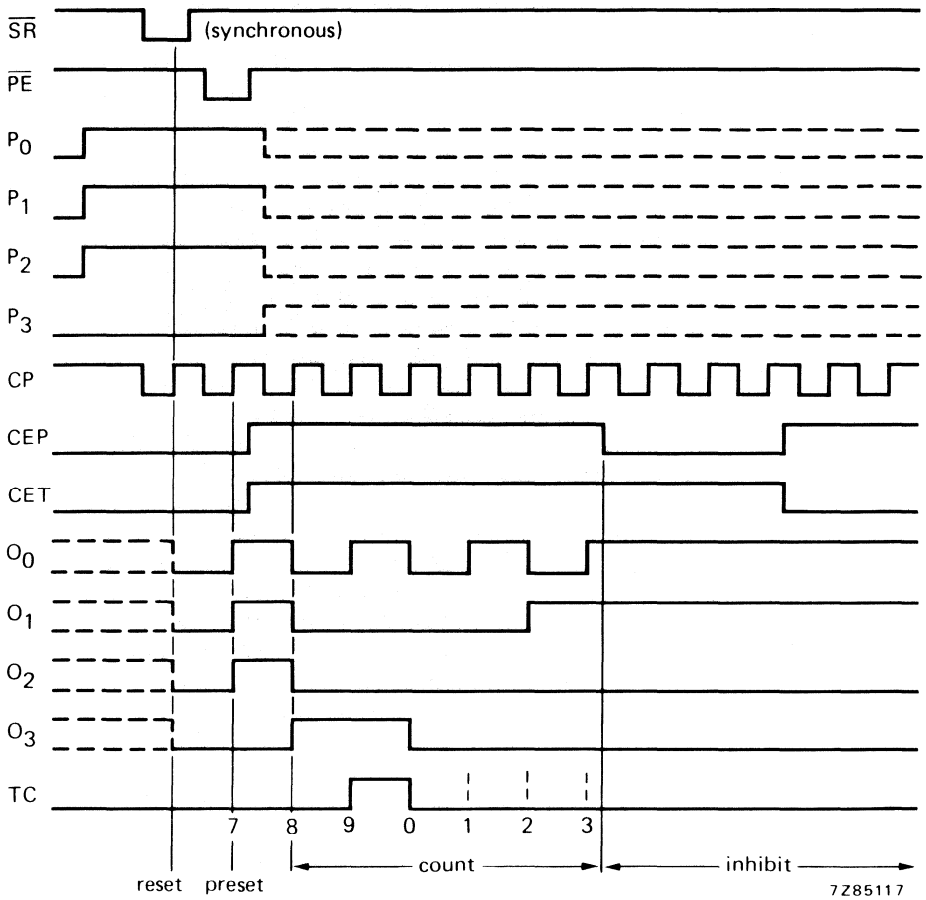
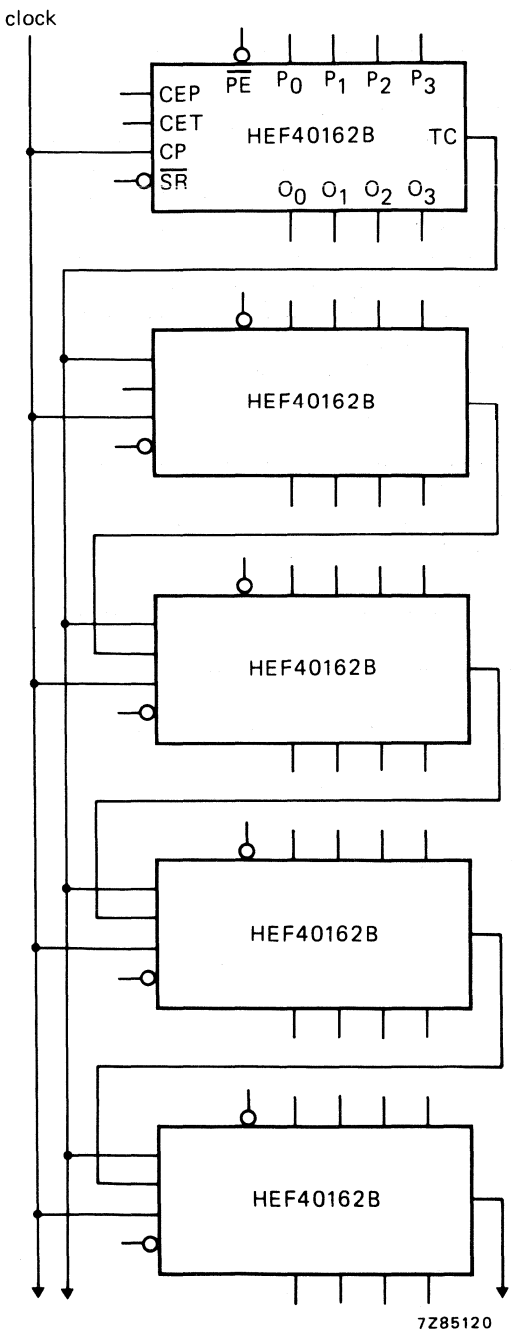


Fig. 9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40162B is:

- Programmable decade counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig. 10 Synchronous multi-stage counting scheme.

4-BIT SYNCHRONOUS BINARY COUNTER WITH SYNCHRONOUS RESET

The HEF40163B is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), four synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP), count enable trickle (CET) and synchronous reset ($\overline{SR}$)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3. When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_0 to O_3 = HIGH) and when CET is HIGH. A LOW on $\overline{SR}$ sets all outputs (O_0 to O_3 and TC) LOW on the next LOW to HIGH transition of CP, independent of the state of all other synchronous mode control inputs (CEP, CET and $\overline{PE}$). Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET, $\overline{PE}$ and $\overline{SR}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.

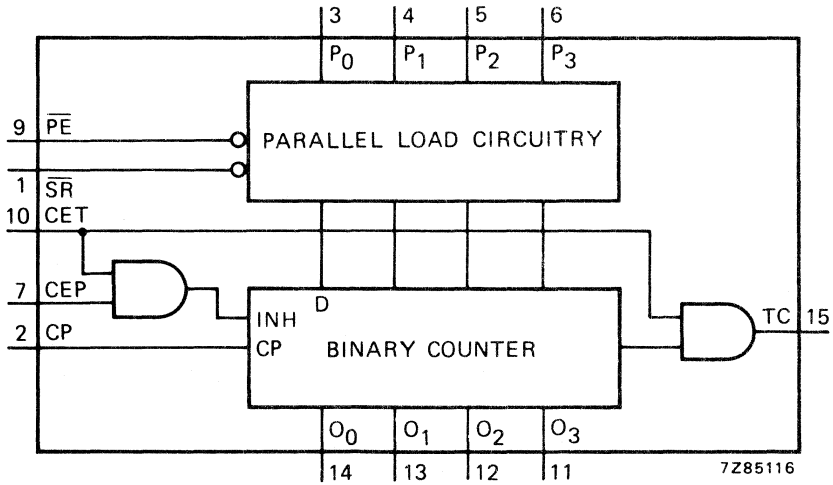


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

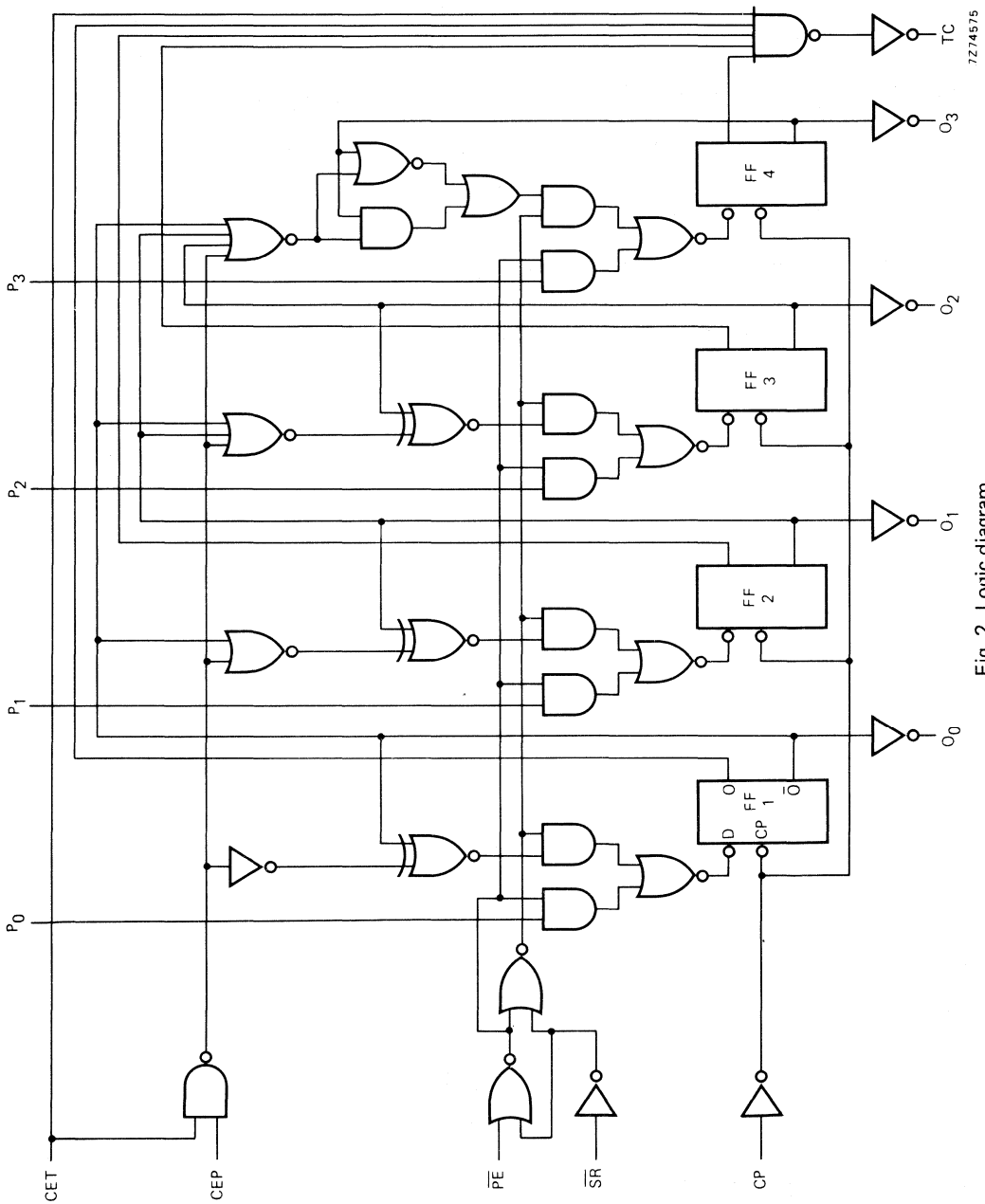


Fig. 2 Logic diagram.

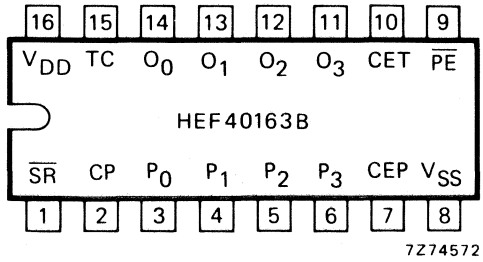


Fig. 3 Pinning diagram.

PINNING

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{SR}$	synchronous reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

HEF40163BP : 16-lead DIL; plastic (SOT-38Z).
HEF40163BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40163BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

SYNCHRONOUS MODE SELECTION

$\overline{SR}$	$\overline{PE}$	CEP	CET	mode
H	L	X	X	preset
H	H	L	X	no change
H	H	X	L	no change
H	H	H	H	count
L	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot O_1 \cdot O_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3$

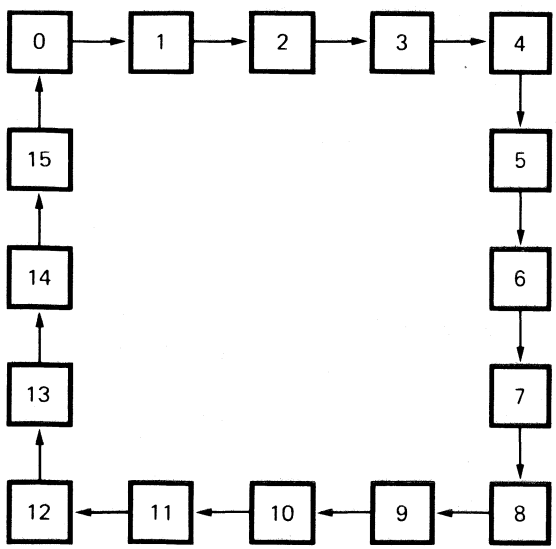


Fig. 4 State diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET → TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms Figs 5, 6, 7 and 8
	10		40	20		ns	
	15		30	15		ns	
Set-up times							
P_n → CP	5	t_{su}	110	55		ns	
	10		40	20		ns	
	15		30	15		ns	
$\overline{PE}$ → CP	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
CEP, CET → CP	5	t_{su}	260	130		ns	
	10		100	50		ns	
	15		70	35		ns	
$\overline{SR}$ → CP	5	t_{su}	50	25		ns	
	10		20	10		ns	
	15		15	10		ns	
Hold times							
P_n → CP	5	t_{hold}	20	−35		ns	
	10		10	−10		ns	
	15		5	−10		ns	
$\overline{PE}$ → CP	5	t_{hold}	15	−45		ns	
	10		5	−15		ns	
	15		5	−10		ns	
CEP, CET → CP	5	t_{hold}	25	−105		ns	
	10		15	−35		ns	
	15		10	−25		ns	
$\overline{SR}$ → CP	5	t_{hold}	15	−10		ns	
	10		5	−5		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5	f_{max}	2,5	5		MHz	
	10		7	14		MHz	
	15		9	18		MHz	

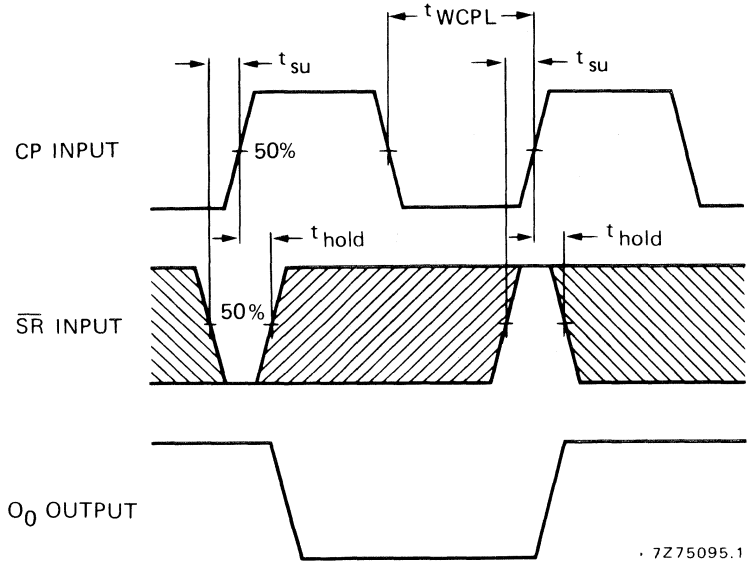


Fig. 5 Waveforms showing set-up and hold times for $\overline{SR}$ input and minimum CP pulse width.

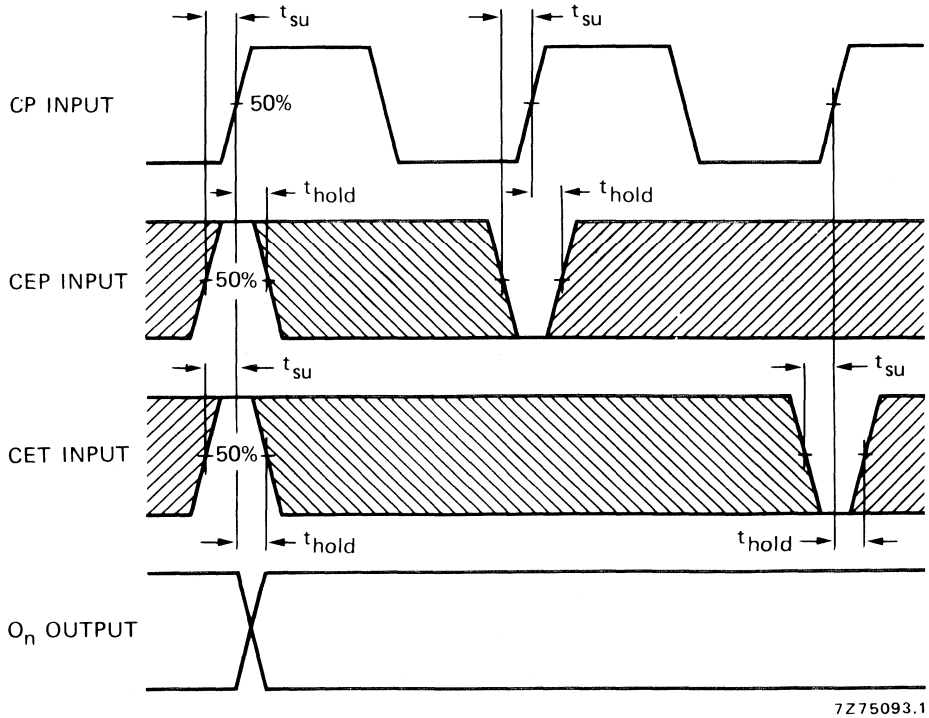


Fig. 6 Waveforms showing set-up times and hold times for CEP and CET inputs.
Condition: $\overline{PE}$ = $\overline{SR}$ = HIGH.

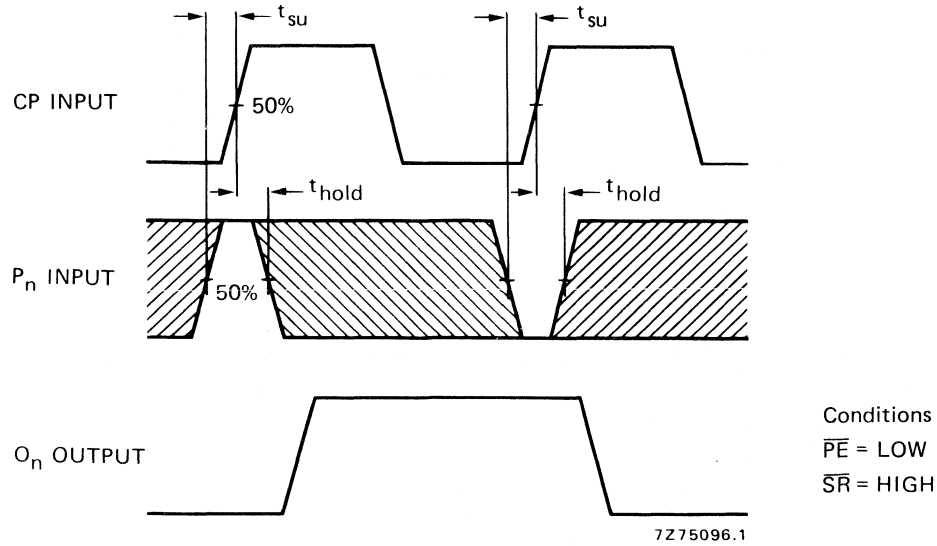


Fig. 7 Waveforms showing set-up times and hold times for P_n inputs.

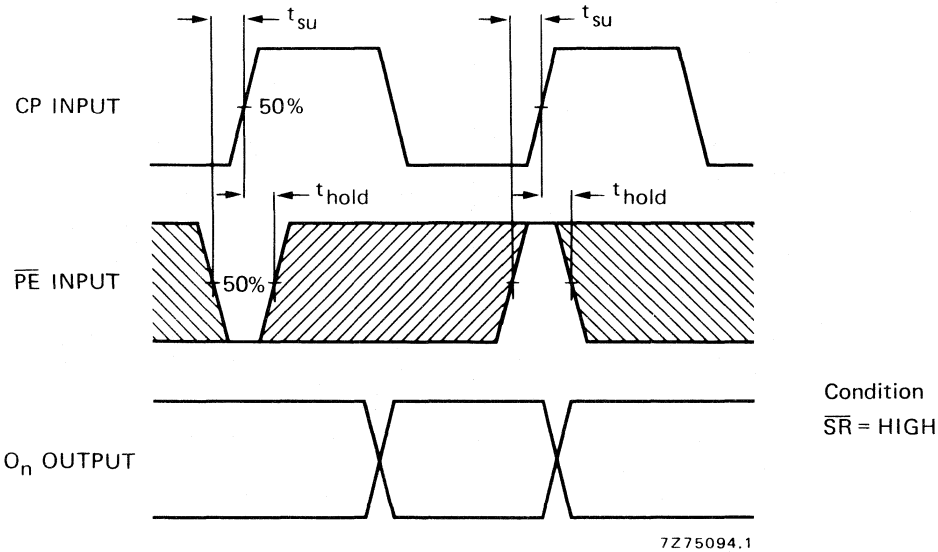


Fig. 8 Waveforms showing set-up times and hold times for $\overline{PE}$ input.

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

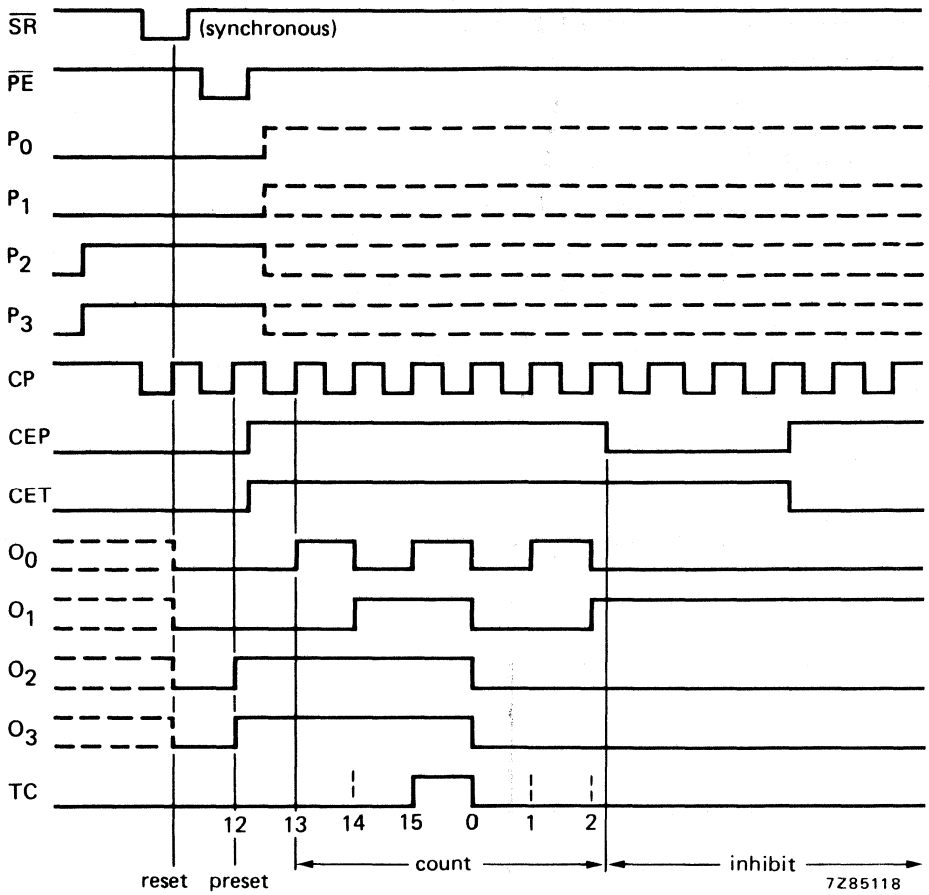
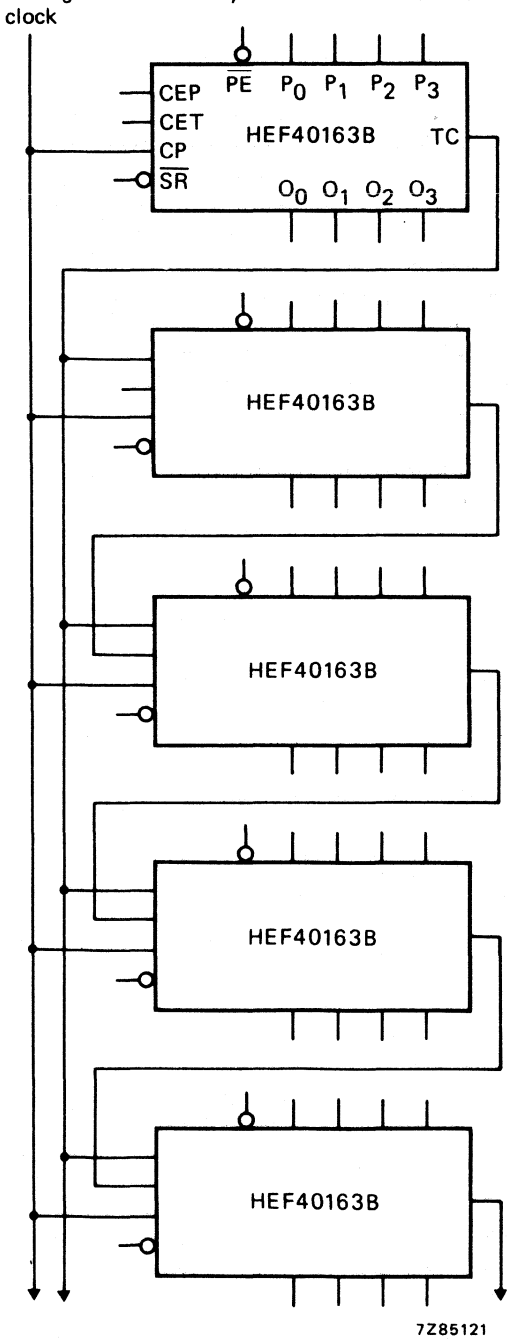


Fig. 9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40163B is:

- Programmable binary counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig. 10 Synchronous multi-stage counting scheme.

HEX D-TYPE FLIP-FLOP

The HEF40174B is a hex edge-triggered D-type flip-flop with six data inputs (D_0 to D_5), a clock input (CP), an overriding asynchronous master reset input ($\overline{MR}$), and six buffered outputs (O_0 to O_5). Information on D_0 to D_5 is transferred to O_0 to O_5 on the LOW to HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to O_5 = LOW) independent of CP and D_0 to D_5.

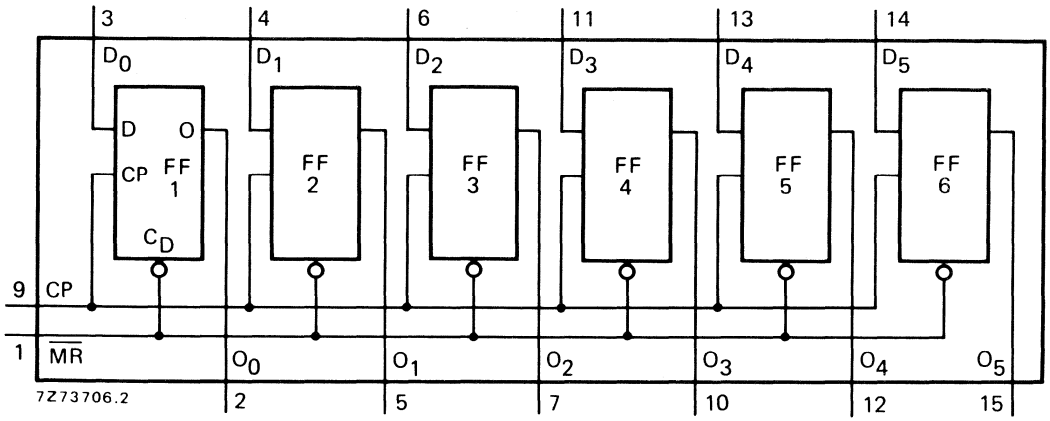


Fig. 1 Functional diagram.

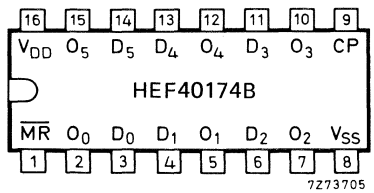


Fig. 2 Pinning diagram.

HEF40174BP: 16-lead DIL; plastic (SOT-38Z).
HEF40174BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40174BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA } see Family Specifications

I_{DD} LIMITS category MSI }

PINNING

D_0 to D_5	data inputs
CP	clock input (LOW to HIGH; edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_5	buffered outputs

FUNCTION TABLE

inputs			output
CP	D	$\overline{MR}$	O
⎍	H	H	H
⎍	L	H	L
⎎	X	H	no change
X	X	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
⎍ = positive-going transition
⎎ = negative-going transition

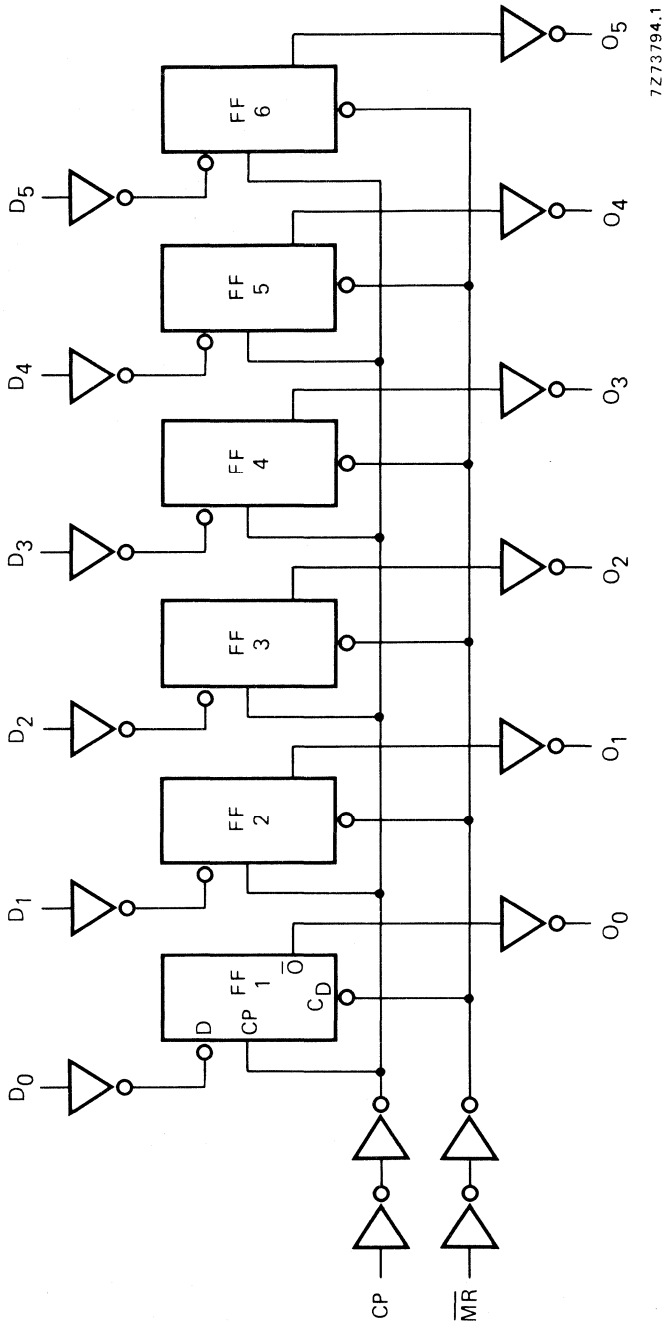


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			75	155	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			20	45	ns	12 ns + (0,16 ns/pF) C_L
	5			75	155	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			20	45	ns	12 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			85	175	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		20	10		ns	see also waveforms Fig. 4
D_n → CP	10	t_{su}	10	5		ns	
	15		10	5		ns	
Hold time	5		10	0		ns	
D_n → CP	10	t_{hold}	5	0		ns	
	15		5	0		ns	
Minimum clock pulse width; LOW	5		70	35		ns	
	10	t_{WCPL}	30	15		ns	
	15		20	10		ns	
Minimum $\overline{MR}$ pulse width; LOW	5		70	35		ns	
	10	t_{WMRL}	35	15		ns	
	15		25	10		ns	
Recovery time for $\overline{MR}$	5		45	25		ns	
	10	t_{RMR}	20	10		ns	
	15		15	5		ns	
Maximum clock pulse frequency	5		5	11		MHz	
	10	f_{max}	15	30		MHz	
	15		20	45		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	3500 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	16 000 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	
	15	42 000 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	

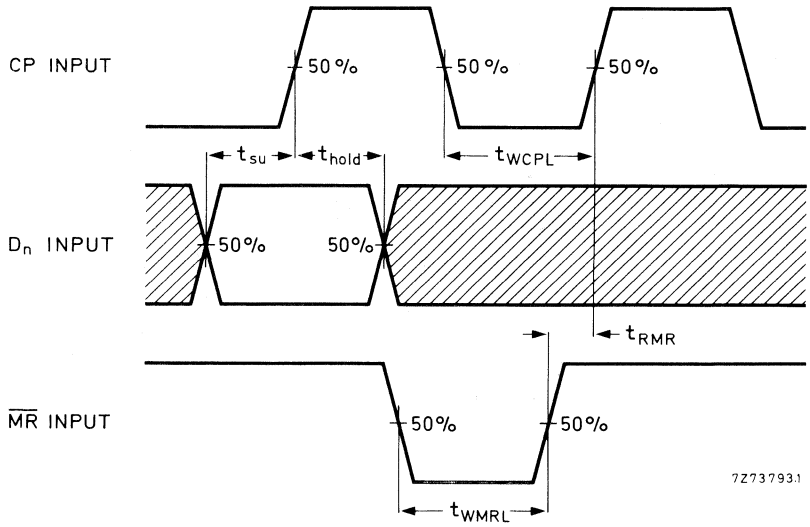


Fig. 4 Waveforms showing minimum pulse widths for CP and $\overline{MR}$, $\overline{MR}$ to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40174B are:

- Shift registers
- Buffer/storage register
- Pattern generator

QUADRUPLE D-TYPE FLIP-FLOP

The HEF40175B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), a clock input (CP), an overriding asynchronous master reset input ($\overline{MR}$), four buffered outputs (O_0 to O_3), and four complementary buffered outputs ($\overline{O}_0$ to $\overline{O}_3$). Information on D_0 to D_3 is transferred to O_0 to O_3 on the LOW to HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to O_3 = LOW, $\overline{O}_0$ to $\overline{O}_3$ = HIGH), independent of CP and D_0 to D_3.

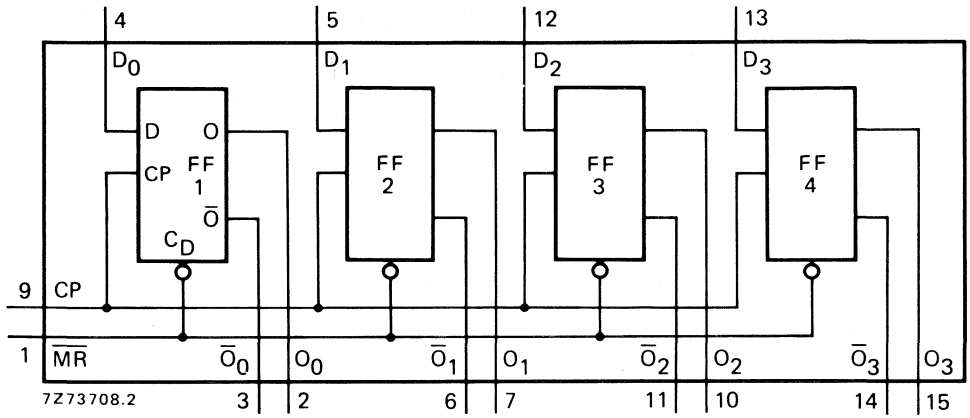


Fig. 1 Functional diagram.

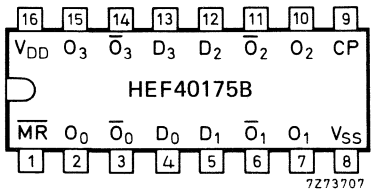


Fig. 2 Pinning diagram.

HEF40175BP: 16-lead DIL; plastic (SOT-38Z).
HEF40175BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40175BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

PINNING

D_0 to D_3	data inputs
CP	clock input (LOW to HIGH; edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	buffered outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary buffered outputs

FUNCTION TABLE

inputs			outputs	
CP	D	$\overline{MR}$	O	$\overline{O}$
↑	H	H	H	L
↑	L	H	L	H
↓	X	H	no change	no change
X	X	L	L	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↑ = positive-going transition
↓ = negative-going transition

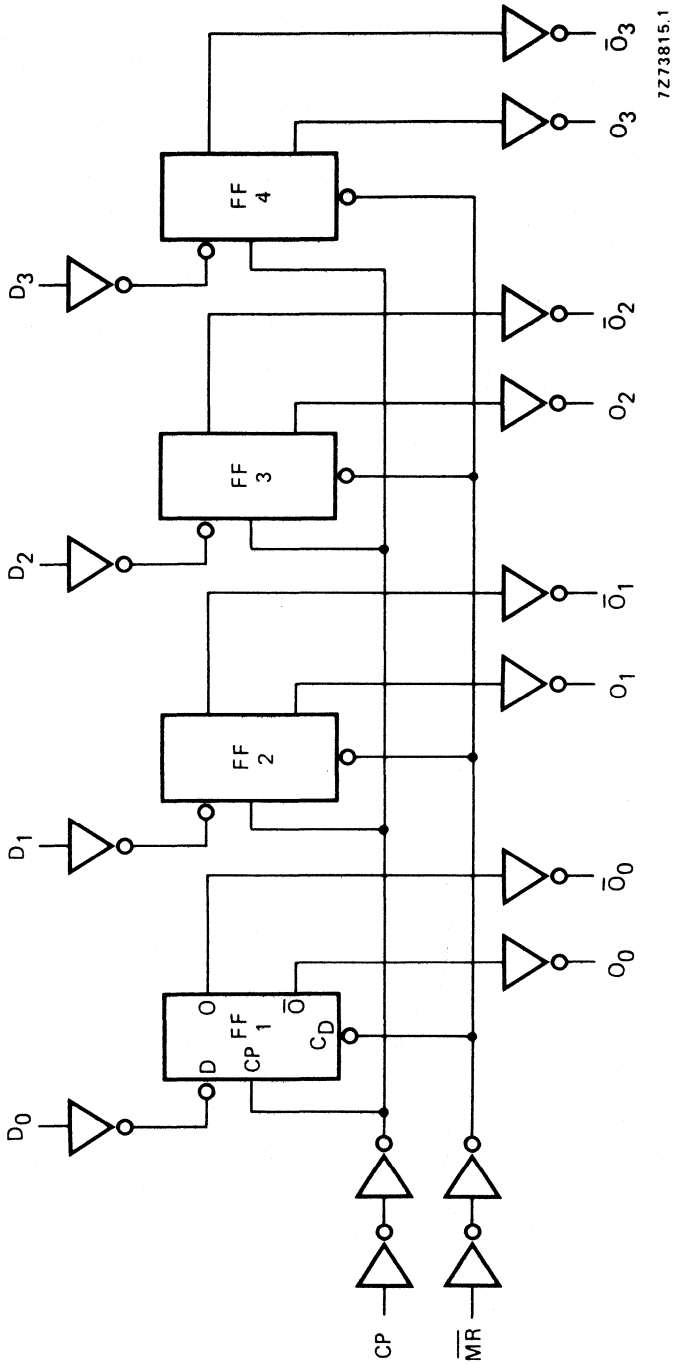


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP ⟶ O_n, $\overline{O}_n$	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
	5			70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			25	45	ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ ⟶ O_n	5			75	155	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ ⟶ $\overline{O}_n$	5			70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		60	30		ns	see also waveforms Fig. 4
D_n ⟶ CP	10	t_{su}	20	10		ns	
	15		15	5		ns	
Hold time	5		25	−5		ns	
D_n ⟶ CP	10	t_{hold}	10	0		ns	
	15		10	0		ns	
Minimum clock	5		90	45		ns	
pulse width; LOW	10	t_{WCPL}	35	15		ns	
	15		25	10		ns	
Minimum $\overline{MR}$ pulse	5		80	40		ns	
width; LOW	10	t_{WMRL}	30	15		ns	
	15		20	10		ns	
Recovery time	5		0	−30		ns	
for $\overline{MR}$	10	t_{RMR}	0	−20		ns	
	15		0	−15		ns	
Maximum clock	5		5	11		MHz	
pulse frequency	10	f_{max}	15	30		MHz	
	15		20	45		MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$8400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$22\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

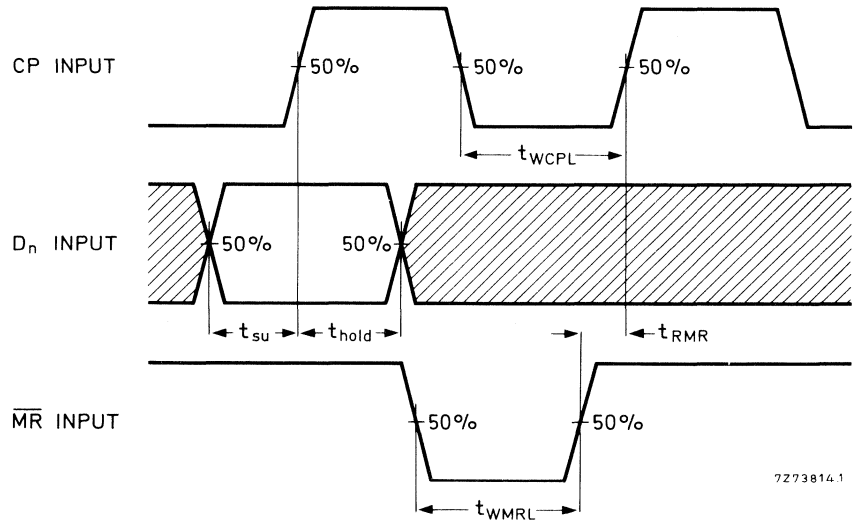


Fig. 4 Waveforms showing minimum pulse widths for CP and $\overline{MR}$, $\overline{MR}$ to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40175B are:

- Shift registers
- Buffer/storage register
- Pattern generator

4-BIT UP/DOWN DECADE COUNTER

The HEF40192B is a 4-bit synchronous up/down decade counter. The counter has a count-up clock input (CP_U), a count-down clock input (CP_D), an asynchronous parallel load input ($\overline{PL}$), four parallel data inputs (P_0 to P_3), an asynchronous master reset input (MR), four counter outputs (O_0 to O_3), an active LOW terminal count-up (carry) output ($\overline{TC}_U$) and an active LOW terminal count-down (borrow) output ($\overline{TC}_D$).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. The outputs $\overline{TC}_U$ and $\overline{TC}_D$ are normally HIGH. When the circuit has reached the maximum count state of '9', the next HIGH to LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again. Likewise, output $\overline{TC}_D$ will go LOW when the circuit is in the zero state and CP_D goes LOW. When $\overline{PL}$ is LOW, the information on P_0 to P_3 is asynchronously loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

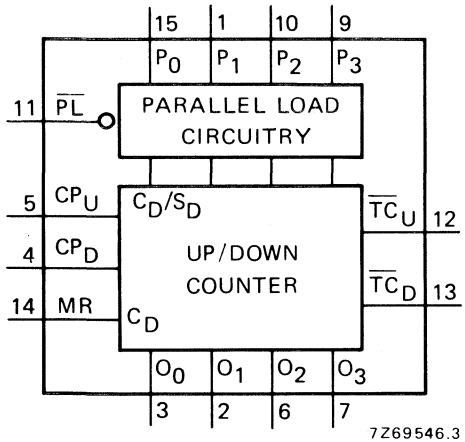


Fig. 1 Functional diagram.

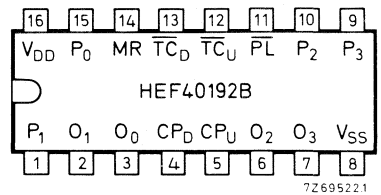


Fig. 2 Pinning diagram.

HEF40192BP : 16-lead DIL; plastic (SOT-38Z).
HEF40192BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40192BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{PL}$	parallel load input (active LOW)
P_0 to P_3	parallel data inputs
CP_U	count-up clock pulse input (LOW to HIGH, edge-triggered)
CP_D	count-down clock pulse input (LOW to HIGH, edge-triggered)
MR	master reset input (asynchronous)
$\overline{TC}_U$	buffered terminal count-up (carry) output (active LOW)
$\overline{TC}_D$	buffered terminal count-down (borrow) output (active LOW)
O_0 to O_3	buffered counter outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

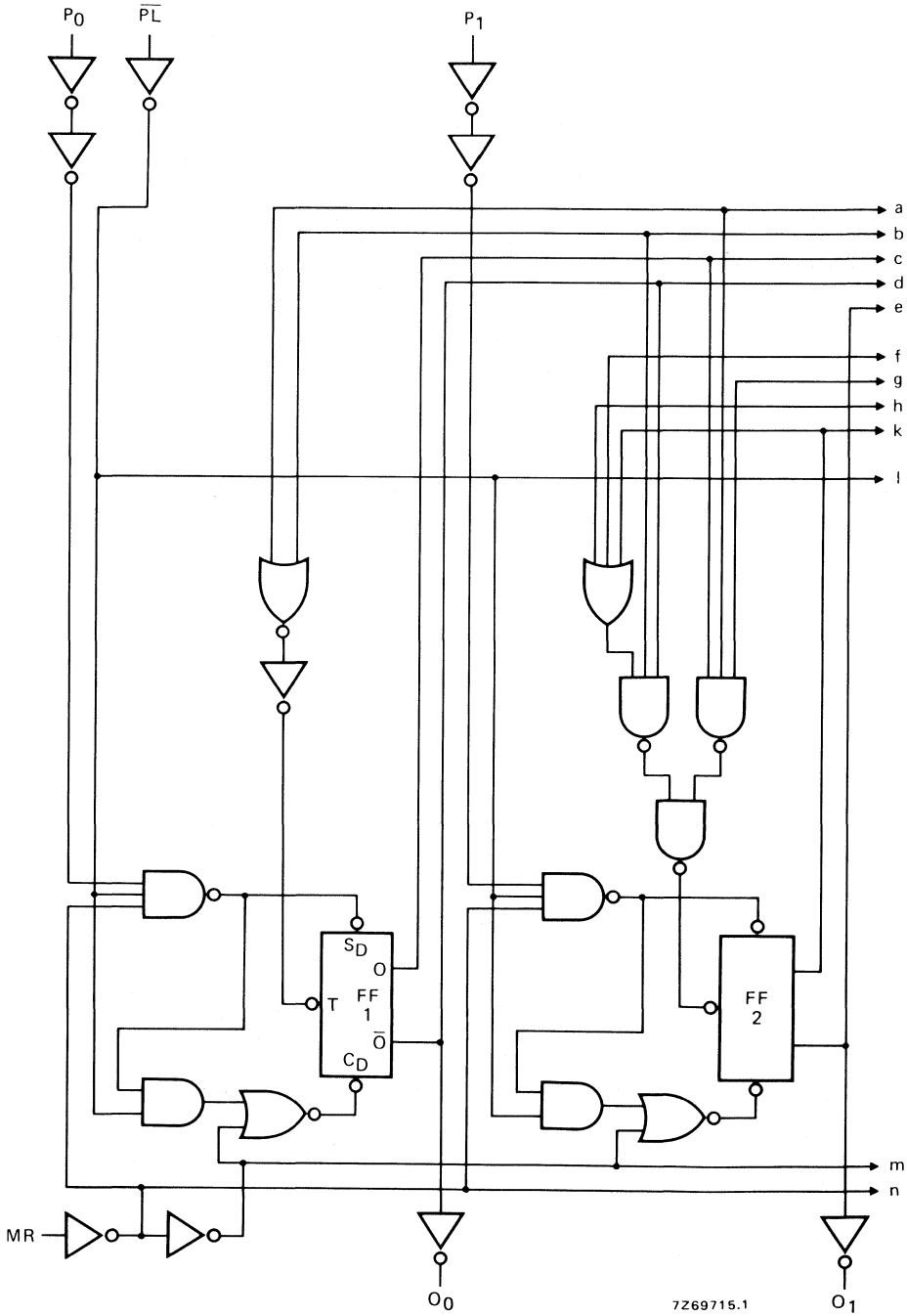


Fig. 3 Logic diagram (continued on next page).

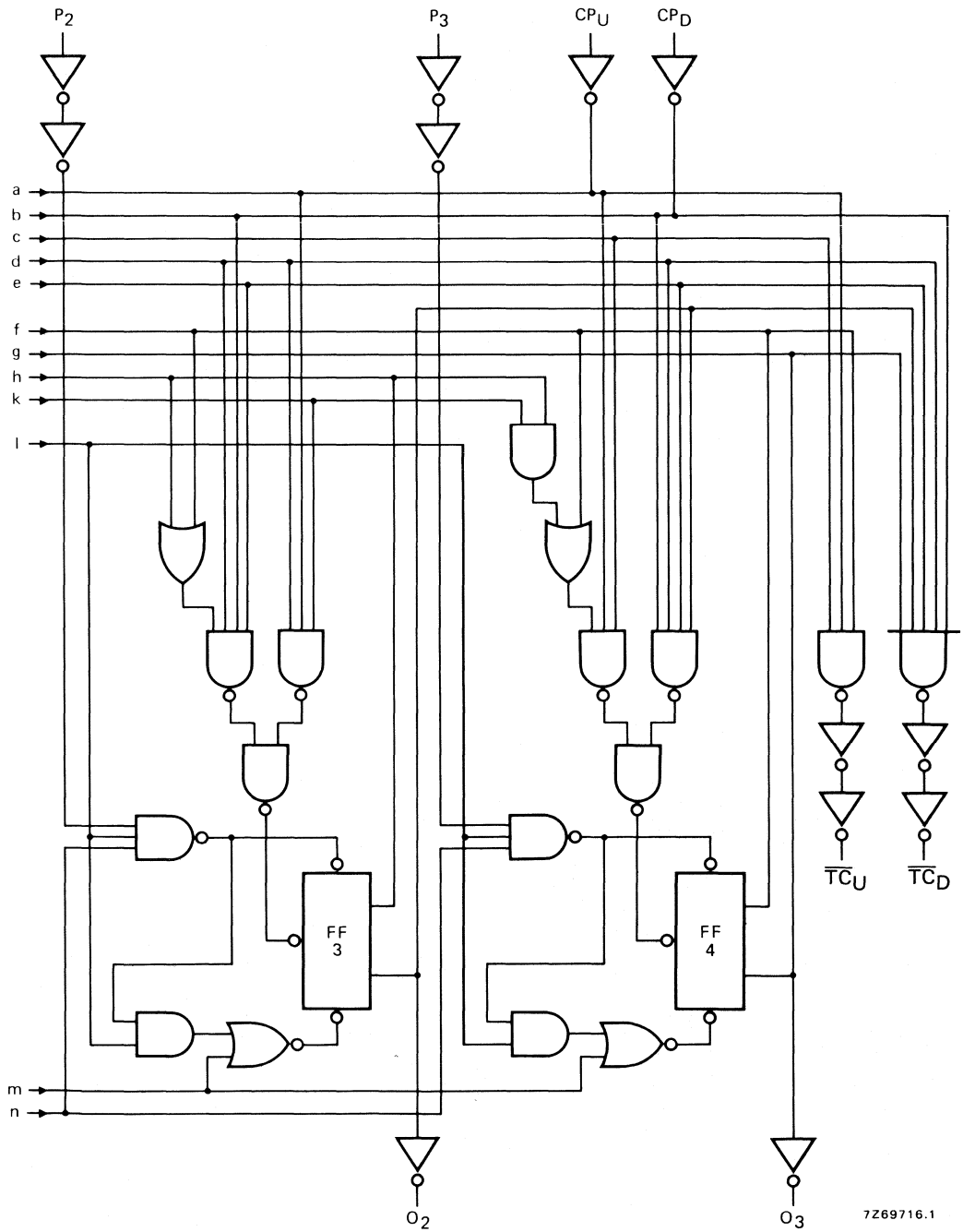


Fig. 3 Logic diagram (continued).

FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	mode
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H	∫	H	count-up
L	H	H	∫	count-down

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition

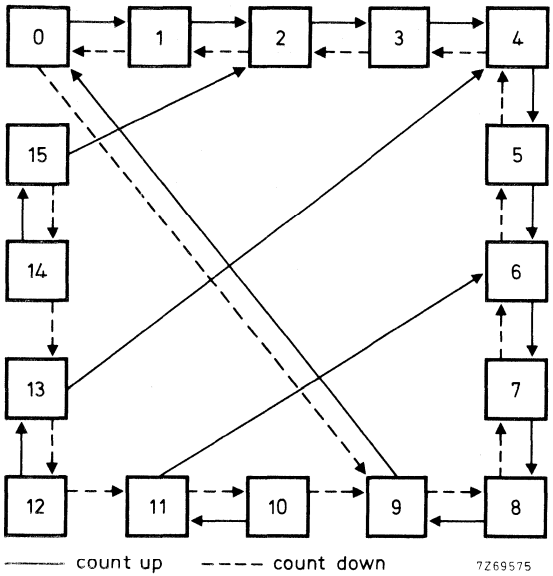


Fig. 4 State diagram.

Logic equations for terminal count:

$$\overline{TC}_U = \overline{O_0 \cdot O_3 \cdot \overline{CP}_U}$$

$$\overline{TC}_D = \overline{\overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \cdot \overline{CP}_D}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$550\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$6500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$CP_U \rightarrow O_n$	5			210	415	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	165	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow O_n$	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170	ns	74 ns + (0,23 ns/pF) C_L
	15			65	125	ns	57 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$CP_U \rightarrow \overline{TC}_U$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	185	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow \overline{TC}_D$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			100	195	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			195	390	ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$MR \rightarrow \overline{TC}_U$	5			145	285	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
$MR \rightarrow \overline{TC}_D$	5			365	730	ns	338 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		130	265	ns	119 ns + (0,23 ns/pF) C_L
	15			100	205	ns	92 ns + (0,16 ns/pF) C_L
$\overline{PL} \rightarrow O_n$	5			185	360	ns	158 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L
	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		160	80		ns	
$P_n \longrightarrow \overline{PL}$	10	t_{su}	60	30		ns	
	15		50	25		ns	
Hold time	5		10	−70		ns	
$P_n \longrightarrow \overline{PL}$	10	t_{hold}	5	−25		ns	
	15		5	−20		ns	
Minimum CP_U or CP_D	5		150	75		ns	
pulse width; LOW	10	t_{WCPL}	50	25		ns	
	15		35	20		ns	
Minimum MR	5		180	90		ns	
pulse width; HIGH	10	t_{WMRH}	70	35		ns	
	15		60	30		ns	see also waveforms Fig. 5
Minimum $\overline{PL}$	5		120	60		ns	
pulse width; LOW	10	t_{WPLL}	45	20		ns	
	15		30	15		ns	
Recovery time	5		125	65		ns	
for MR	10	t_{RMR}	70	35		ns	
	15		50	25		ns	
Recovery time	5		90	45		ns	
for $\overline{PL}$	10	t_{RPL}	35	15		ns	
	15		25	10		ns	
Maximum clock	5		2,5	5		MHz	
pulse frequency	10	f_{max}	7	14		MHz	
	15		9	18		MHz	

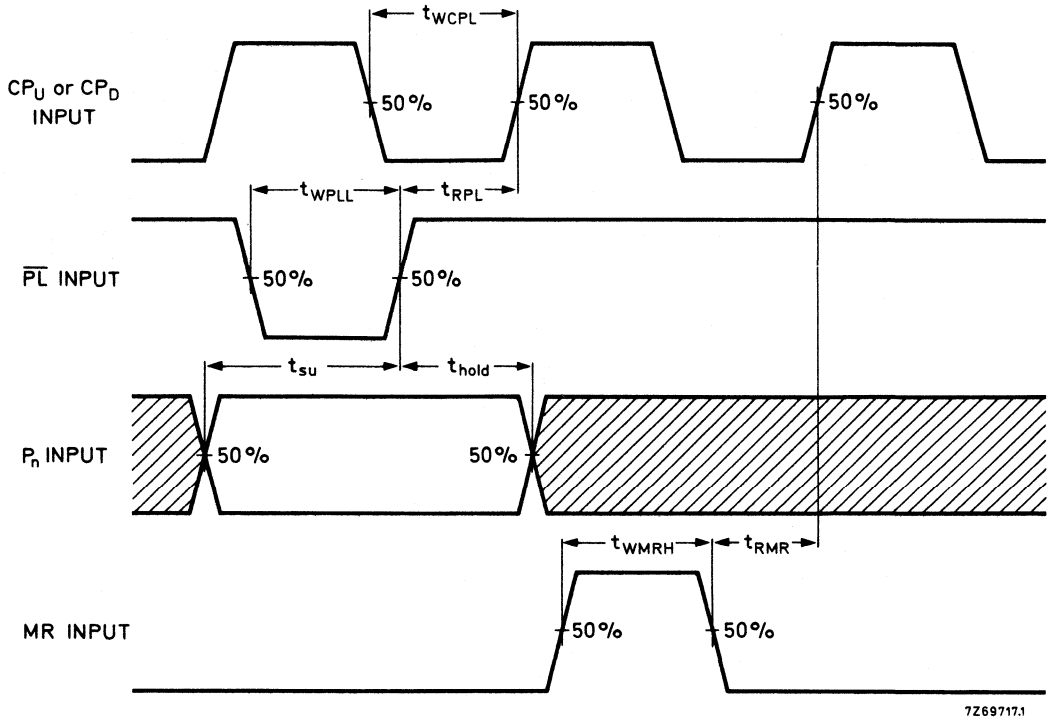


Fig. 5 Waveforms showing recovery times for $\overline{PL}$ and MR, minimum pulse widths for CP_U, CP_D, $\overline{PL}$ and MR, and set-up and hold times for P to $\overline{PL}$. Set-up times and hold times are shown as positive values but may be specified as negative values.

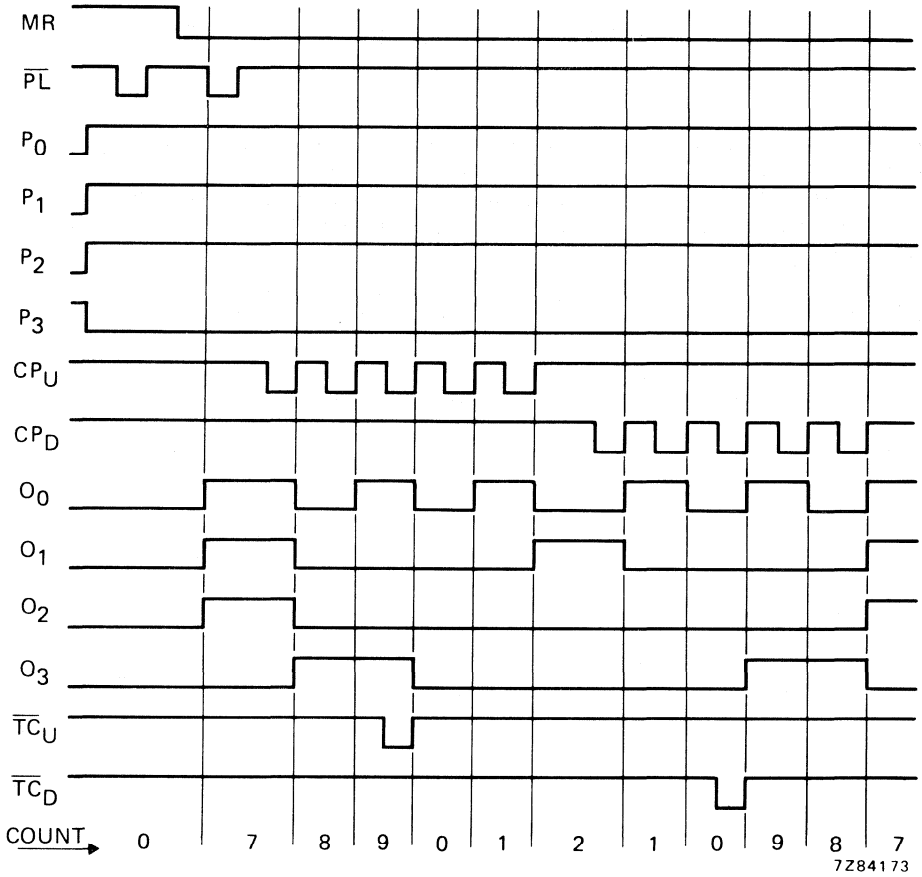


Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF40192B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage sunchronous counting.

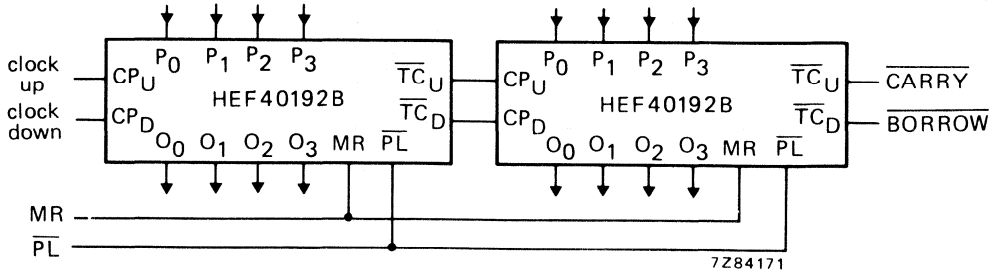


Fig. 7 Example of cascaded HEF40192B ICs.

4-BIT UP/DOWN BINARY COUNTER

The HEF40193B is a 4-bit synchronous up/down binary counter. The counter has a count-up clock input (CP_U), a count-down clock input (CP_D), an asynchronous parallel load input ($\overline{PL}$), four parallel data inputs (P_0 to P_3), an asynchronous master reset input (MR), four counter outputs (O_0 to O_3), an active LOW terminal count-up (carry) output ($\overline{TC}_U$) and an active LOW terminal count-down (borrow) output ($\overline{TC}_D$).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. The outputs $\overline{TC}_U$ and $\overline{TC}_D$ are normally HIGH. When the circuit has reached the maximum count state of '15', the next HIGH to LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again. Likewise, output $\overline{TC}_D$ will go LOW when the circuit is in the zero state and CP_D goes LOW. When $\overline{PL}$ is LOW, the information on P_0 to P_3 is asynchronously loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

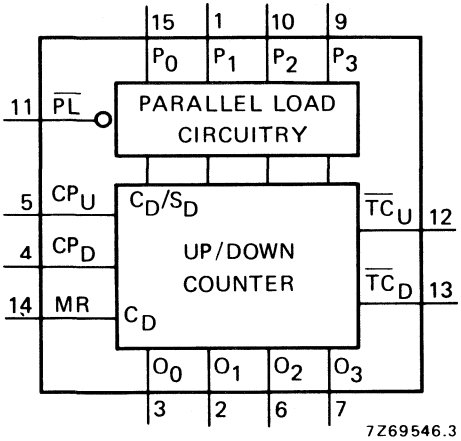


Fig. 1 Functional diagram.

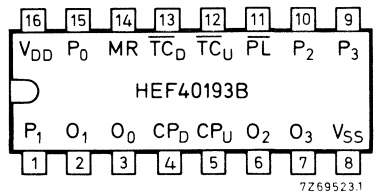


Fig. 2 Pinning diagram.

HEF40193BP : 16-lead DIL; plastic (SOT-38Z).
HEF40193BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40193BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{PL}$	parallel load input (active LOW)
P_0 to P_3	parallel data inputs
CP_U	count-up clock pulse input (LOW to HIGH, edge-triggered)
CP_D	count-down clock pulse input (LOW to HIGH, edge-triggered)
MR	master reset input (asynchronous)
$\overline{TC}_U$	buffered terminal count-up (carry) output (active LOW)
$\overline{TC}_D$	buffered terminal count-down (borrow) output (active LOW)
O_0 to O_3	buffered counter outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

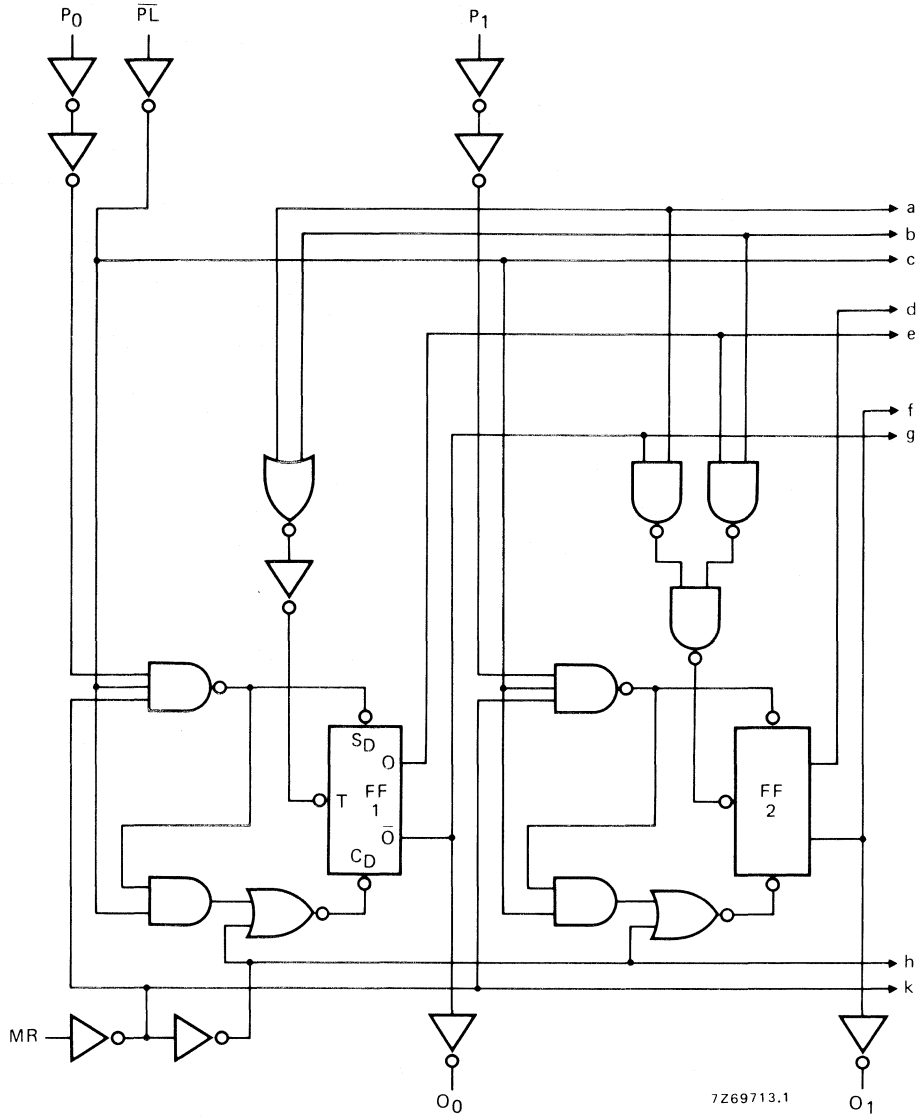


Fig. 3 Logic diagram (continued on next page).

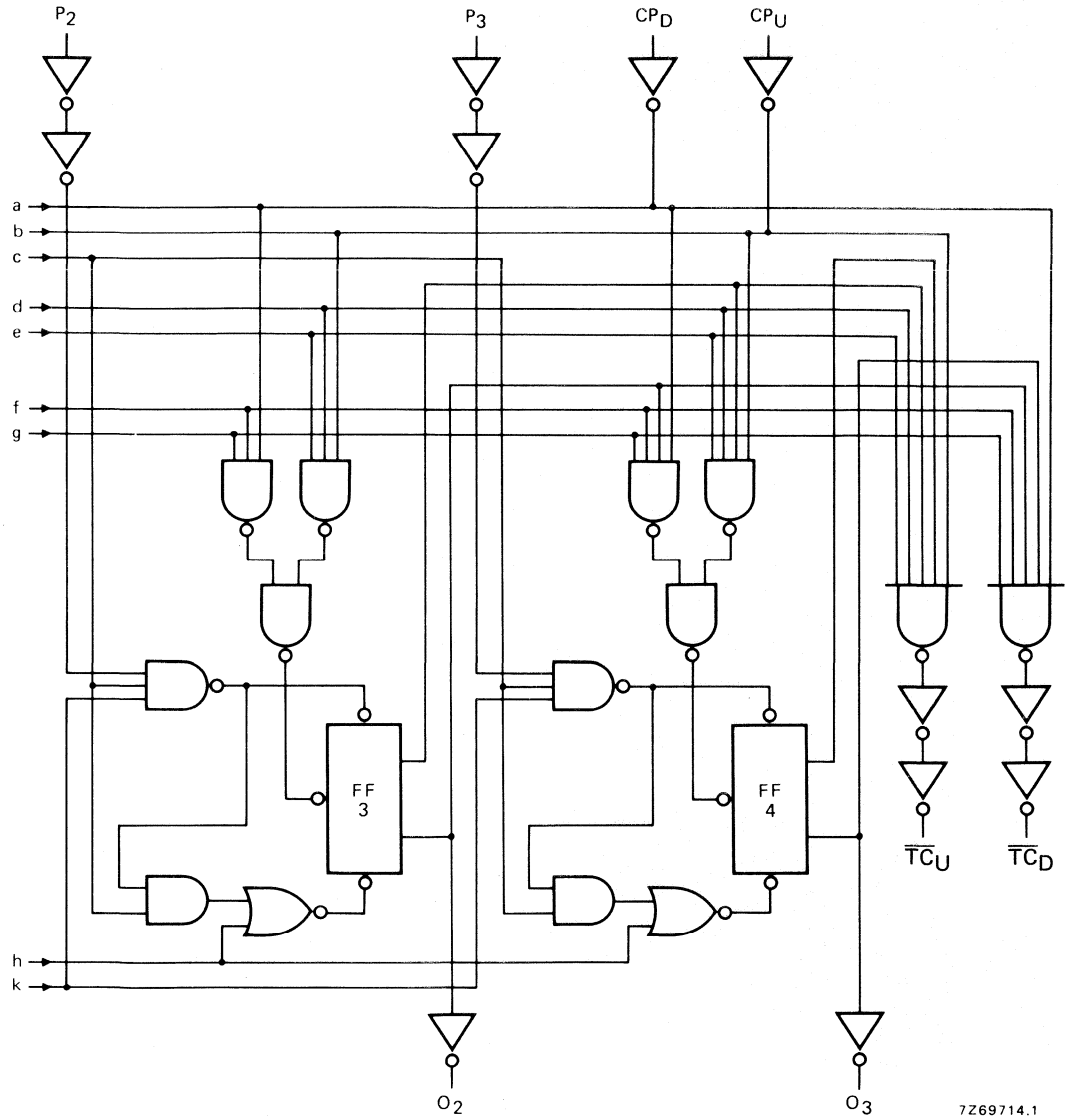
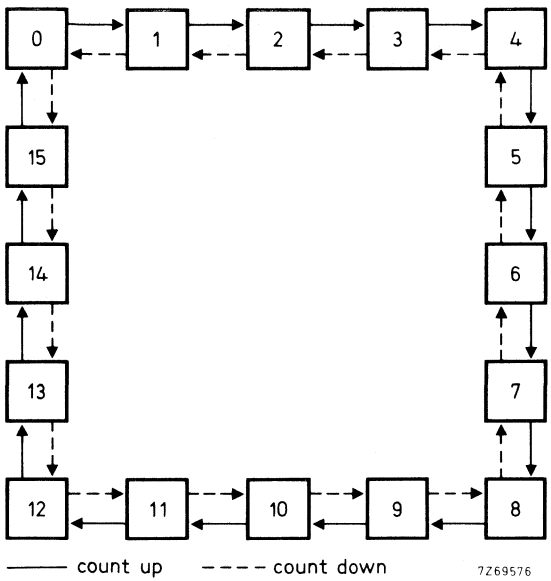


Fig. 3 Logic diagram (continued).

FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	mode
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H	∫	H	count-up
L	H	H	∫	count-down

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition



Logic equations for terminal count:

$$\overline{TC}_U = \overline{O_0 \cdot O_1 \cdot O_2 \cdot O_3 \cdot \overline{CP}_U}$$

$$\overline{TC}_D = \overline{\overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \cdot \overline{CP}_D}$$

Fig. 4 State diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
$CP_U \rightarrow O_n$	5			210	415 ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	165 ns	74 ns + (0,23 ns/pF) C_L
	15			60	120 ns	52 ns + (0,16 ns/pF) C_L
	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow O_n$	5			210	425 ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170 ns	74 ns + (0,23 ns/pF) C_L
	15			60	125 ns	57 ns + (0,16 ns/pF) C_L
	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
$CP_U \rightarrow \overline{TC}_U$	5			125	250 ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
	5			95	185 ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80 ns	29 ns + (0,23 ns/pF) C_L
	15			30	60 ns	22 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow \overline{TC}_D$	5			140	280 ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			100	195 ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85 ns	29 ns + (0,23 ns/pF) C_L
	15			30	65 ns	22 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			195	390 ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160 ns	69 ns + (0,23 ns/pF) C_L
	15			60	120 ns	52 ns + (0,16 ns/pF) C_L
$MR \rightarrow \overline{TC}_U$	5			145	285 ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
$MR \rightarrow \overline{TC}_D$	5			365	730 ns	338 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		130	265 ns	119 ns + (0,23 ns/pF) C_L
	15			100	205 ns	92 ns + (0,16 ns/pF) C_L
$\overline{PL} \rightarrow O_n$	5			185	360 ns	158 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			55	110 ns	47 ns + (0,16 ns/pF) C_L
	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		160	80		ns	
$P_n \rightarrow \overline{PL}$	10	t_{su}	60	30		ns	
	15		50	25		ns	
Hold time	5		10	−70		ns	
$P_n \rightarrow \overline{PL}$	10	t_{hold}	5	−25		ns	
	15		5	−20		ns	
Minimum CP_U or CP_D	5		150	75		ns	
pulse width; LOW	10	t_{WCPL}	50	25		ns	
	15		35	20		ns	
Minimum MR	5		180	90		ns	
pulse width; HIGH	10	t_{WMRH}	70	35		ns	
	15		60	30		ns	see also waveforms Fig. 5
Minimum $\overline{PL}$	5		120	60		ns	
pulse width; LOW	10	t_{WPLL}	45	20		ns	
	15		30	15		ns	
Recovery time	5		125	65		ns	
for MR	10	t_{RMR}	70	35		ns	
	15		50	25		ns	
Recovery time	5		90	45		ns	
for $\overline{PL}$	10	t_{RPL}	35	15		ns	
	15		25	10		ns	
Maximum clock	5		2,5	5		MHz	
pulse frequency	10	f_{max}	7	14		MHz	
	15		9	18		MHz	

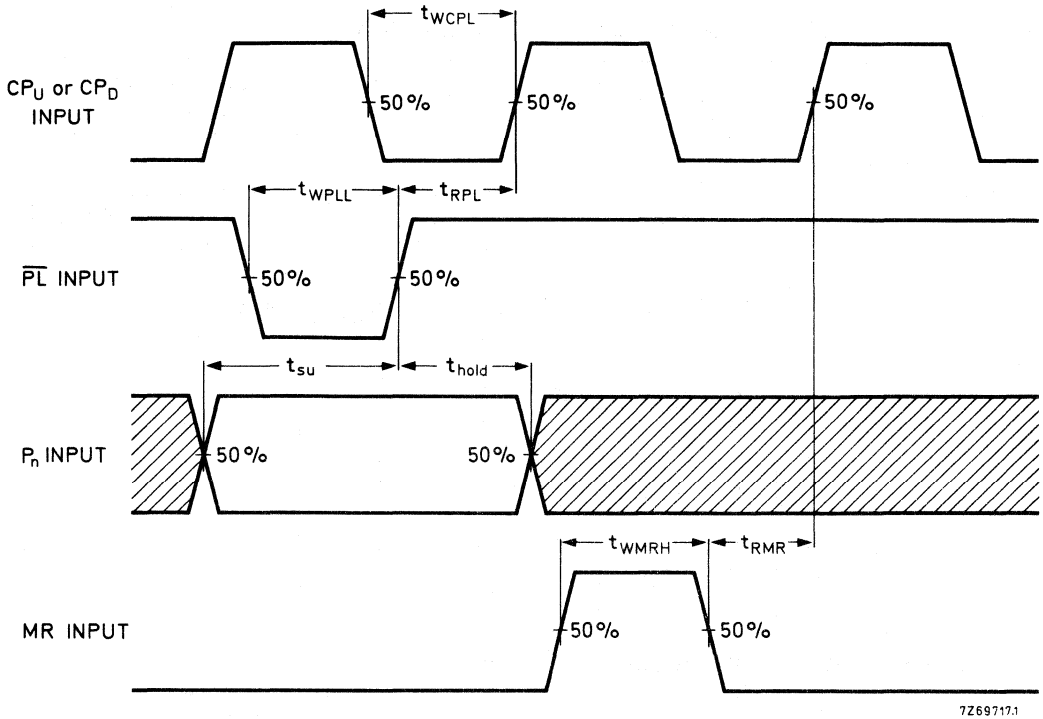


Fig. 5 Waveforms showing recovery times for $\overline{PL}$ and MR, minimum pulse widths for CP_U, CP_D, $\overline{PL}$ and MR, and set-up and hold times for P to $\overline{PL}$. Set-up times and hold times are shown as positive values but may be specified as negative values.

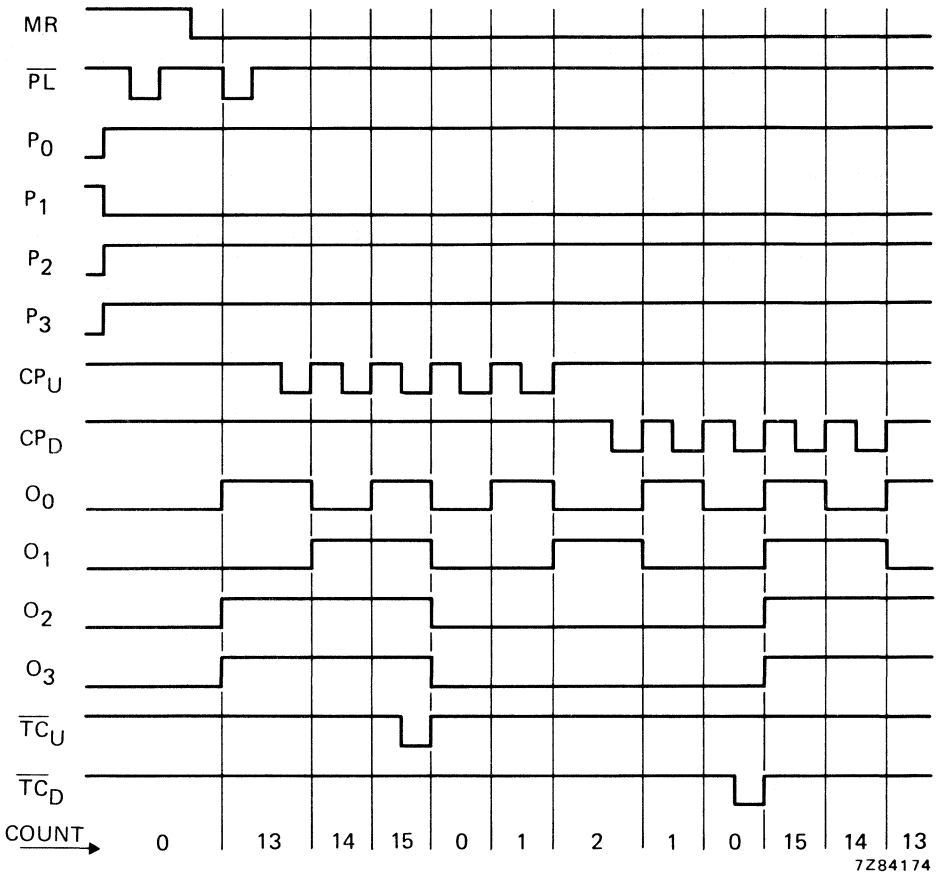


Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF40193B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage synchronous counting

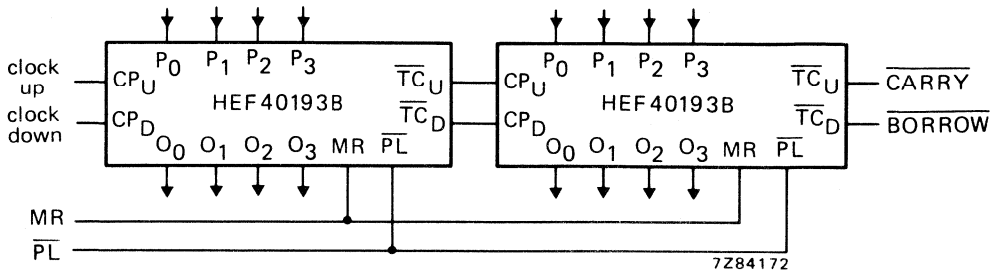


Fig. 7 Example of cascaded HEF40193B ICs.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The HEF40194B is a 4-bit bidirectional shift register with two mode control inputs (S_0 and S_1), a clock input (CP), a serial data shift left input (D_{SL}), a serial data shift right input (D_{SR}), four parallel data inputs (P_0 to P_3), an overriding asynchronous master reset input ($\overline{MR}$), and four buffered parallel outputs (O_0 to O_3). When LOW, $\overline{MR}$ resets all stages and forces O_0 to O_3 LOW, overriding all other input conditions. When $\overline{MR}$ is HIGH, the operation mode is controlled by S_0 and S_1 as shown in the function table.

Serial and parallel operation are edge-triggered on the LOW to HIGH transition of CP. The inputs at which the data are to be entered and S_0, S_1 must be stable for a set-up time before the LOW to HIGH transition of CP.

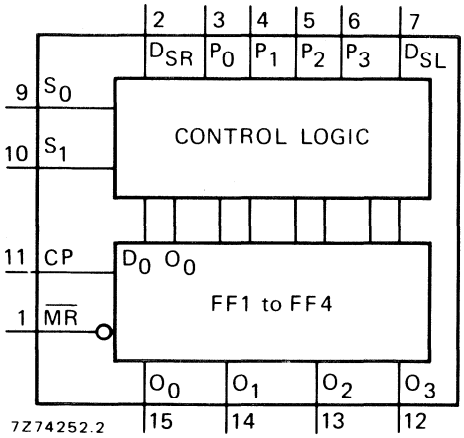


Fig. 1 Functional diagram.

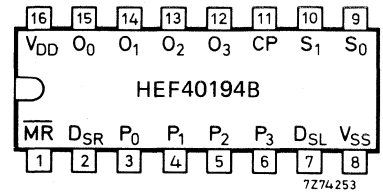


Fig. 2 Pinning diagram.

HEF40194BP : 16-lead DIL; plastic (SOT-38Z).
HEF40194BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40194BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

S_0, S_1	mode control inputs
P_0 to P_3	parallel data inputs
D_{SR}	serial data shift right input
D_{SL}	serial data shift left input
CP	clock input (LOW to HIGH edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	buffered parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI — see Family Specifications

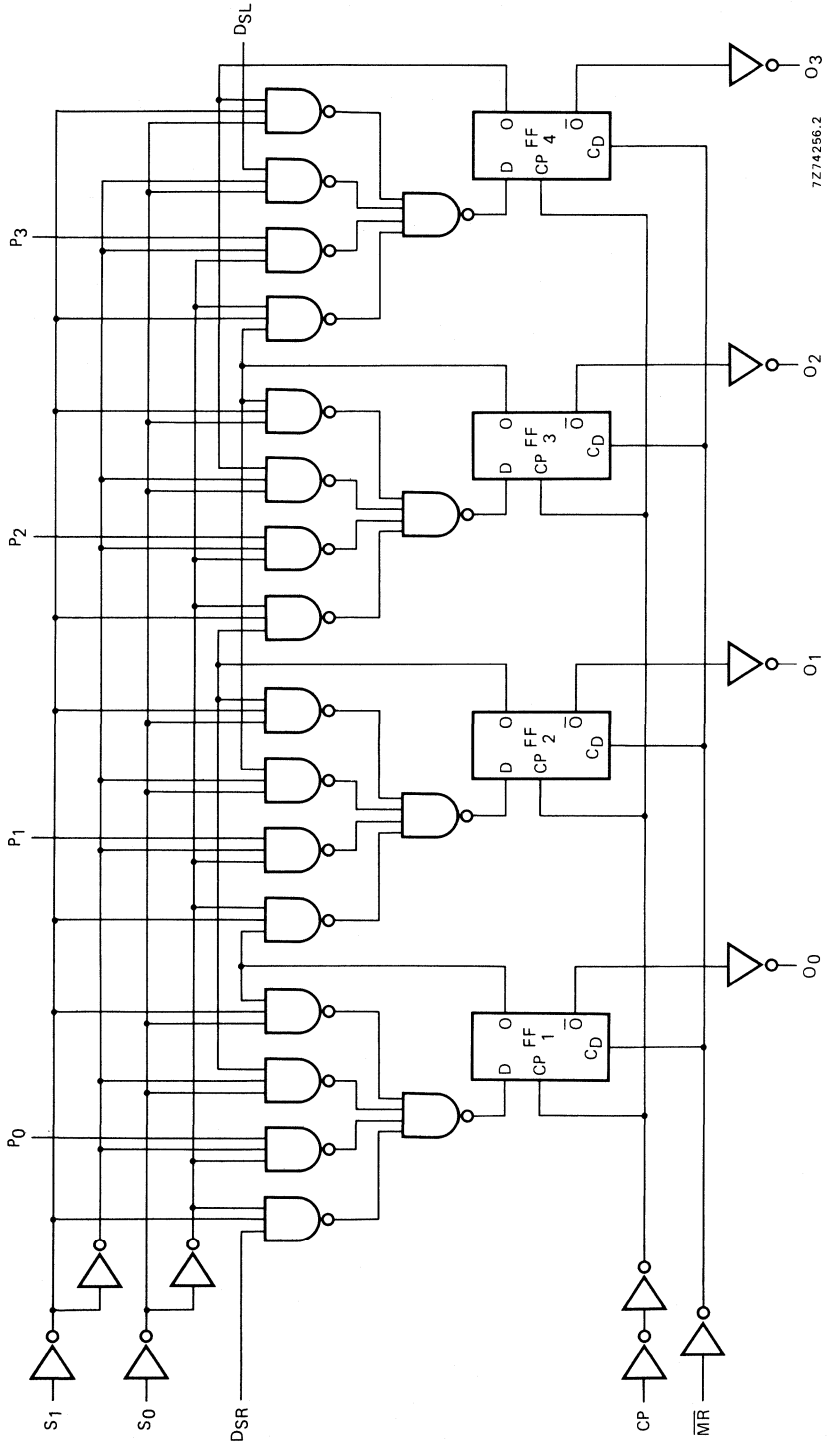


Fig. 3 Logic diagram.

FUNCTION TABLE

operating mode	inputs ($\overline{MR}$ = HIGH)					outputs at t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	P_0 to P_3	O_0	O_1	O_2	O_3
hold	L	L	X	X	X	O_0	O_1	O_2	O_3
shift left	H	L	X	L	X	O_1	O_2	O_3	L
	H	L	X	H	X	O_1	O_2	O_3	H
shift right	L	H	L	X	X	L	O_0	O_1	O_2
	L	H	H	X	X	H	O_0	O_1	O_2
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
t_{n+1} = state after next LOW to HIGH transition of CP

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6\,900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$18\,900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			100	205	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			80	165	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	55	ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			85	175	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up times	5		80	40		ns	
P_n, D_{SR}, D_{SL} → CP	10	t_{su}	30	15		ns	
	15		20	10		ns	
	5		140	70		ns	
S_n → CP	10	t_{su}	60	30		ns	
	15		40	20		ns	
Hold times	5		10	−30		ns	
P_n, D_{SR}, D_{SL} → CP	10	t_{hold}	5	−10		ns	
	15		5	−5		ns	
	5		25	−45		ns	
S_n → CP	10	t_{hold}	15	−15		ns	
	15		10	−10		ns	
Minimum clock pulse width; LOW	5		50	25		ns	see also waveforms Figs 4 and 5
	10	t_{WCPL}	20	10		ns	
	15		20	10		ns	
Minimum $\overline{MR}$ pulse width; LOW	5		80	40		ns	
	10	t_{WMRL}	40	20		ns	
	15		30	15		ns	
Recovery time for $\overline{MR}$	5		30	10		ns	
	10	t_{RMR}	15	5		ns	
	15		15	5		ns	
Maximum clock pulse frequency	5		6	12		MHz	
	10	f_{max}	15	30		MHz	
	15		20	40		MHz	

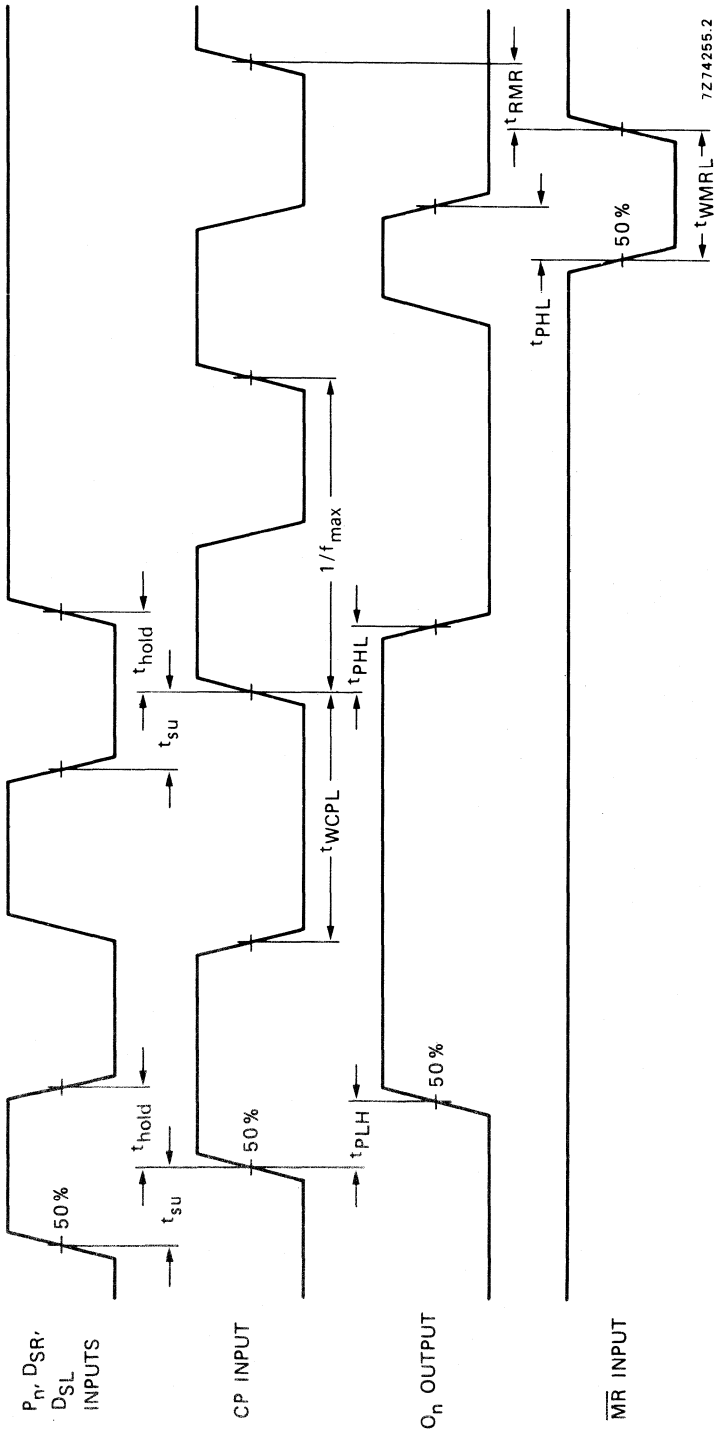


Fig. 4 Waveforms showing set-up times, hold times for D_{SR}, D_{SL} and P_n inputs; minimum $\overline{MR}$ pulse width, $\overline{MR}$ to output delays and $\overline{MR}$ to CP recovery time; minimum CP pulse width and CP to output delays. Set-up and hold times are shown as positive values but may be specified as negative values.

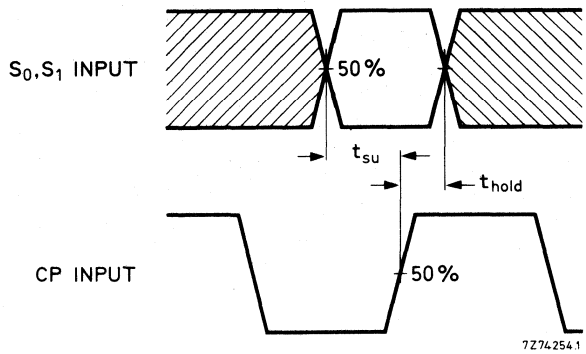


Fig. 5 Waveforms showing set-up times and hold times for S_0 and S_1 inputs. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40194B are:

- Arithmetic unit register
- Serial/parallel converter.

4-BIT UNIVERSAL SHIFT REGISTER

The HEF40195B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J, $\overline{K}$), a synchronous parallel enable input ($\overline{PE}$), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a buffered inverted output from the last bit position ($\overline{O}_3$) and an overriding asynchronous master reset input ($\overline{MR}$). Each register stage is of a D-type master-slave flip-flop.

Operation is synchronous (except for $\overline{MR}$) and is edge-triggered on the LOW to HIGH transition of the CP input. When $\overline{PE}$ is LOW, data are loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP. When $\overline{PE}$ is HIGH, data are shifted into the first register position from J and $\overline{K}$ and all the data in the register are shifted one position to the right on the LOW to HIGH transition of CP.

D-type entry is obtained by interconnecting J and $\overline{K}$.

When J is HIGH and $\overline{K}$ is LOW, the first stage is in the toggle mode. When J is LOW and $\overline{K}$ is HIGH, the first stage is in the hold mode.

A LOW on $\overline{MR}$ resets all four bit positions (O_0 to O_3 = LOW, $\overline{O}_3$ = HIGH) independent of all other input conditions.

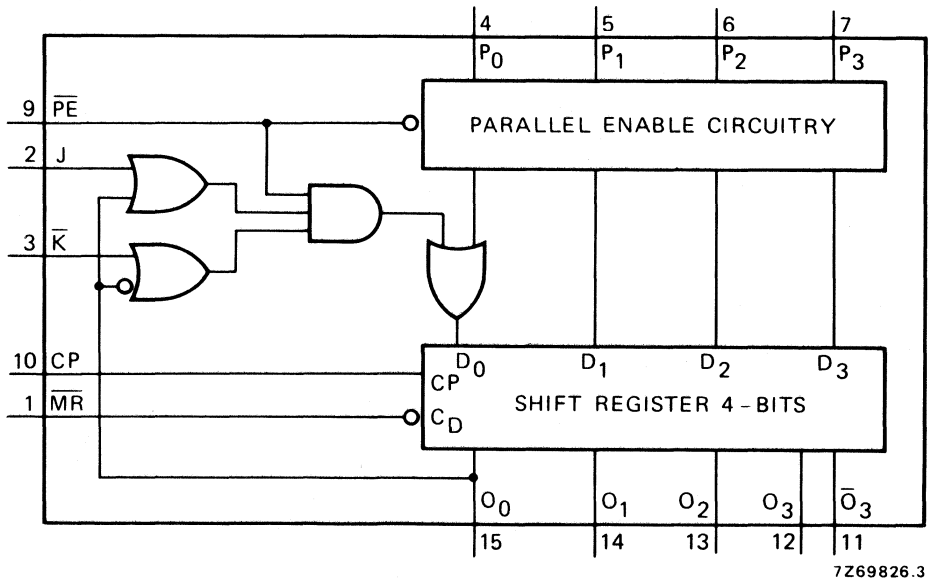


Fig. 1 Functional diagram.

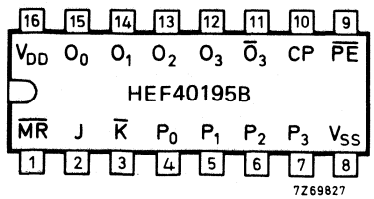


Fig. 2 Pinning diagram.

HEF40195BP : 16-lead DIL; plastic (SOT-38Z).
HEF40195BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF40195BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

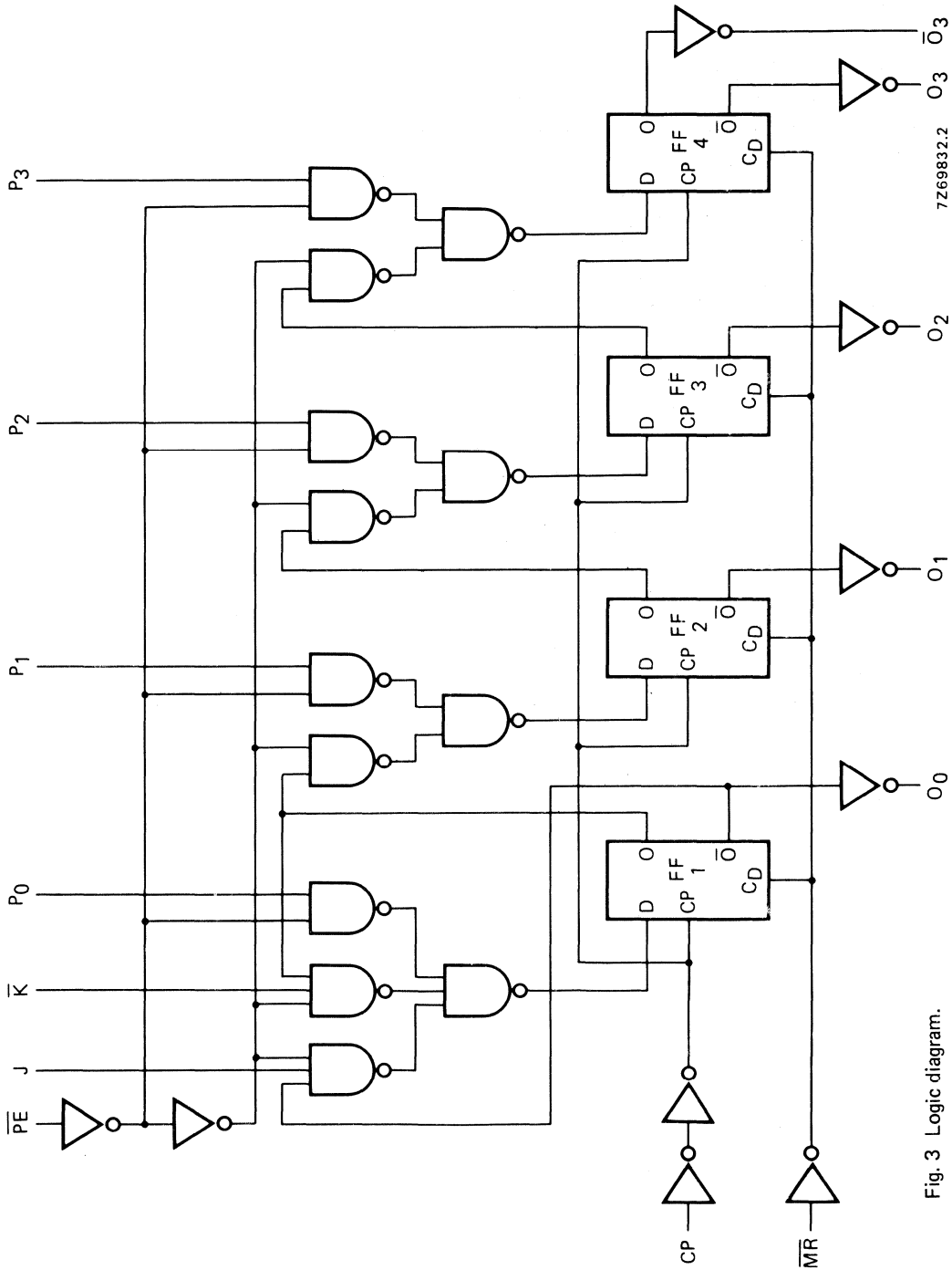


Fig. 3 Logic diagram.

PINNING

$\overline{PE}$	parallel enable input (active LOW)
P_0 to P_3	parallel data inputs
J	first stage J-input (active HIGH)
$\overline{K}$	first stage K-input (active LOW)
CP	clock input (LOW to HIGH edge triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	buffered parallel outputs
$\overline{O}_3$	buffered inverted output from last stage

FUNCTION TABLE

operating mode	inputs ($\overline{MR}$ = HIGH)							outputs at $t_n + 1$				
	$\overline{PE}$	J	$\overline{K}$	P_0	P_1	P_2	P_3	O_0	O_1	O_2	O_3	$\overline{O}_3$
shift mode	H	L	L	X	X	X	X	L	O_0	O_1	O_2	$\overline{O}_2$
	H	L	H	X	X	X	X	O_0	O_0	O_1	O_2	$\overline{O}_2$
	H	H	L	X	X	X	X	$\overline{O}_0$	O_0	O_1	O_2	$\overline{O}_2$
	H	H	H	X	X	X	X	H	O_0	O_1	O_2	$\overline{O}_2$
parallel entry mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
$t_n + 1$ = state after next LOW to HIGH transition of CP

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			105	215	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	85	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
CP → $\overline{O}_3$	5			125	255	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			100	205	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			125	235	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	85	ns	32 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Set-up times	5			70	35	ns	see also waveforms Figs 4 and 5
J, $\overline{K}$ → CP	10	t_{su}		20	10	ns	
	15			10	5	ns	
	5			85	40	ns	
P_n → CP	10	t_{su}		25	10	ns	
	15			10	5	ns	
	5			115	55	ns	
$\overline{PE}$ → CP	10	t_{su}		45	20	ns	
	15			30	15	ns	
Hold times	5			15	−20	ns	
J, $\overline{K}$ → CP	10	t_{hold}		5	−5	ns	
	15			0	−5	ns	
	5			20	−25	ns	
P_n → CP	10	t_{hold}		10	−5	ns	
	15			0	−5	ns	
	5			10	−50	ns	
$\overline{PE}$ → CP	10	t_{hold}		5	−20	ns	
	15			5	−10	ns	
Minimum clock	5			60	30	ns	
pulse width; LOW	10	t_{WCPL}		25	10	ns	
	15			20	10	ns	
Minimum $\overline{MR}$	5			100	50	ns	
pulse width; HIGH	10	t_{WMRL}		40	20	ns	
	15			30	15	ns	
Recovery time	5			30	10	ns	
for $\overline{MR}$	10	t_{RMR}		15	5	ns	
	15			15	5	ns	
Maximum clock	5			5	10	MHz	
pulse frequency	10	f_{max}		14	28	MHz	
	15			19	39	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$8300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$22\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

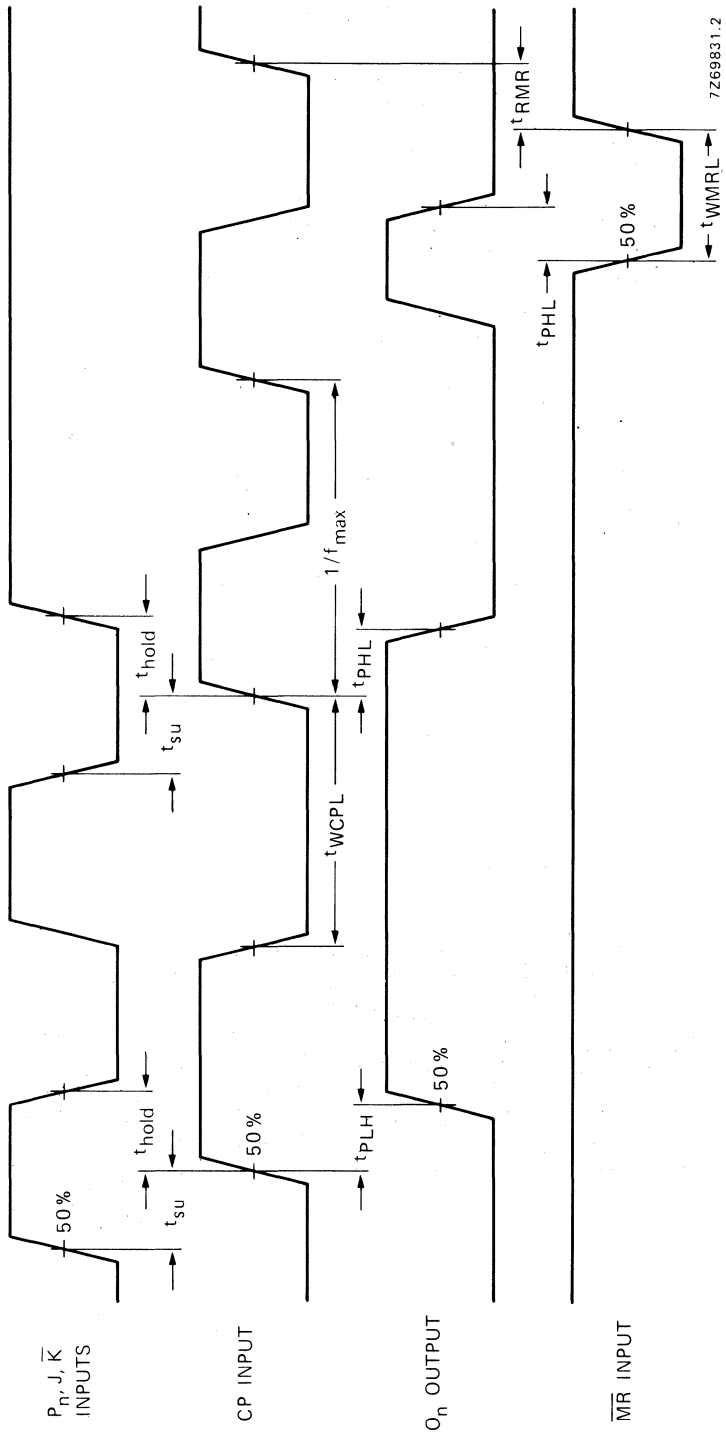


Fig. 4 Waveforms showing set-up times, hold times for J, $\overline{K}$ and P_n inputs; minimum $\overline{MR}$ pulse width, $\overline{MR}$ to output delays and $\overline{MR}$ to CP recovery time; minimum CP pulse width and CP to output delays. Set-up and hold times are shown as positive values but may be specified as negative values.

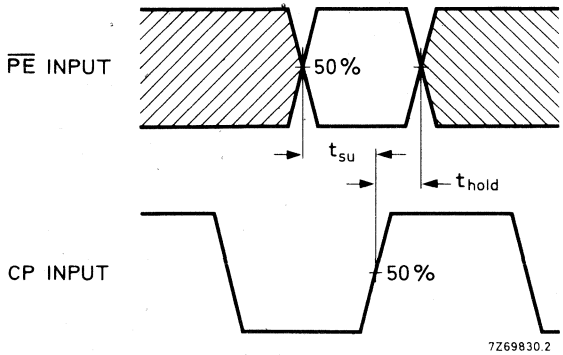


Fig. 5 Waveforms showing set-up and hold times for $\overline{PE}$ input. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40195B are:

- Serial data transfer
- Parallel data transfer
- Serial to parallel data transfer
- Parallel to serial data transfer

OCTAL BUFFERS WITH 3-STATE OUTPUTS

The HEF40240B is an octal inverting buffer with 3-state outputs. It features output stages with high current output capability suitable for driving highly capacitive loads.

The 3-state outputs are controlled by the output enable inputs $\overline{EO}_A$ and $\overline{EO}_B$. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity.

Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

The HEF40240B is pin and functionally compatible with the TTL '240' device.

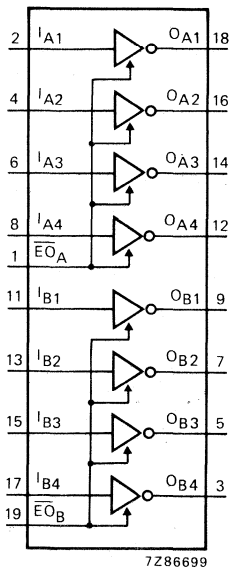


Fig. 1 Functional diagram.

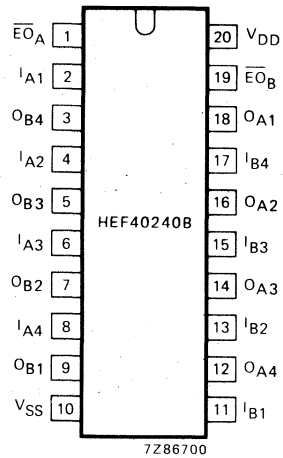


Fig. 2 Pinning diagram.

HEF40240BP : 20-lead DIL; plastic (SOT-146).
HEF40240BT : 20-lead mini-pack; plastic (SO-20; SOT-163A).

PINNING

I_{A1} to I_{A4}, I_{B1} to I_{B4} } inputs
O_{A1} to O_{A4}, O_{B1} to O_{B4} } bus outputs
$\overline{EO}_A$, $\overline{EO}_B$ output enable inputs (active LOW)

FAMILY DATA

I_{DD} LIMITS category buffers } see Family Specifications

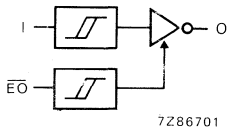


Fig. 3 Logic diagram (one buffer).

TRUTH TABLE

inputs		output
I_n	$\overline{EO}$	O_n
H	L	L
L	L	H
X	H	Z

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance off state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

See Family Specifications except for:

D.C. current into any input	$\pm I_I$	max.	10 mA
D.C source or sink current into any output	$\pm I_O$	max.	25 mA
D.C. current into the supply terminals	$\pm I$	max.	100 mA

D.C. CHARACTERISTICS

V_{SS} = 0 V

parameter	V_{DD}	V_{OH}	V_{OL}	symbol	T_{amb} (°C) −40 min.	−40 typ.	+25 min.	+25 typ.	+85 min.	+85 typ.	unit
	V	V	V								
Output current HIGH	5	3,6	–	$-I_{OH}$	9,3	–	10,0	24,0	10,7	–	mA
	10	8,4	–	$-I_{OH}$	14,4	–	15,0	46,0	15,0	–	mA
	15	13,2	–	$-I_{OH}$	19,5	–	20,0	62,0	19,8	–	mA
Output current HIGH	5	4,6	–	$-I_{OH}$	0,75	–	0,6	1,2	0,45	–	mA
	10	9,5	–	$-I_{OH}$	1,85	–	1,5	3,0	1,1	–	mA
	15	13,5	–	$-I_{OH}$	14,5	–	15,0	50,0	15,5	–	mA
Output current LOW	5	–	0,4	I_{OL}	2,9	–	2,3	5,4	1,75	–	mA
	10	–	0,5	I_{OL}	9,5	–	7,6	17,0	5,50	–	mA
	15	–	1,5	I_{OL}	30,0	–	25,0	45,0	19,0	–	mA
Hysteresis voltage (any input)	5	–	–	V_H	–	–	–	220,0	–	–	mV
	10	–	–	V_H	–	–	–	250,0	–	–	mV
	15	–	–	V_H	–	–	–	320,0	–	–	mV

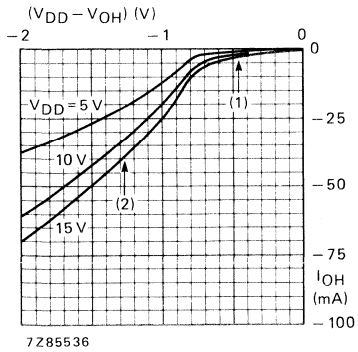


Fig. 4 Typical output source current characteristic.

(1) P-channel MOS transistor conducting.
(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

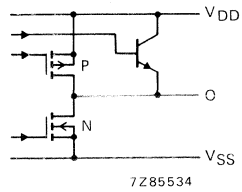


Fig. 5 Schematic diagram of output stage.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

all buffers switching	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$4\,250\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma\ (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$17\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	
	15	$46\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	typical extrapolation formula
Propagation delays							
$A_n \rightarrow B_n$	5			95	190	ns	83 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	35 ns + (0,10 ns/pF) C_L
	15			30	60	ns	26 ns + (0,07 ns/pF) C_L
$A_n \rightarrow B_n$	5			85	170	ns	82 ns + (0,06 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	38 ns + (0,03 ns/pF) C_L
	15			30	60	ns	29 ns + (0,02 ns/pF) C_L
Output transition	5			40	80	ns	see Fig. 6
times	10	t_{THL}		20	40	ns	
HIGH to LOW	15			15	30	ns	
	5			30	60	ns	
LOW to HIGH	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO} \rightarrow A_n, B_n$	5			70	140	ns	
HIGH	10	t_{PHZ}		35	70	ns	
	15			30	60	ns	
	5			75	150	ns	
LOW	10	t_{PLZ}		40	80	ns	
	15			30	60	ns	
Output enable times							
$\overline{EO} \rightarrow A_n, B_n$	5			80	160	ns	
HIGH	10	t_{PZH}		35	70	ns	
	15			30	60	ns	
	5			90	180	ns	
LOW	10	t_{PZL}		40	80	ns	
	15			30	60	ns	

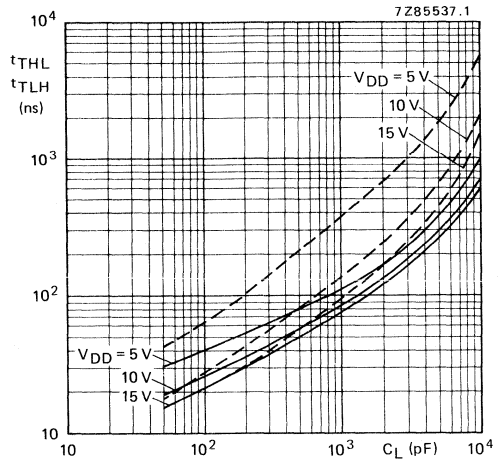


Fig. 6 Output transition times as a function of the load capacitance.
———— t_{TLH}; – – – – – t_{THL}.

OCTAL BUFFERS WITH 3-STATE OUTPUTS

The HEF40244B is an octal non-inverting buffer with 3-state outputs. It features output stages with high current output capability suitable for driving highly capacitive loads.

The 3-state outputs are controlled by the output enable inputs $\overline{EO}_A$ and $\overline{EO}_B$. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity.

Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

The HEF40244B is pin and functionally compatible with the TTL '244' device.

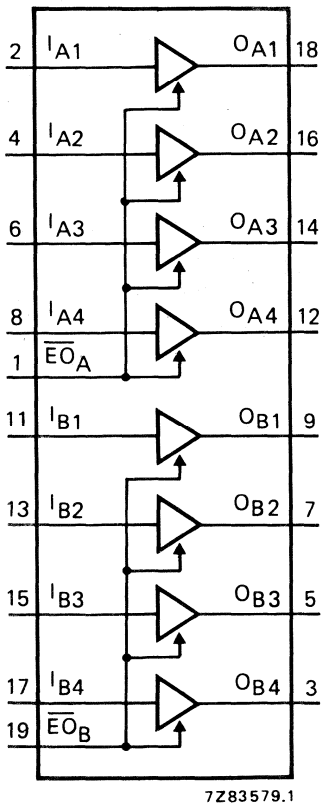


Fig. 1 Functional diagram.

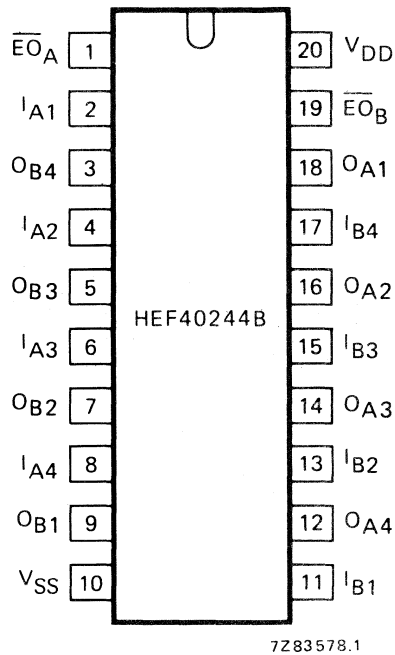


Fig. 2 Pinning diagram.

HEF40244BP : 20-lead DIL; plastic (SOT-146).
HEF40244BT : 20 lead mini-pack; plastic (SO-20; SOT-163A).

FAMILY DATA | see Family Specifications

I_{DD} LIMITS category buffers |

PINNING

I_{A1} to I_{A4}, I_{B1} to I_{B4}	inputs
O_{A1} to O_{A4}, O_{B1} to O_{B4}	bus outputs
$\overline{EO}_A$, $\overline{EO}_B$	output enable inputs (active LOW)

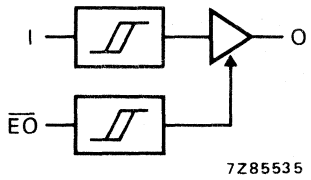


Fig. 3 Logic diagram (one buffer).

TRUTH TABLE

inputs		output
I_n	$\overline{EO}$	O_n
H	L	H
L	L	L
X	H	Z

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance off state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10 mA
D.C. source or sink current into any output	$\pm I_O$	max.	25 mA
D.C. current into the supply terminals	$\pm I$	max.	100 mA

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 typ.	+25 min.	+25 typ.	+85 min.	+85 typ.	
Output current HIGH	5	4,6			0,75		0,6	1,2	0,45		mA
	10	9,5		$-I_{OH}$	1,85		1,5	3,0	1,1		mA
	15	13,5			14,5		15	50	15,5		mA
Output current HIGH	5	3,6			9,3		10	24	10,7		mA
	10	8,4		$-I_{OH}$	14,4		15	46	15,0		mA
	15	13,2			19,5		20	62	19,8		mA
Output current LOW	5		0,4		2,9		2,3	5,4	1,75		mA
	10		0,5	I_{OL}	9,5		7,6	17	5,50		mA
	15		1,5		30,0		25	45	19,0		mA
Hysteresis voltage (any input)	5							220			mV
	10			V_H				250			mV
	15							320			mV

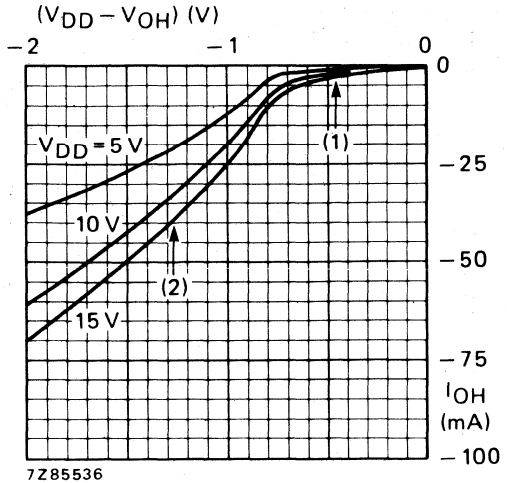


Fig. 4 Typical output source current characteristic.

(1) P-channel MOS transistor conducting.
(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

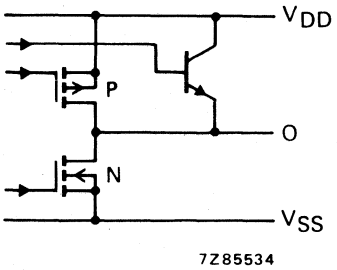


Fig. 5 Schematic diagram of output stage.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

all buffers switching	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	4 250 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	17 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	46 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$A_n \longrightarrow B_n$	5			95	190	ns	83 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	35 ns + (0,10 ns/pF) C_L
	15			30	60	ns	26 ns + (0,07 ns/pF) C_L
$A_n \longrightarrow B_n$	5			85	170	ns	82 ns + (0,06 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	38 ns + (0,03 ns/pF) C_L
	15			30	60	ns	29 ns + (0,02 ns/pF) C_L
Output transition times	5			40	80	ns	see Fig. 6
	10	t_{THL}		20	40	ns	
HIGH to LOW	15			15	30	ns	
	5			30	60	ns	
LOW to HIGH	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO} \longrightarrow A_n, B_n$	5			70	140	ns	
HIGH	10	t_{PHZ}		35	70	ns	
	15			30	60	ns	
	5			75	150	ns	
LOW	10	t_{PLZ}		40	80	ns	
	15			30	60	ns	
Output enable times							
$\overline{EO} \longrightarrow A_n, B_n$	5			80	160	ns	
HIGH	10	t_{PZH}		35	70	ns	
	15			30	60	ns	
	5			90	180	ns	
LOW	10	t_{PZL}		40	80	ns	
	15			30	60	ns	

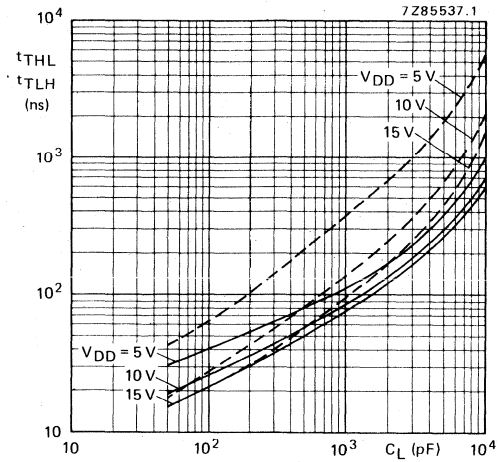


Fig. 6 Output transition times as a function of the load capacitance.
——— t_{TLH}; – – – – t_{THL}.

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

The HEF40245B is an octal bus transmitter/receiver designed for 8-line asynchronous, 2-way data communication between data buses. It features output stages with high current output capability suitable for driving highly capacitive loads.

The direction input (DR) controls transmission of data from bus A to bus B, or bus B to bus A, depending on its logic level. The 3-state outputs are controlled by the enable input $\overline{EO}$. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity.

Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

The HEF40245B is pin and functionally compatible with the TTL '245' device.

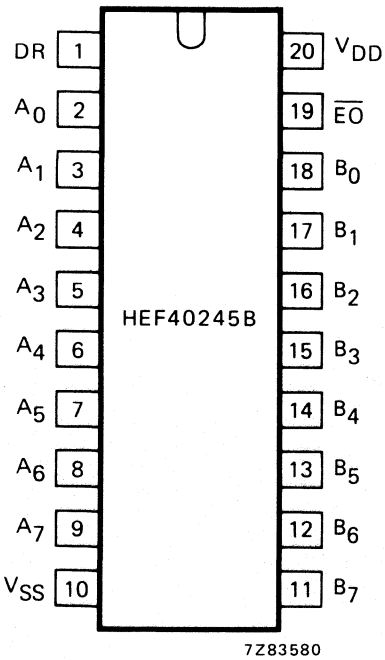


Fig. 1 Pinning diagram.

PINNING

A_0 to A_7	data input/output
B_0 to B_7	data input/output
DR	direction input
$\overline{EO}$	output enable input (active LOW)

HEF40245BP : 20-lead DIL; plastic (SOT-146).
HEF40245BT : 20-lead mini-pack; plastic (SO-20; SOT-163A).

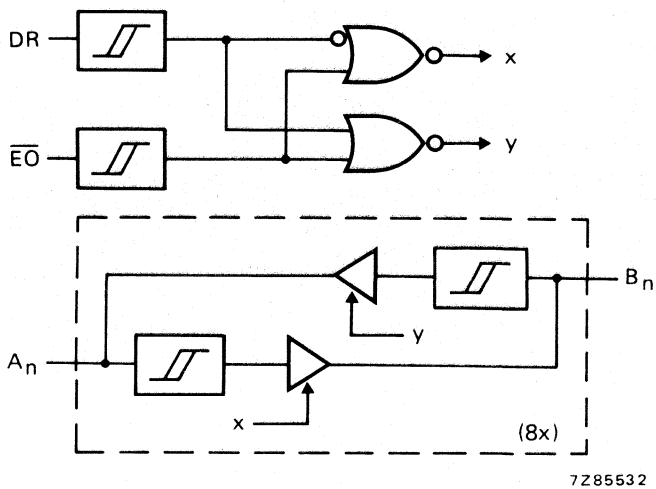


Fig. 2 Logic diagram; for functional diagram see Fig. 3.

FAMILY DATA

I_{DD} LIMITS category buffers } see Family Specifications.

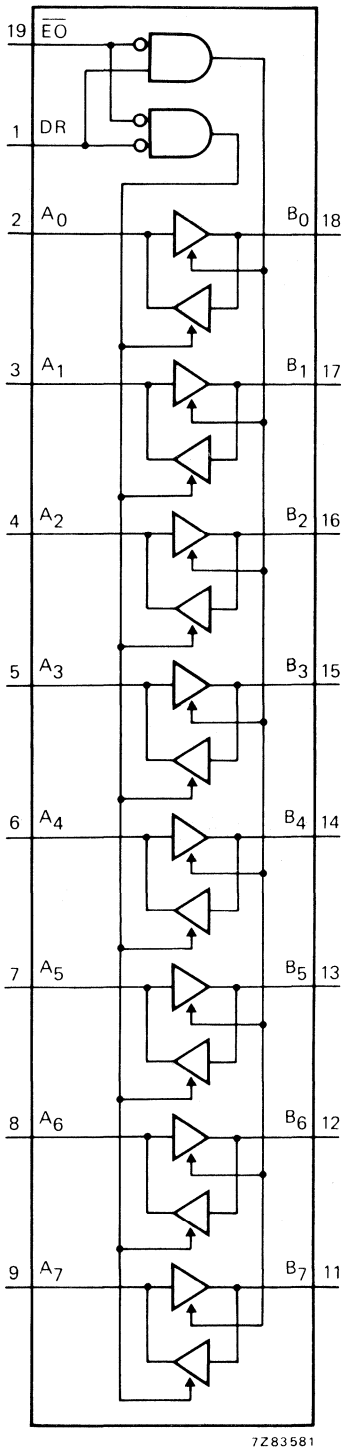
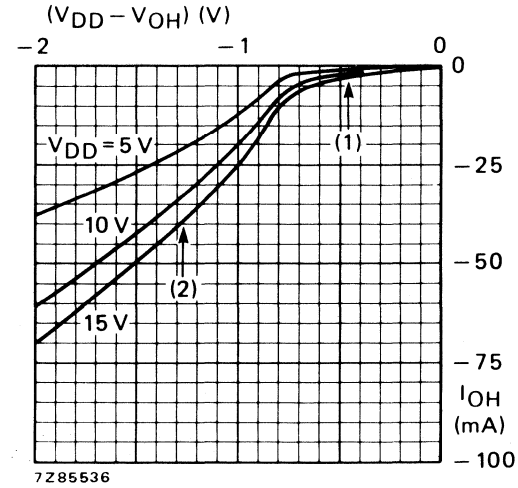


Fig. 3 Functional diagram.

FUNCTION TABLE

inputs		inputs/outputs	
$\overline{EO}$	DR	A_n	B_n
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance OFF-state



(1) P-channel MOS transistor conducting.
(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

Fig. 4 Typical output source current characteristic.

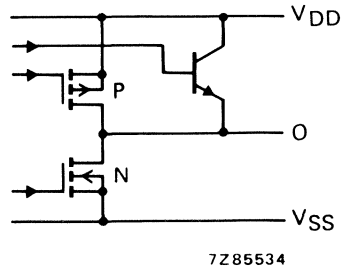


Fig. 5 Schematic diagram of output stage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10	mA
D.C. source or sink current into any output	$\pm I_O$	max.	25	mA
D.C. current into the supply terminals	$\pm I$	max.	100	mA

D.C. CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 typ.	+25 max.	+85 min.	+85 max.	
Output current HIGH	5	4,6		$-I_{OH}$	0,75		0,6	1,2		0,45		mA
	10	9,5			1,85		1,5	3,0		1,1		mA
	15	13,5			14,5		15	50		15,5		mA
Output current HIGH	5	3,6		$-I_{OH}$	9,3		10	24		10,7		mA
	10	8,4			14,4		15	46		15,0		mA
	15	13,2			19,5		20	62		19,8		mA
Output current LOW	5		0,4	I_{OL}	2,9		2,3	5,4		1,75		mA
	10		0,5		9,5		7,6	17		5,50		mA
	15		1,5		30,0		25	45		19,0		mA
Hysteresis voltage (any input)	5			V_H				220				mV
	10							250				mV
	15							320				mV
3-state input/output leakage current pins A_n or B_n	15			I_{OZ}*	−	1,6	−	−	1,6	−	12	μA

* Relevant output in OFF-state; A_n at V_{SS} or V_{DD}; B_n at V_{SS} or V_{DD}.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
A_n → B_n	5			95	190	ns	83 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	35 ns + (0,10 ns/pF) C_L
	15			30	60	ns	26 ns + (0,07 ns/pF) C_L
A_n → B_n	5			85	170	ns	82 ns + (0,06 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	38 ns + (0,03 ns/pF) C_L
	15			30	60	ns	29 ns + (0,02 ns/pF) C_L
Output transition times	5			40	80	ns	see Fig. 6
	10	t_{THL}		20	40	ns	
HIGH to LOW	15			15	30	ns	
	5			30	60	ns	
LOW to HIGH	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO}$ → A_n, B_n	5			100	200	ns	
HIGH	10	t_{PHZ}		50	100	ns	
	15			40	80	ns	
	5			100	200	ns	
LOW	10	t_{PLZ}		60	120	ns	
	15			50	100	ns	
Output enable times							
$\overline{EO}$ → A_n, B_n	5			100	200	ns	
HIGH	10	t_{PZH}		45	90	ns	
	15			35	70	ns	
	5			115	230	ns	
LOW	10	t_{PZL}		55	110	ns	
	15			45	90	ns	

all buffers switching	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	4 250 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	17 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	46 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

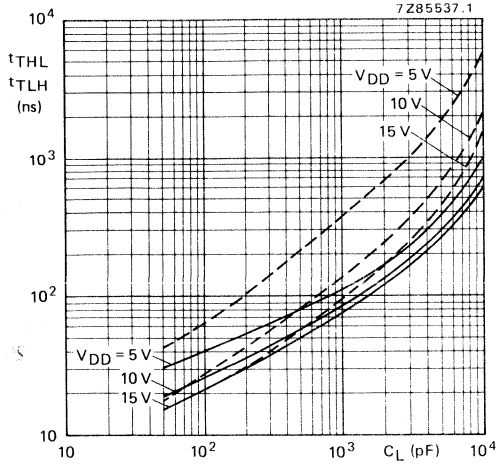


Fig. 6 Output transition times as a function of the load capacitance.
——— t_{TLH}; – – – – t_{THL}.

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

The HEF40373B is an 8-bit transparent latch with 3-state buffered outputs. The output stages have high current output capability suitable for driving highly capacitive loads. The latch outputs follow the data inputs when the latch enable (E) is HIGH. When E is LOW, the data that meets the set-up times is latched. The 3-state outputs are controlled by the output enable input $\overline{EO}$. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device features hysteresis on the E input to improve noise rejection.
Schmitt-trigger action in the E input makes the circuit highly tolerant to slower input rise and fall times.

The HEF40373B is pin and functionally compatible with the TTL '373' device.
Supply voltage range: 3 to 15 V.

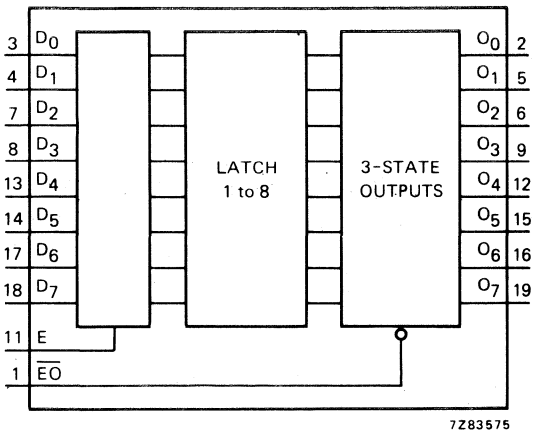


Fig. 1 Functional diagram.

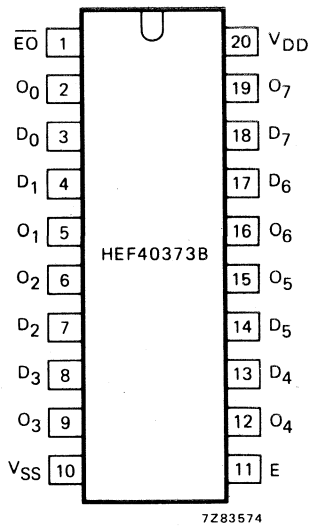


Fig. 2 Pinning diagram.

HEF40373BP : 20-lead DIL; plastic (SOT-146).
HEF40373BT : 20-lead mini-pack; plastic (SO-20; SOT-163A).

PINNING

D_0 to D_7	data inputs
E	latch enable input
$\overline{EO}$	output enable input (active LOW)
O_0 to O_7	3-state buffered outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

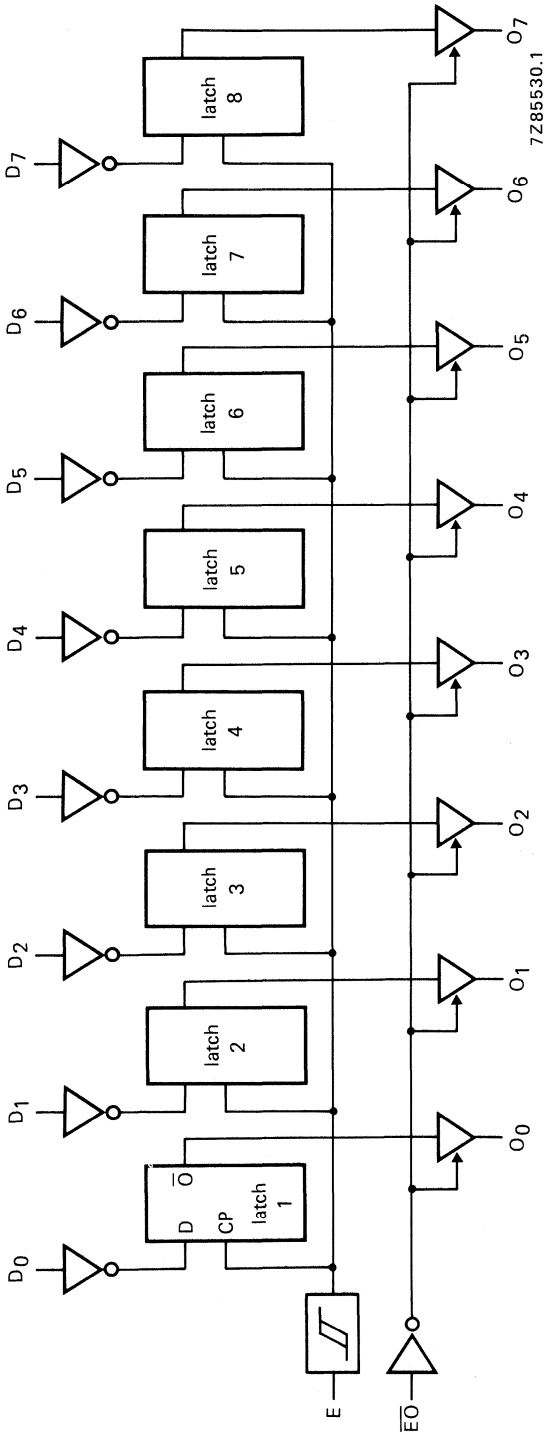


Fig. 3 Logic diagram.

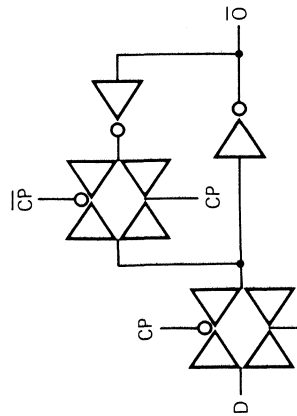


Fig. 4 Logic diagram (one latch).

FUNCTION TABLE

operating modes	inputs			internal register	outputs O_0 to O_7
	$\overline{EO}$	E	D_n		
enable & read register	L	H	L	L	L
	L	H	H	H	H
latch & read register	L	L	l	L	L
	L	L	h	H	H
latch register & disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH state (the more positive voltage)
h = HIGH state (one set-up time prior to the HIGH-to-LOW enable transition)
L = LOW state (the less positive voltage)
l = LOW state (one set-up time prior to the HIGH-to-LOW enable transition)
Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10	mA
D.C. source or sink current into any output	$\pm I_O$	max.	25	mA
D.C. current into the supply terminals	$\pm I$	max.	100	mA

D.C. CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 typ.	+25 min.	+25 typ.	+85 min.	+85 typ.	
Output current HIGH	5	4,6		$-I_{OH}$	0,75		0,6	1,2	0,45		mA
	10	9,5			1,85		1,5	3,0	1,1		mA
	15	13,5			14,5		15	50	15,5		mA
Output current HIGH	5	3,6		$-I_{OH}$	9,3		10	24	10,7		mA
	10	8,4			14,4		15	46	15,0		mA
	15	13,2			19,5		20	62	19,8		mA
Output current LOW	5		0,4	I_{OL}	2,9		2,3	5,4	1,75		mA
	10		0,5		9,5		7,6	17	5,50		mA
	15		1,5		30,0		25	45	19,0		mA
Hysteresis voltage at enable input (E)	5			V_H				220			mV
	10							250			mV
	15							320			mV

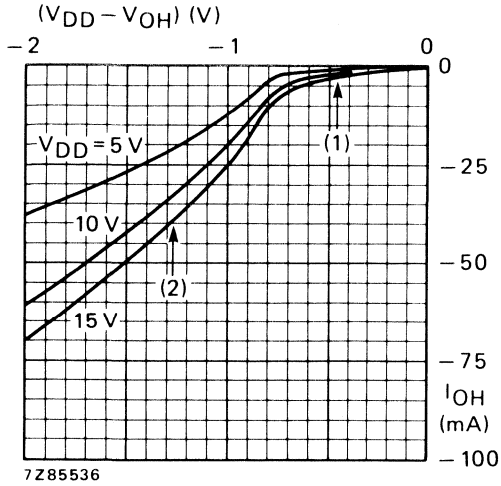


Fig. 5 Typical output source current characteristic.

(1) P-channel MOS transistor conducting.
(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

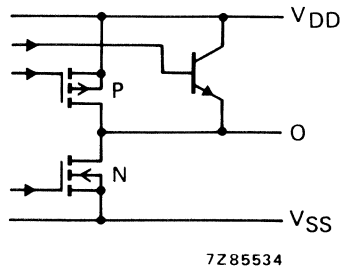


Fig. 6 Schematic diagram of output stage.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
E → O_n	5			150	300	ns	138 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	59 ns + (0,01 ns/pF) C_L
	15			40	80	ns	36 ns + (0,07 ns/pF) C_L
E → O_n	5			125	250	ns	122 ns + (0,06 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	48 ns + (0,03 ns/pF) C_L
	15			40	80	ns	39 ns + (0,02 ns/pF) C_L
Output transition times	5			40	80	ns	see Fig. 7.
	10	t_{THL}		20	40	ns	
HIGH to LOW	15			15	30	ns	
	5			30	60	ns	
LOW to HIGH	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO}$ → O_n	5			65	130	ns	
HIGH	10	t_{PHZ}		30	60	ns	
	15			25	50	ns	
	5			75	150	ns	
LOW	10	t_{PLZ}		40	80	ns	
	15			30	60	ns	
Output enable times							
$\overline{EO}$ → O_n	5			65	130	ns	
HIGH	10	t_{PZH}		30	60	ns	
	15			25	50	ns	
	5			85	170	ns	
LOW	10	t_{PZL}		35	70	ns	
	15			25	50	ns	
Set-up time	5		15	7		ns	
D_n → E	10	t_{su}	10	5		ns	
	15		10	5		ns	
Hold time	5		25	15		ns	
D_n → E	10	t_{hold}	15	4		ns	
	15		10	3		ns	
Minimum latch enable pulse width LOW	5		60	30		ns	
	10	t_{WEL}	30	15		ns	
	15		20	10		ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	3325 f_i + Σ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	14200 f_i + Σ($f_o C_L$) × V_{DD}^2	
	15	37425 f_i + Σ($f_o C_L$) × V_{DD}^2	

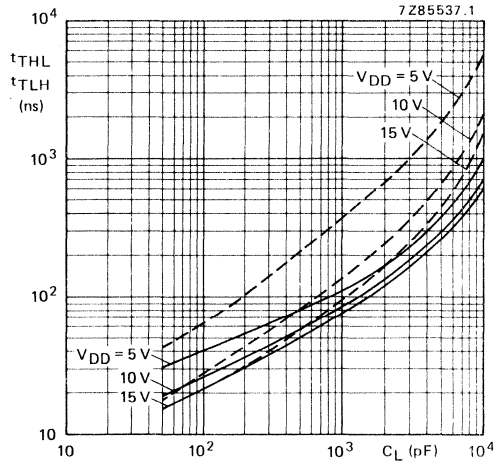


Fig. 7 Output transition times as a function of the load capacitance.
——— t_{TLH}; – – – – t_{THL}.

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The HEF40374B is an octal D-type flip-flop with 3-state buffered outputs with a common clock input (CP). The device is used primarily as an 8-bit positive edge-triggered storage register for interfacing with a 3-state bus. Data on the D-inputs is transferred to storage during the LOW-to-HIGH transition of the clock (CP) input. The 3-state output buffers are controlled by an active LOW output enable input ($\overline{EO}$). A HIGH on $\overline{EO}$ forces the eight outputs to a high impedance OFF-state. When $\overline{EO}$ is LOW, the data in the register appears at the outputs.

The output stages have high current output capability suitable for driving highly capacitive loads.
The device features hysteresis on the CP input to improve noise rejection.
Schmitt-trigger action in the E input makes the circuit highly tolerant to slower input rise and fall times.

The HEF40373B is pin and functionally compatible with the TTL '374' device.
Supply voltage range: 3 to 15 V.

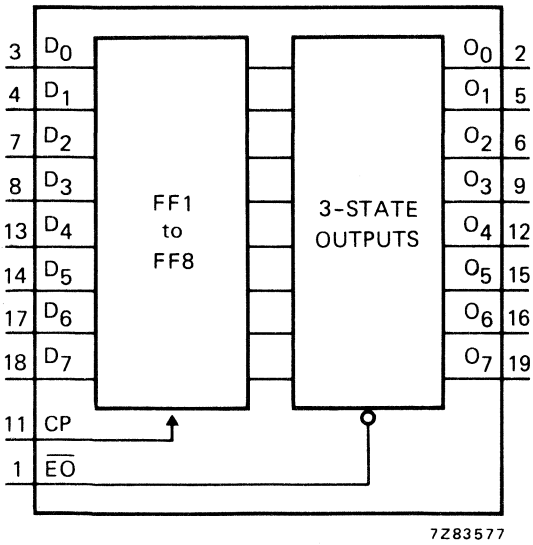


Fig. 1 Functional diagram.

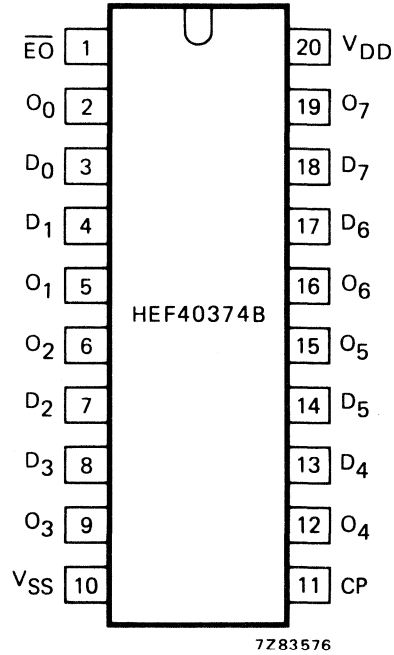


Fig. 2 Pinning diagram.

PINNING

D_0 to D_7	data inputs
CP	clock input
$\overline{EO}$	output enable input (active LOW)
O_0 to O_7	3-state buffered outputs

HEF40374BP : 20-lead DIL; plastic (SOT-146).
HEF40374BT : 20-lead mini-pack; plastic (SO-20; SOT-163A).

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

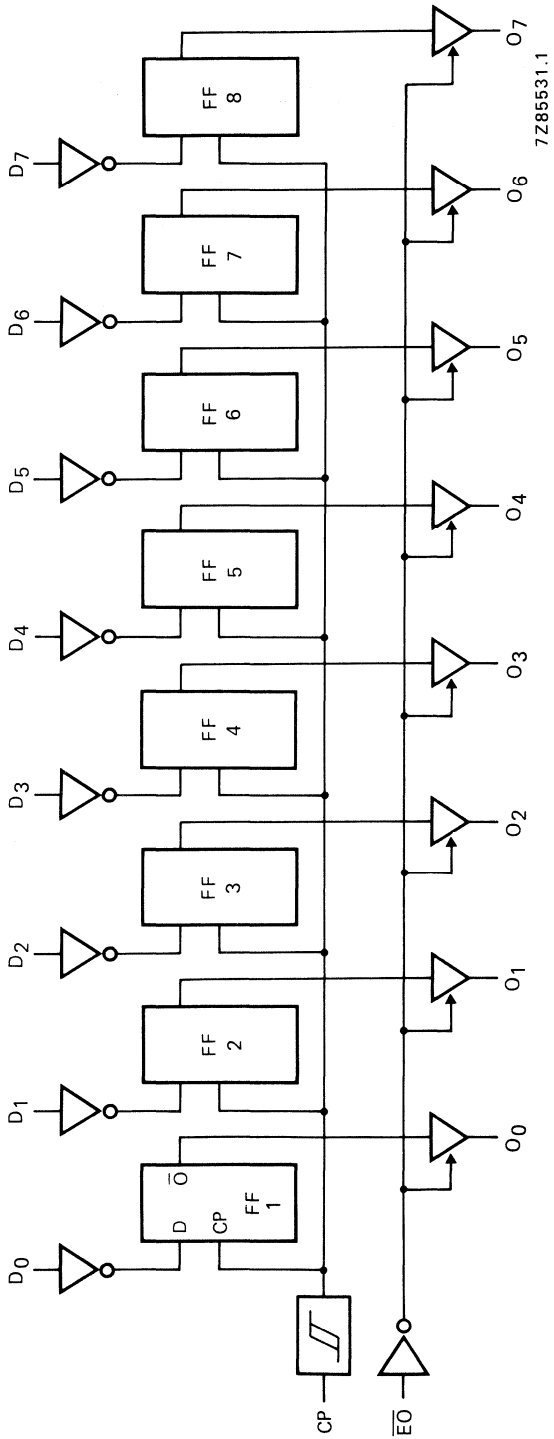


Fig. 3 Logic diagram.

FUNCTION TABLE

operating modes	inputs			internal register	outputs
	$\overline{EO}$	CP	D_n		O_0 to O_7
load & read register	L	∫	l	L	L
	L	∫	h	H	H
load register & disable outputs	H	∫	l	L	Z
	H	∫	h	H	Z

H = HIGH state (the more positive voltage)
h = HIGH state (one set-up time prior to the LOW-to-HIGH clock transition)
L = LOW state (the less positive voltage)
l = LOW state (one set-up time prior to the LOW-to-HIGH clock transition)
Z = high impedance OFF-state
∫ = LOW-to-HIGH clock transition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10	mA
D.C. source or sink current into any output	$\pm I_O$	max.	25	mA
D.C. current into the supply terminals	$\pm I$	max.	100	mA

D.C. CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 typ.	+25 min.	+25 typ.	+85 min.	+85 typ.	
Output current HIGH	5	4,6		$-I_{OH}$	0,75		0,6	1,2	0,45		mA
	10	9,5			1,85		1,5	3,0	1,1		mA
	15	13,5			14,5		15	50	15,5		mA
Output current HIGH	5	3,6		$-I_{OH}$	9,3		10	24	10,7		mA
	10	8,4			14,4		15	46	15,0		mA
	15	13,2			19,5		20	62	19,8		mA
Output current LOW	5		0,4	I_{OL}	2,9		2,3	5,4	1,75		mA
	10		0,5		9,5		7,6	17	5,50		mA
	15		1,5		30,0		25	45	19,0		mA
Hysteresis voltage at clock input (CP)	5			V_H				220			mV
	10							250			mV
	15							320			mV

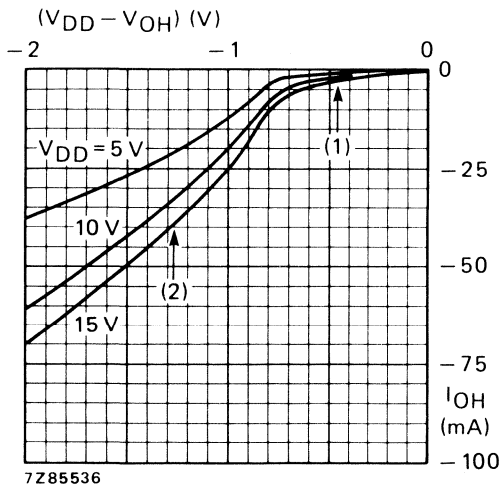


Fig. 4 Typical output source current characteristic.

(1) P-channel MOS transistor conducting.
(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

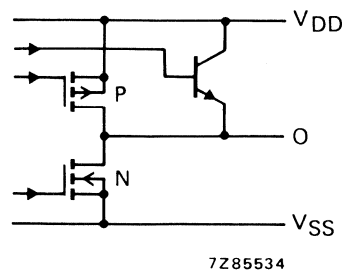


Fig. 5 Schematic diagram of output stage.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			125	250	ns	113 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	54 ns + (0,01 ns/pF) C_L
	15			40	80	ns	36 ns + (0,07 ns/pF) C_L
CP → O_n	5			125	250	ns	122 ns + (0,06 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	53 ns + (0,03 ns/pF) C_L
	15			40	80	ns	39 ns + (0,02 ns/pF) C_L
Output transition times	5			40	80	ns	see Fig. 6
	10	t_{THL}		20	40	ns	
HIGH to LOW	15			15	30	ns	
	5			30	60	ns	
LOW to HIGH	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO}$ → O_n	5			60	120	ns	
HIGH	10	t_{PHZ}		30	60	ns	
	15			24	48	ns	
	5			70	140	ns	
LOW	10	t_{PLZ}		35	70	ns	
	15			30	60	ns	
Output enable times							
$\overline{EO}$ → O_n	5			65	130	ns	
HIGH	10	t_{PZH}		30	60	ns	
	15			24	48	ns	
	5			85	170	ns	
LOW	10	t_{PZL}		35	70	ns	
	15			25	50	ns	
Set-up time	5		20	0		ns	
D_n → CP	10	t_{su}	20	2		ns	
	15		20	5		ns	
Hold time	5		20	10		ns	
D_n → CP	10	t_{hold}	15	2		ns	
	15		10	0		ns	
Minimum clock pulse width; LOW	5		50	25		ns	
	10	t_{WCPL}	25	12		ns	
	15		20	10		ns	
Maximum clock pulse frequency	5		25	5		MHz	
	10	f_{max}	6	12		MHz	
	15		8	17		MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	3 775 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	15 700 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	40 575 f_i + Σ($f_o C_L$) x V_{DD}^2	

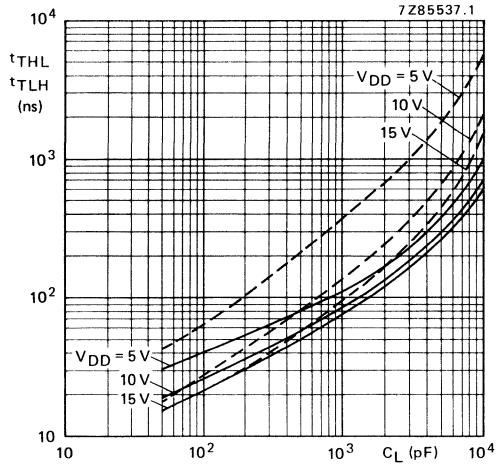
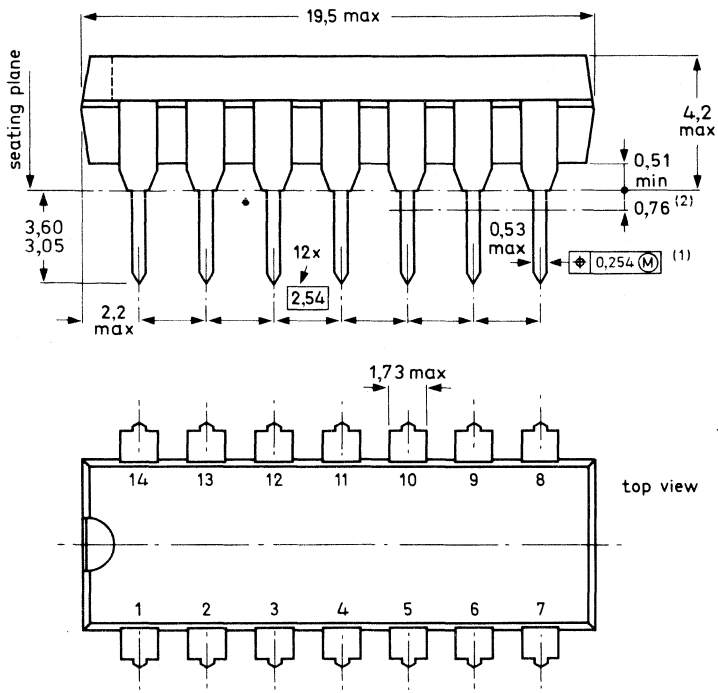


Fig. 6 Output transition times as a function of the load capacitance.
——— t_{TLH}; – – – – t_{THL}.

PACKAGE INFORMATION

Package outlines
Soldering

14-LEAD DUAL IN-LINE; PLASTIC (SOT27)



⊕ Positional accuracy.

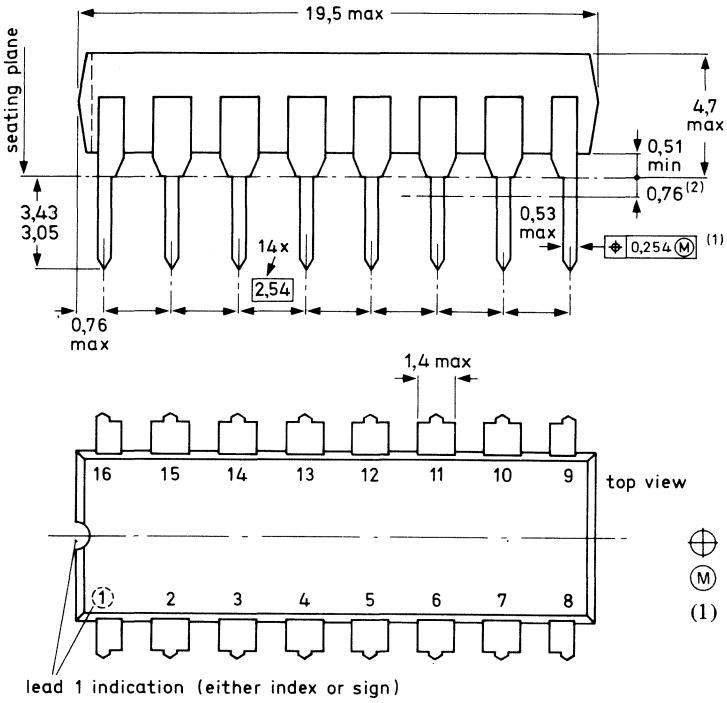
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38Z)



⊕ Positional accuracy.

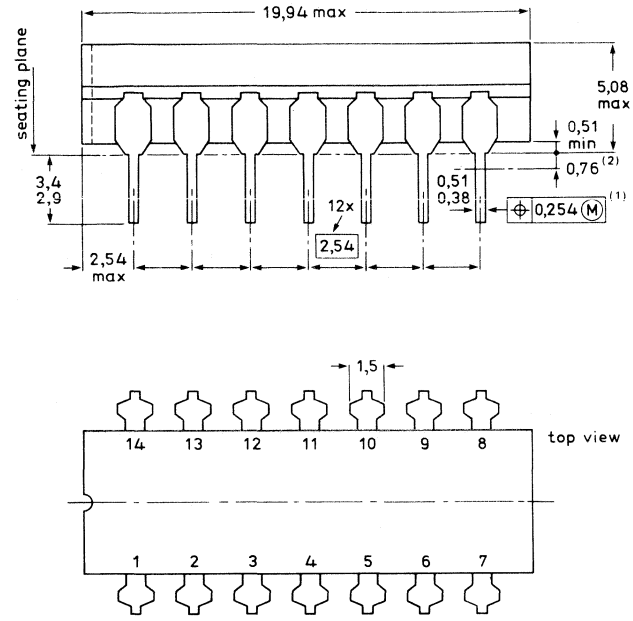
Ⓜ Maximum Material Condition.

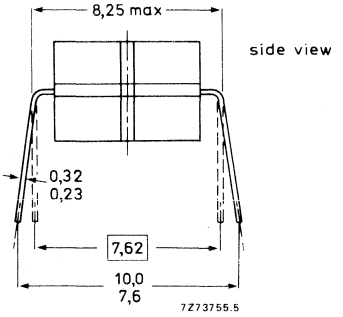
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

14-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT73)





Dimensions in mm

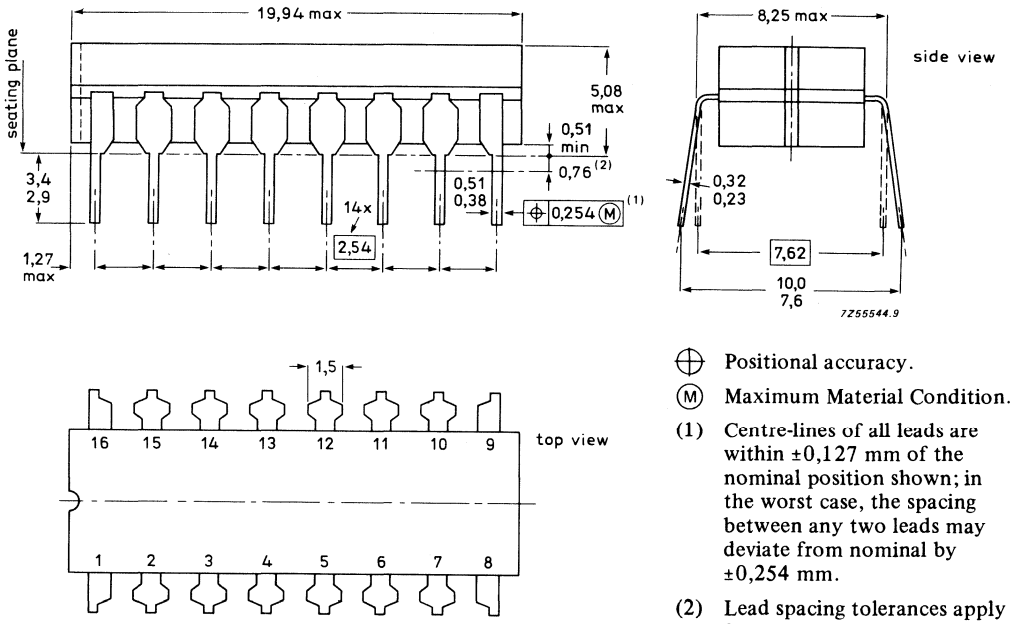
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT74)



Dimensions in mm

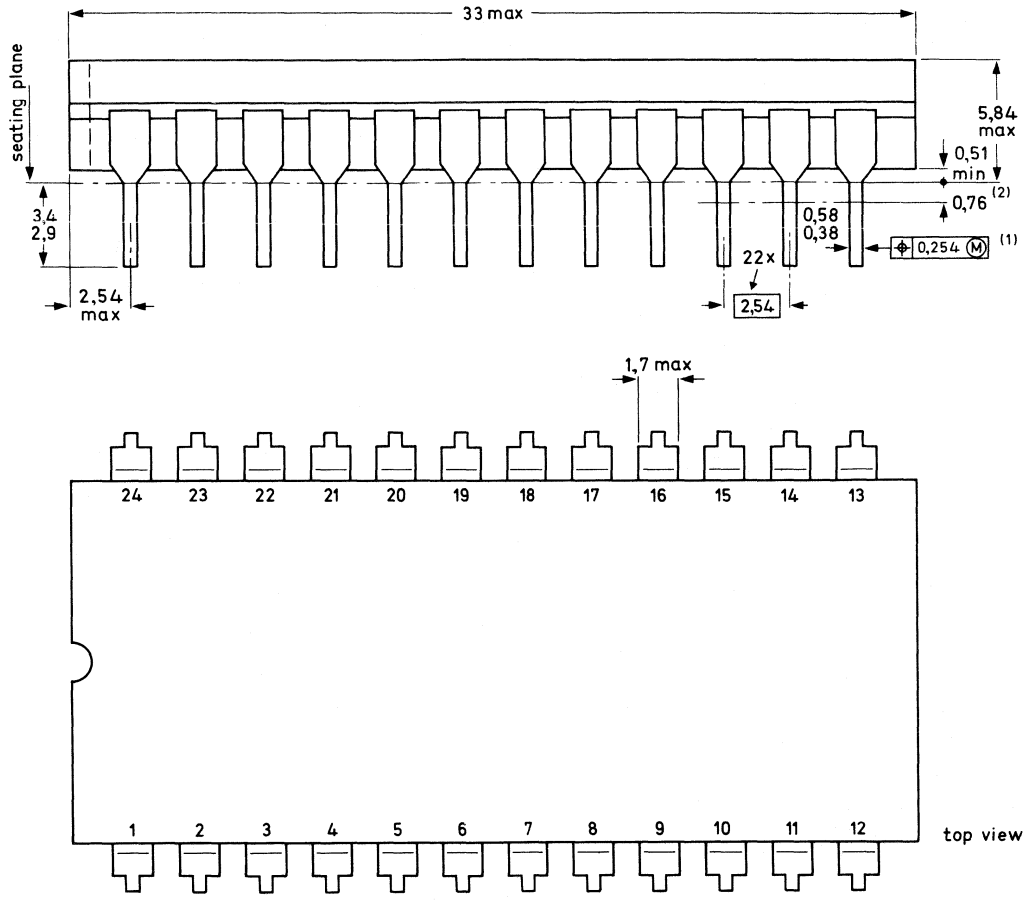
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

24-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT94)



⊕ Positional accuracy.

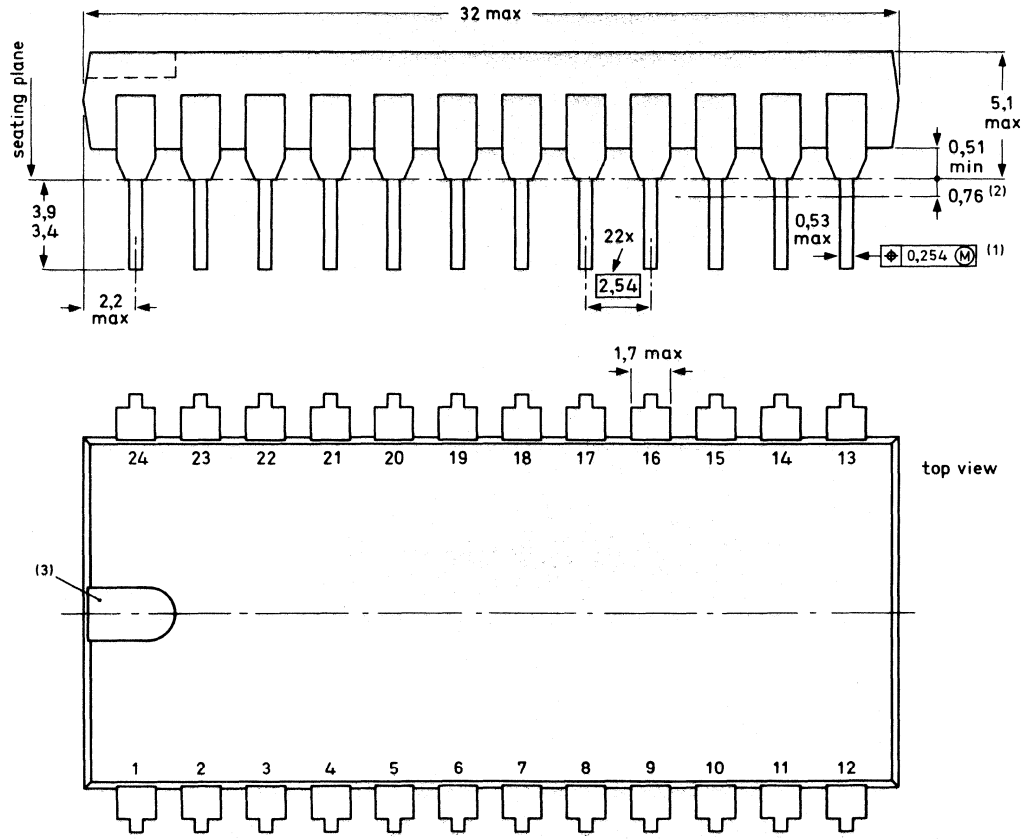
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

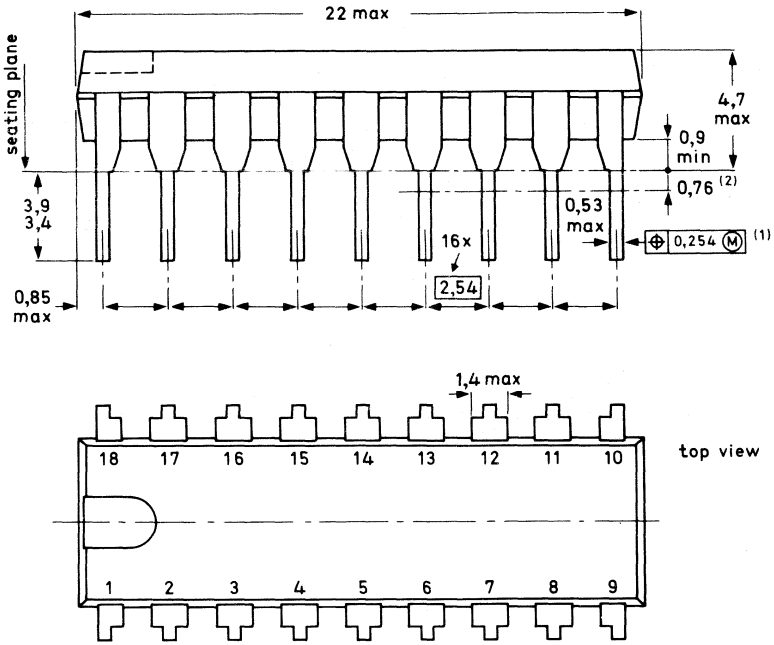
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102)



⊕ Positional accuracy.

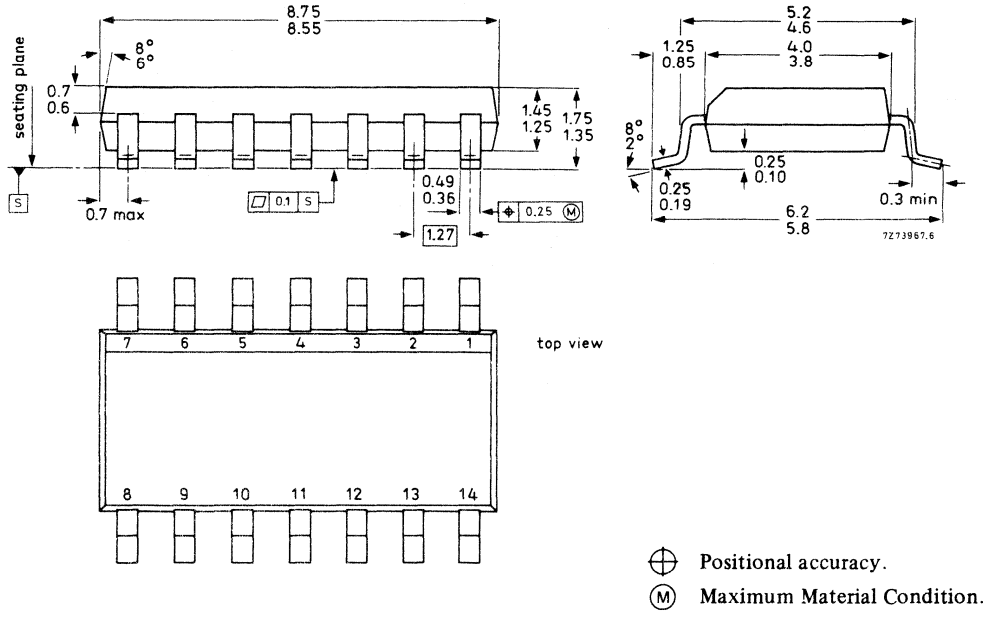
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

14-LEAD MINI-PACK; PLASTIC (SO14; SOT108A)

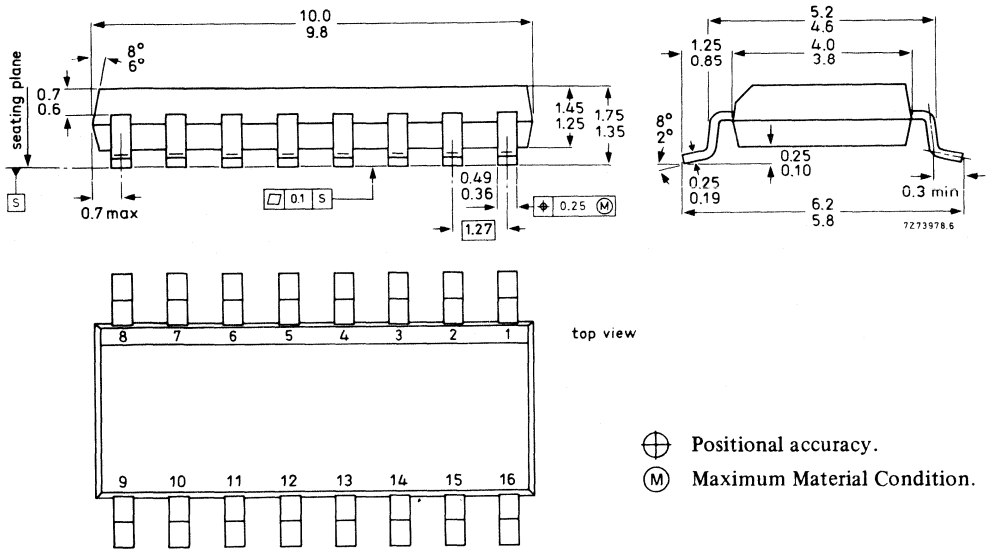


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

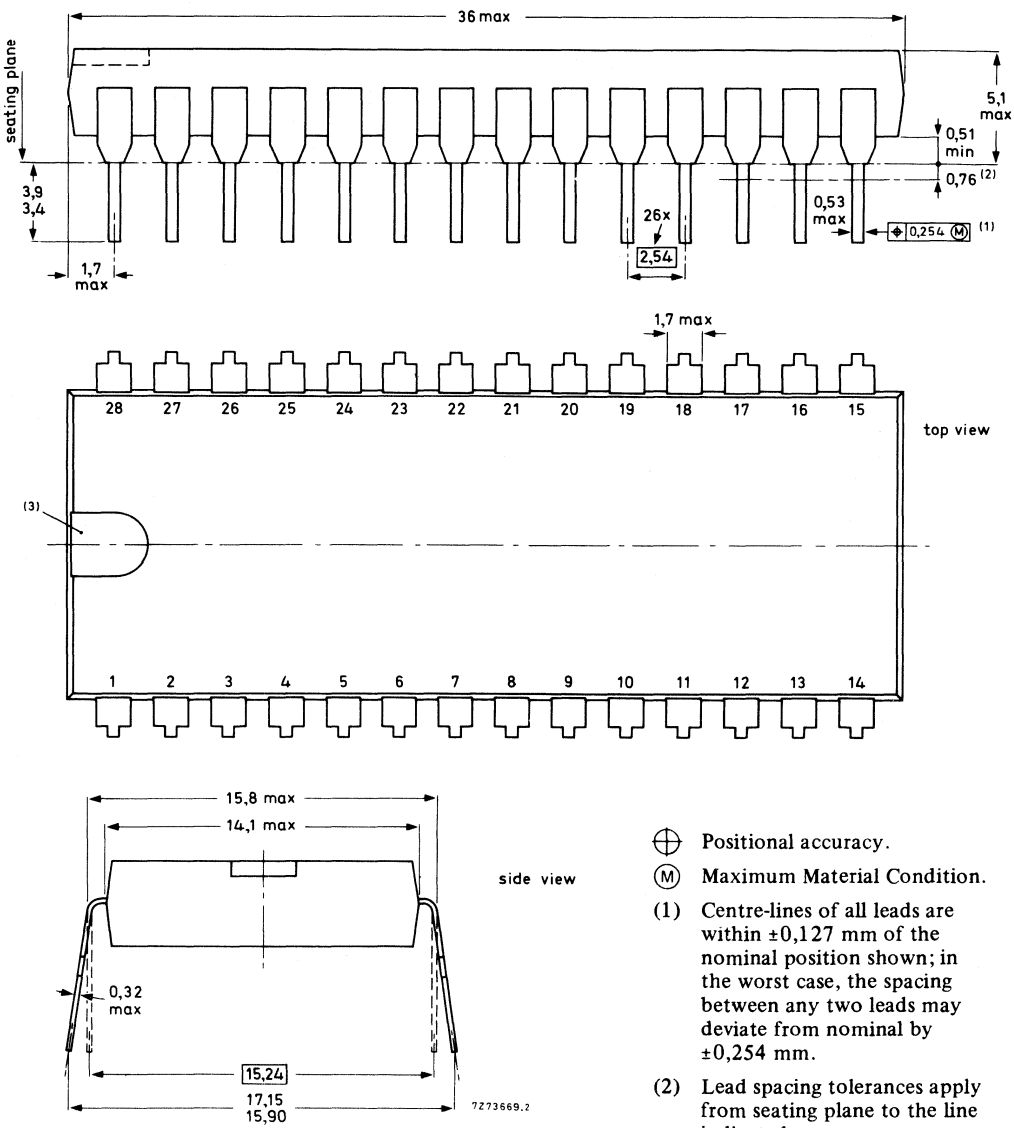
Dimension in mm

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)



Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

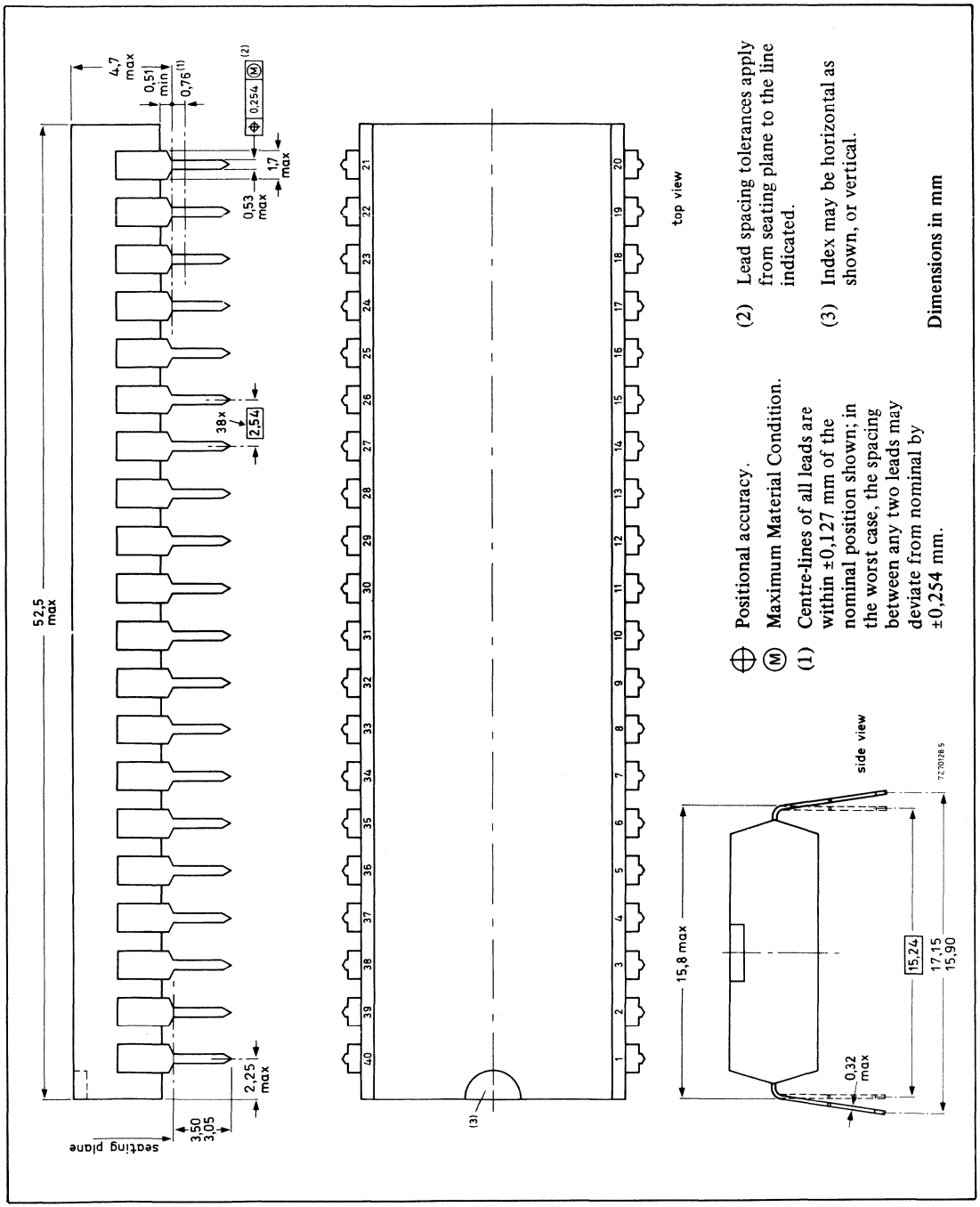
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

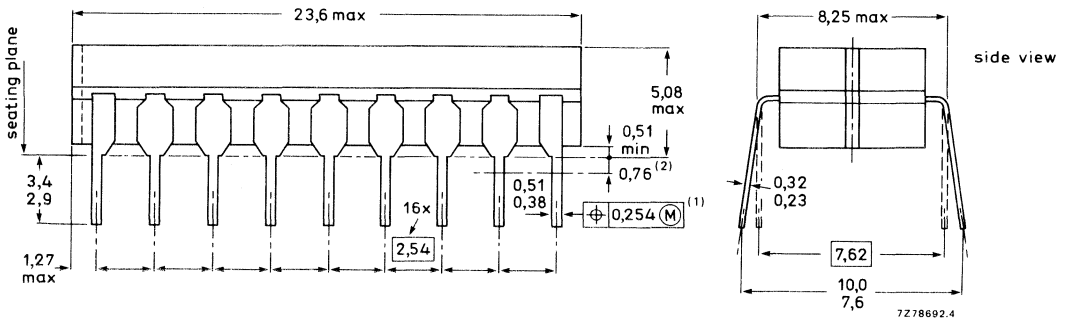
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

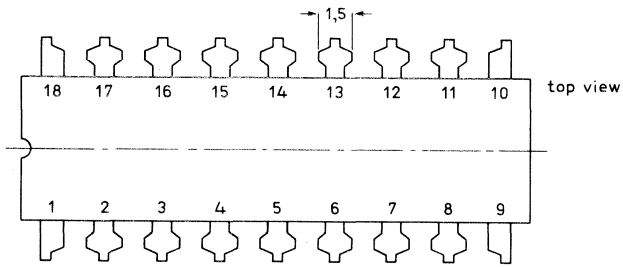
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT133B)





Dimensions in mm

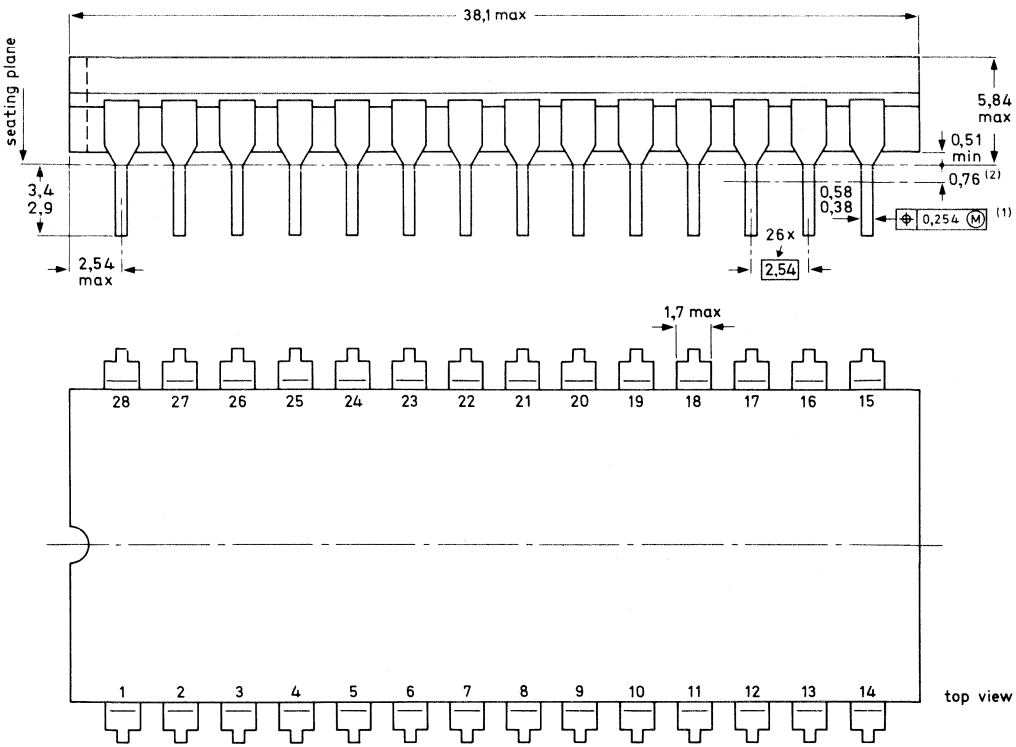
⊕ Positional accuracy.

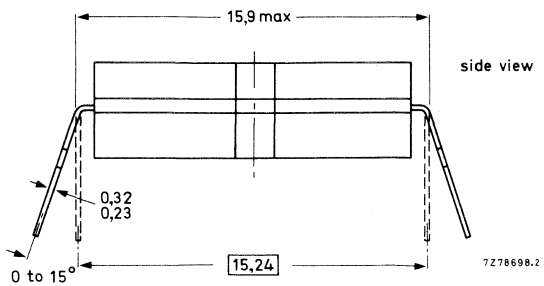
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT135A)





⊕ Positional accuracy.

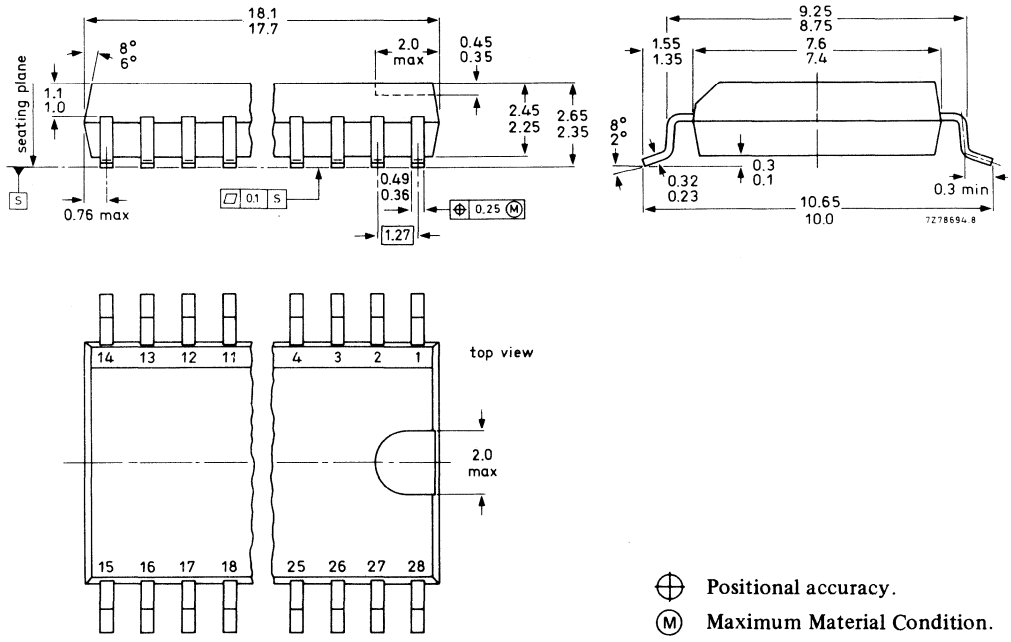
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)

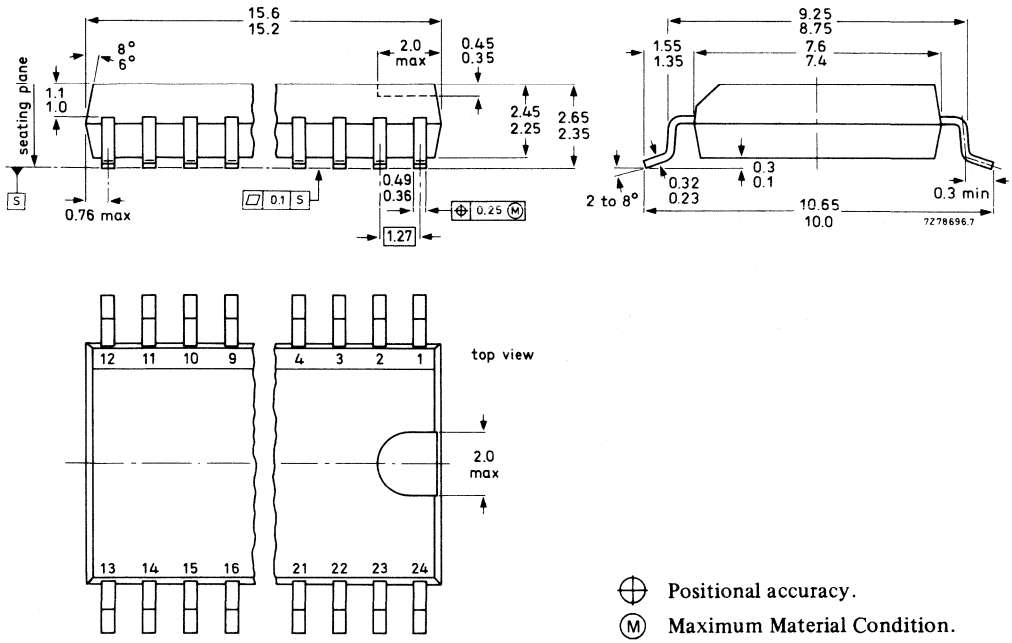


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

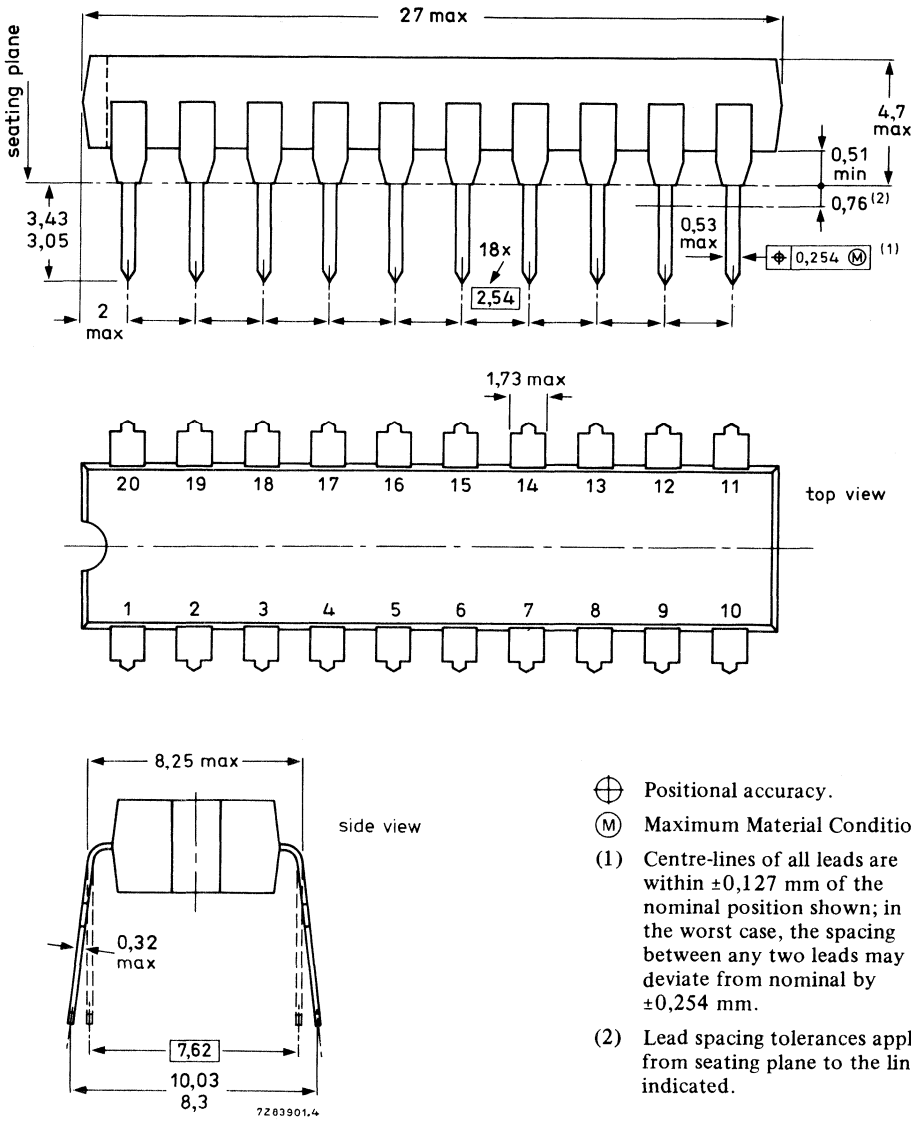
Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)



Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

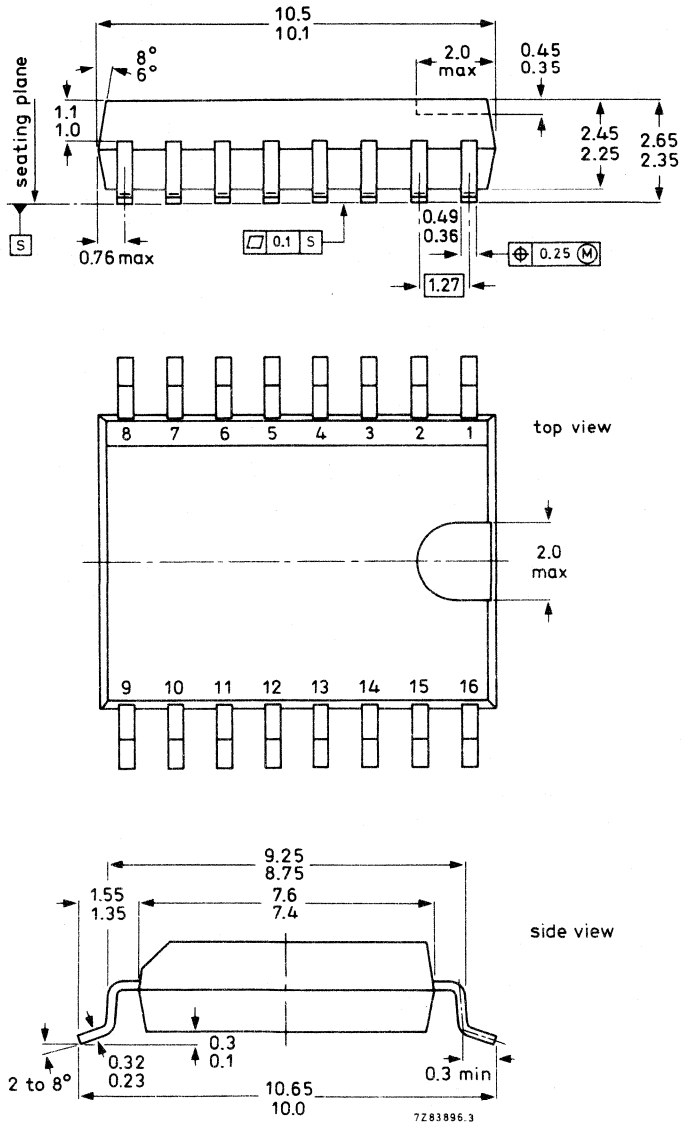
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

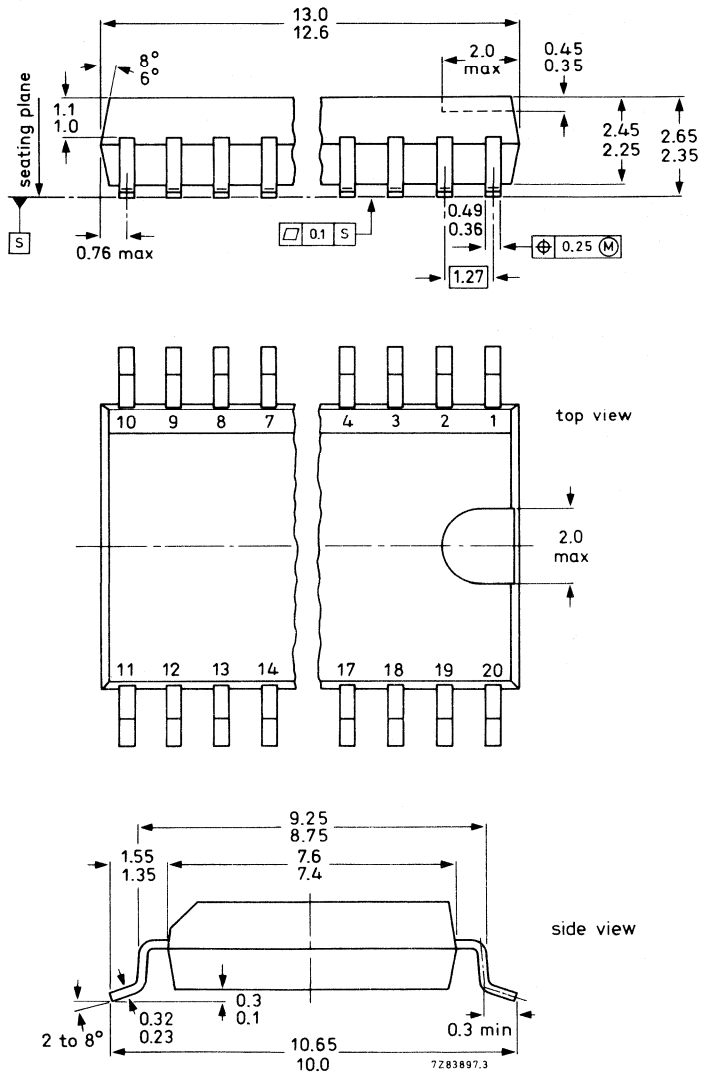


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to vii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

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The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T8 **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers and infrared detectors**

T15 **Dry reed switches**

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

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The red series of data handbooks comprises:

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Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8a **Light-emitting diodes**

S8b **Devices for optoelectronics**
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9 **PowerMos transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave transistors**

S12 **Surface acoustic wave devices**

S13 **Semiconductor sensors**

S14 **Liquid Crystal Displays**

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IC02a/b	**Video and associated systems** Bipolar, MOS	
IC03	**Integrated circuits for telephony** Bipolar, MOS	
IC04	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family – uncased ICs** CMOS	
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family	
IC08	**ECL 10K and 100K logic families**	
IC09N	**TTL logic series**	
IC10	**Memories** MOS, TTL, ECL	
IC11	**Linear Products**	
Supplement to IC11	**Linear Products**	
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